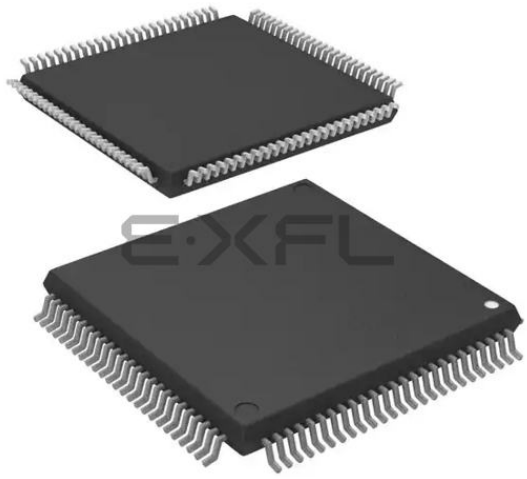
Renesas Electronics America Inc - R5F524TAADFP#30 Datasheet



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Applications of "Embedded - Microcontrollers"

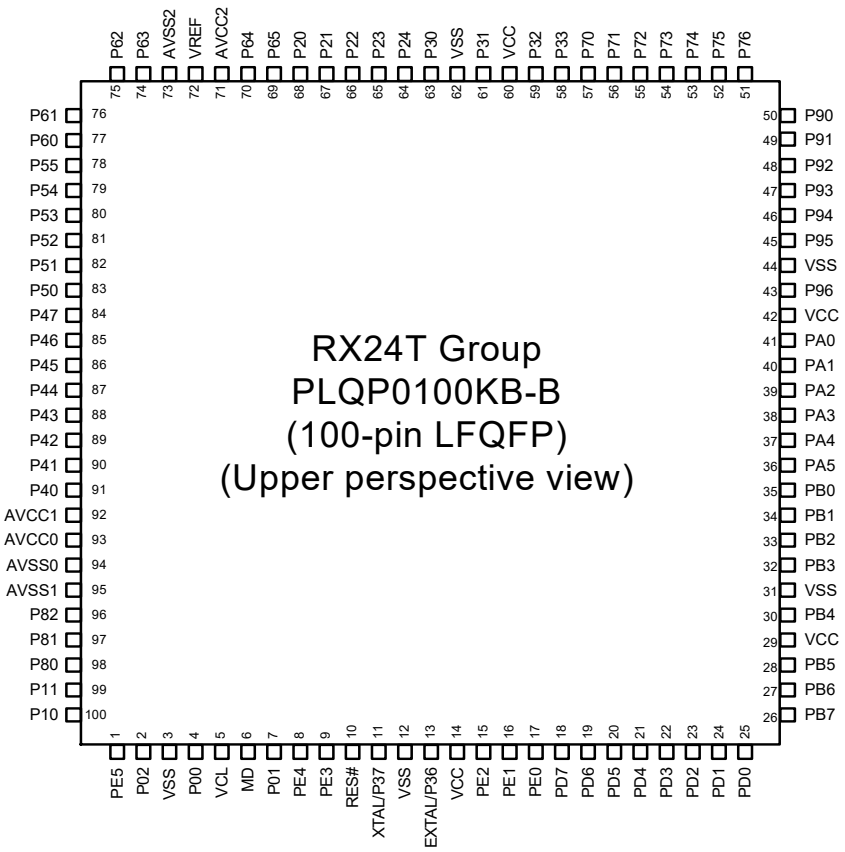
Details	
Product Status	Discontinued at Digi-Key
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	80
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 22x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f524taadfp-30

Table 1.4 Pin Functions (2/4)

Classifications	Pin Name	I/O	Description
Multi-function timer pulse unit 3 (MTU3d)	MTIOC9A#, MTIOC9B#, MTIOC9C#, MTIOC9D#	I/O	The TGRA9 to TGRD9 input capture inverted input/output compare inverted output/PWM inverted output pins.
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for the external clock.
	MTCLKA#, MTCLKB#, MTCLKC#, MTCLKD#	Input	Inverted input pins for the external clock.
	ADSM0, ADSM1	Output	A/D trigger output pins.
General PWM timer (GPTB)	GTIOC0A, GTIOC0B	I/O	The GPT0.GTGRA and GPT0.GTGRB input capture input/output compare output/PWM output pins
	GTIOC0A#, GTIOC0B#	I/O	The GPT0.GTGRA and GPT0.GTGRB input capture inverted input/output compare inverted output/PWM inverted output pins
	GTIOC1A, GTIOC1B	I/O	The GPT1.GTGRA and GPT1.GTGRB input capture input/output compare output/PWM output pins
	GTIOC1A#, GTIOC1B#	I/O	The GPT1.GTGRA and GPT1.GTGRB input capture inverted input/output compare inverted output/PWM inverted output pins
	GTIOC2A, GTIOC2B	I/O	The GPT2.GTGRA and GPT2.GTGRB input capture input/output compare output/PWM output pins
	GTIOC2A#, GTIOC2B#	I/O	The GPT2.GTGRA and GPT2.GTGRB input capture inverted input/output compare inverted output/PWM inverted output pins
	GTIOC3A, GTIOC3B	I/O	The GPT3.GTGRA and GPT3.GTGRB input capture input/output compare output/PWM output pins
	GTIOC3A#, GTIOC3B#	I/O	The GPT3.GTGRA and GPT3.GTGRB input capture inverted input/output compare inverted output/PWM inverted output pins
	GTETRG	Input	External trigger input pin for GPT0 to GPT3
	GTECLKA, GTECLKB, GTECLKC, GTECLKD	Input	Input pins A to D for the external clock
	GTADSM0, GTADSM1	Output	A/D conversion start request monitoring output pins
8-bit timer (TMR)	TMO0 to TMO7	Output	Compare match output pins.
	TMCI0 to TMCI7	Input	Input pins for the external clock to be input to the counter.
	TMRI0 to TMRI7	Input	Counter reset input pins.
Port output enable 3 (POE3b, POE3A)	POE0#, POE4#, POE8#, POE10#, POE11#, POE12#	Input	Input pins for request signals to switch the MTU and GPT pins between the high impedance state or operation as general I/O port pins
Serial communications interface (SCIg)	• Asynchronous mode/clock synchronous mode		
	SCK1, SCK5, SCK6	I/O	Input/output pins for the clock.
	RXD1, RXD5, RXD6	Input	Input pins for received data.
	TXD1, TXD5, TXD6	Output	Output pins for transmitted data.
	CTS1#, CTS5#, CTS6#	Input	Input pins for controlling the start of transmission and reception.
	RTS1#, RTS5#, RTS6#	Output	Output pins for controlling the start of transmission and reception.
	• Simple I^2C mode		
	SSCL1, SSCL5, SSCL6	I/O	Input/output pins for the I^2C clock.
	SSDA1, SSDA5, SSDA6	I/O	Input/output pins for the I^2C data.
	• Simple SPI mode		
	SCK1, SCK5, SCK6	I/O	Input/output pins for the clock.
	SMISO1, SMISO5, SMISO6	I/O	Input/output pins for slave transmit data.
	SMOSI1, SMOSI5, SMOSI6	I/O	Input/output pins for master transmit data.
	SS1#, SS5#, SS6#	Input	Chip-select input pins.

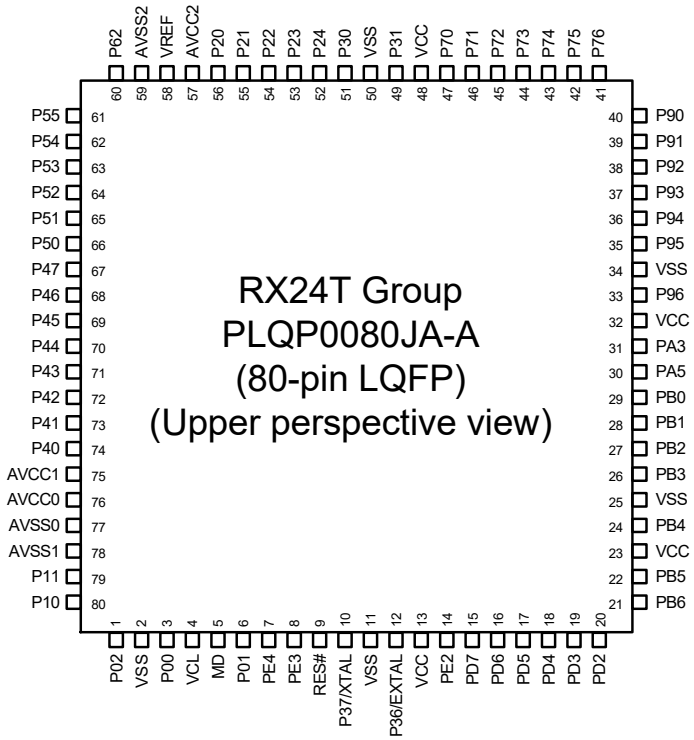
1.5 Pin Assignments

Figure 1.3 to Figure 1.6 shows the pin assignments. Table 1.5 to Table 1.8 shows the lists of pins and pin functions.



Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, refer to List of Pins and Pin Functions (100-Pin LFQFP, Chip Version A) or (100-Pin LFQFP, Chip Version B).

Figure 1.3 Pin Assignments of the 100-Pin LFQFP (Chip Version A and B)



Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, refer to List of Pins and Pin Functions (80-Pin LQFP/LFQFP).

Figure 1.4 Pin Assignments of the 80-Pin LQFP

Table 1.5 List of Pins and Pin Functions (100-Pin LFQFP, Chip Version B) (1/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (TMR, MTU, POE, CAC, GPT)	Communications (SCI, RSPI, RIIC, RSCAN)	Others
1		PE5			IRQ0
2		P02	MTIOC9D, MTIOC9D#	CTS1#, RTS1#, SS1#	IRQ5, ADST0
3	VSS				
4		P00			IRQ2, ADST1
5	VCL				
6	MD				FINED
7		P01	POE12#		IRQ4, ADST2
8		PE4	MTCLKC, MTCLKC#, POE10#		IRQ1
9		PE3	MTCLKD, MTCLKD#, POE11#		IRQ2
10	RES#				
11	XTAL	P37			
12	VSS				
13	EXTAL	P36			
14	VCC				
15		PE2	POE10#		NMI
16		PE1	MTIOC9D, MTIOC9D#, TMO5	CTS5#, RTS5#, SS5#, SSLA3	
17		PE0	MTIOC9B, MTIOC9B#, TMCI1, TMCI5	RXD5, SMISO5, SSCL5, SSLA2	
18		PD7	MTIOC9A, MTIOC9A#, TMRI1, TMRI5, GTIOC3A, GTIOC3A#	TXD5, SMOSI5, SSDA5, SSLA1	
19		PD6	MTIOC9C, MTIOC9C#, TMO1, GTIOC3B, GTIOC3B#	CTS1#, RTS1#, SS1#, SSLA0	IRQ5, ADST0
20		PD5	TMRI0, TMRI6, GTECLKA	RXD1, SMISO1, SSCL1	IRQ3
21		PD4	TMCI0, TMCI6, GTECLKB	SCK1	IRQ2
22		PD3	TMO0, GTECLKC	TXD1, SMOSI1, SSDA1	
23		PD2	TMCI1, TMO4, GTIOC0A, GTIOC0A#	SCK5, MOSIA	
24		PD1	TMO2, GTIOC0B, GTIOC0B#	MISOA	
25		PD0	TMO6, GTIOC1A, GTIOC1A#	RSPCKA	
26		PB7	GTIOC1B, GTIOC1B#	SCK5	
27		PB6	GTIOC2A, GTIOC2A#	RXD5, SMISO5, SSCL5	IRQ5
28		PB5	GTIOC2B, GTIOC2B#	TXD5, SMOSI5, SSDA5	
29	VCC				
30		PB4	POE8#, GTETRG, GTECLKD	CTS5#, RTS5#, SS5#	IRQ3
31	VSS				
32		PB3	MTIOC0A, MTIOC0A#, CACREF	SCK6, RSPCKA	
33		PB2	MTIOC0B, MTIOC0B#, TMRI0, ADSM0	TXD6, SMOSI6, SSDA6, SDA0	
34		PB1	MTIOC0C, MTIOC0C#, TMCI0, ADSM1	RXD6, SMISO6, SSCL6, SCL0	
35		PB0	MTIOC0D, MTIOC0D#, TMO0	TXD6, SMOSI6, SSDA6, MOSIA	ADTRG2#
36		PA5	MTIOC1A, MTIOC1A#, TMCI3	RXD6, SMISO6, SSCL6, MISOA	IRQ1, ADTRG1#
37		PA4	MTIOC1B, MTIOC1B#, TMCI7	SCK6, RSPCKA	ADTRG0#
38		PA3	MTIOC2A, MTIOC2A#, TMRI7, GTADSM0	SSLA0	
39		PA2	MTIOC2B, MTIOC2B#, TMO7, GTADSM1	CTS6#, RTS6#, SS6#, SSLA1	
40		PA1	MTIOC6A, MTIOC6A#, TMO4	SSLA2, CRXD0	ADTRG0#
41		PA0	MTIOC6C, MTIOC6C#, TMO2	SSLA3, CTXD0	
42	VCC				
43		P96	POE4#		IRQ4
44	VSS				
45		P95	MTIOC6B, MTIOC6B#		
46		P94	MTIOC7A, MTIOC7A#		
47		P93	MTIOC7B, MTIOC7B#		
48		P92	MTIOC6D, MTIOC6D#		
49		P91	MTIOC7C, MTIOC7C#		
50		P90	MTIOC7D, MTIOC7D#		
51		P76	MTIOC4D, MTIOC4D#, GTIOC2B, GTIOC2B#		

Table 1.5 List of Pins and Pin Functions (100-Pin LFQFP, Chip Version B) (3/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (TMR, MTU, POE, CAC, GPT)	Communications (SCI, RSPI, RIIC, RSCAN)	Others
94	AVSS0				
95	AVSS1				
96		P82	MTIC5U, MTIC5U#, TMO4	SCK6	
97		P81	MTIC5V, MTIC5V#, TMCI4	TXD6, SMOSI6, SSDA6	
98		P80	MTIC5W, MTIC5W#, TMRI4	RXD6, SMISO6, SSCL6	
99		P11	MTIOC3A, MTIOC3A#, MTCLKC, MTCLKC#, TMO3		IRQ1
100		P10	MTIOC9B, MTIOC9B#, MTCLKD, MTCLKD#, TMRI3, POE12#	CTS6#, RTS6#, SS6#	IRQ0

Table 1.7 List of Pins and Pin Functions (80-Pin LQFP/LFQFP) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE, CAC)	Communications (SCI, RSPI, RIIC)	Others
49		P31	MTIOC0A, MTCLKC, TMRI6	SSLA1	IRQ6
50	VSS				
51		P30	MTIOC0B, MTCLKD, TMCI6	SSLA0	IRQ7, COMP3
52		P24	MTIC5U, TMCI2, TMO6	RSPCKA	COMP0
53		P23	MTIC5V, TMO2, CACREF	MOSIA	COMP1
54		P22	MTIC5W, TMRI2, TMO4	MISOA	ADTRG2#, COMP2
55		P21	MTCLKA, MTIOC9A, TMCI4		IRQ6, ADTRG1#, AN116, CVREFC1
56		P20	MTCLKB, MTIOC9C, TMRI4		IRQ7, ADTRG0#, AN016, CVREFC0
57	AVCC2				
58	VREF				
59	AVSS2				
60		P62			AN202, IRQ6
61		P55			AN211, IRQ3
62		P54			AN210, IRQ2
63		P53			AN209, IRQ1
64		P52			AN208, IRQ0
65		P51			AN207
66		P50			AN206
67		P47			AN103
68		P46			AN102, CMPC12, CMPC13, CMPC30, CMPC31
69		P45			AN101, CMPC02, CMPC03, CMPC20, CMPC21
70		P44			AN100, CMPC10, CMPC11, CMPC32, CMPC33
71		P43			AN003
72		P42			AN002
73		P41			AN001
74		P40			AN000, CMPC00, CMPC01, CMPC22, CMPC23
75	AVCC1				
76	AVCC0				
77	AVSS0				
78	AVSS1				
79		P11	MTIOC3A, MTCLKC, TMO3		IRQ1
80		P10	MTIOC9B, MTCLKD, TMRI3, POE12#	CTS6#, RTS6#, SS6#	IRQ0

3. Address Space

3.1 Address Space

This MCU has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.
Figure 3.1 shows the memory maps.

Table 4.1 List of I/O Registers (Address Order) (2/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 6420h	MPU	Region-4 Start Page Number Register	RSPAGE4	32	32	1 ICLK
0008 6424h	MPU	Region-4 End Page Number Register	REPAGE4	32	32	1 ICLK
0008 6428h	MPU	Region-5 Start Page Number Register	RSPAGE5	32	32	1 ICLK
0008 642Ch	MPU	Region-5 End Page Number Register	REPAGE5	32	32	1 ICLK
0008 6430h	MPU	Region-6 Start Page Number Register	RSPAGE6	32	32	1 ICLK
0008 6434h	MPU	Region-6 End Page Number Register	REPAGE6	32	32	1 ICLK
0008 6438h	MPU	Region-7 Start Page Number Register	RSPAGE7	32	32	1 ICLK
0008 643Ch	MPU	Region-7 End Page Number Register	REPAGE7	32	32	1 ICLK
0008 6500h	MPU	Memory-Protection Enable Register	MPEN	32	32	1 ICLK
0008 6504h	MPU	Background Access Control Register	MPBAC	32	32	1 ICLK
0008 6508h	MPU	Memory-Protection Error Status-Clearing Register	MPECLR	32	32	1 ICLK
0008 650Ch	MPU	Memory-Protection Error Status Register	MPESTS	32	32	1 ICLK
0008 6514h	MPU	Data Memory-Protection Error Address Register	MPDEA	32	32	1 ICLK
0008 6520h	MPU	Region Search Address Register	MPSA	32	32	1 ICLK
0008 6524h	MPU	Region Search Operation Register	MPOPS	16	16	1 ICLK
0008 6526h	MPU	Region Invalidation Operation Register	MPOPI	16	16	1 ICLK
0008 6528h	MPU	Instruction-Hit Region Register	MHITI	32	32	1 ICLK
0008 652Ch	MPU	Data-Hit Region Register	MHITD	32	32	1 ICLK
0008 7010h	ICU	Interrupt Request Register 016	IR016	8	8	2 ICLK
0008 7017h	ICU	Interrupt Request Register 023	IR023	8	8	2 ICLK
0008 701Bh	ICU	Interrupt Request Register 027	IR027	8	8	2 ICLK
0008 701Ch	ICU	Interrupt Request Register 028	IR028	8	8	2 ICLK
0008 701Dh	ICU	Interrupt Request Register 029	IR029	8	8	2 ICLK
0008 701Eh	ICU	Interrupt Request Register 030	IR030	8	8	2 ICLK
0008 701Fh	ICU	Interrupt Request Register 031	IR031	8	8	2 ICLK
0008 7020h	ICU	Interrupt Request Register 032	IR032	8	8	2 ICLK
0008 7021h	ICU	Interrupt Request Register 033	IR033	8	8	2 ICLK
0008 7022h	ICU	Interrupt Request Register 034	IR034	8	8	2 ICLK
0008 7028h	ICU	Interrupt Request Register 040*2	IR040	8	8	2 ICLK
0008 7029h	ICU	Interrupt Request Register 041*2	IR041	8	8	2 ICLK
0008 702Ch	ICU	Interrupt Request Register 044	IR044	8	8	2 ICLK
0008 702Dh	ICU	Interrupt Request Register 045	IR045	8	8	2 ICLK
0008 702Eh	ICU	Interrupt Request Register 046	IR046	8	8	2 ICLK
0008 702Fh	ICU	Interrupt Request Register 047	IR047	8	8	2 ICLK
0008 7030h	ICU	Interrupt Request Register 048*2	IR048	8	8	2 ICLK
0008 7031h	ICU	Interrupt Request Register 049*2	IR049	8	8	2 ICLK
0008 7032h	ICU	Interrupt Request Register 050*2	IR050	8	8	2 ICLK
0008 7033h	ICU	Interrupt Request Register 051*2	IR051	8	8	2 ICLK
0008 7034h	ICU	Interrupt Request Register 052*2	IR052	8	8	2 ICLK
0008 7035h	ICU	Interrupt Request Register 053*2	IR053	8	8	2 ICLK
0008 7036h	ICU	Interrupt Request Register 054*2	IR054	8	8	2 ICLK
0008 7037h	ICU	Interrupt Request Register 055*2	IR055	8	8	2 ICLK
0008 7038h	ICU	Interrupt Request Register 056*2	IR056	8	8	2 ICLK
0008 7039h	ICU	Interrupt Request Register 057	IR057	8	8	2 ICLK
0008 703Bh	ICU	Interrupt Request Register 059*2	IR059	8	8	2 ICLK
0008 703Ch	ICU	Interrupt Request Register 060*2	IR060	8	8	2 ICLK
0008 703Dh	ICU	Interrupt Request Register 061*2	IR061	8	8	2 ICLK
0008 703Eh	ICU	Interrupt Request Register 062*2	IR062	8	8	2 ICLK
0008 703Fh	ICU	Interrupt Request Register 063*2	IR063	8	8	2 ICLK
0008 7040h	ICU	Interrupt Request Register 064	IR064	8	8	2 ICLK
0008 7041h	ICU	Interrupt Request Register 065	IR065	8	8	2 ICLK
0008 7042h	ICU	Interrupt Request Register 066	IR066	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (5/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
0008 70D0h	ICU	Interrupt Request Register 208*2	IR208	8	8	2 ICLK
0008 70D1h	ICU	Interrupt Request Register 209*2	IR209	8	8	2 ICLK
0008 70D2h	ICU	Interrupt Request Register 210*2	IR210	8	8	2 ICLK
0008 70D3h	ICU	Interrupt Request Register 211*2	IR211	8	8	2 ICLK
0008 70D4h	ICU	Interrupt Request Register 212*2	IR212	8	8	2 ICLK
0008 70D5h	ICU	Interrupt Request Register 213*2	IR213	8	8	2 ICLK
0008 70D6h	ICU	Interrupt Request Register 214*2	IR214	8	8	2 ICLK
0008 70D7h	ICU	Interrupt Request Register 215*2	IR215	8	8	2 ICLK
0008 70D8h	ICU	Interrupt Request Register 216*2	IR216	8	8	2 ICLK
0008 70D9h	ICU	Interrupt Request Register 217*2	IR217	8	8	2 ICLK
0008 70DAh	ICU	Interrupt Request Register 218	IR218	8	8	2 ICLK
0008 70DBh	ICU	Interrupt Request Register 219	IR219	8	8	2 ICLK
0008 70DCh	ICU	Interrupt Request Register 220	IR220	8	8	2 ICLK
0008 70DDh	ICU	Interrupt Request Register 221	IR221	8	8	2 ICLK
0008 70DEh	ICU	Interrupt Request Register 222	IR222	8	8	2 ICLK
0008 70DFh	ICU	Interrupt Request Register 223	IR223	8	8	2 ICLK
0008 70E0h	ICU	Interrupt Request Register 224	IR224	8	8	2 ICLK
0008 70E1h	ICU	Interrupt Request Register 225	IR225	8	8	2 ICLK
0008 70E2h	ICU	Interrupt Request Register 226	IR226	8	8	2 ICLK
0008 70E3h	ICU	Interrupt Request Register 227	IR227	8	8	2 ICLK
0008 70E4h	ICU	Interrupt Request Register 228	IR228	8	8	2 ICLK
0008 70E5h	ICU	Interrupt Request Register 229	IR229	8	8	2 ICLK
0008 70EEh	ICU	Interrupt Request Register 238*2	IR238	8	8	2 ICLK
0008 70EFh	ICU	Interrupt Request Register 239*2	IR239	8	8	2 ICLK
0008 70F0h	ICU	Interrupt Request Register 240*2	IR240	8	8	2 ICLK
0008 70F1h	ICU	Interrupt Request Register 241*2	IR241	8	8	2 ICLK
0008 70F2h	ICU	Interrupt Request Register 242*2	IR242	8	8	2 ICLK
0008 70F3h	ICU	Interrupt Request Register 243*2	IR243	8	8	2 ICLK
0008 70F4h	ICU	Interrupt Request Register 244*2	IR244	8	8	2 ICLK
0008 70F6h	ICU	Interrupt Request Register 246	IR246	8	8	2 ICLK
0008 70F7h	ICU	Interrupt Request Register 247	IR247	8	8	2 ICLK
0008 70F8h	ICU	Interrupt Request Register 248	IR248	8	8	2 ICLK
0008 70F9h	ICU	Interrupt Request Register 249	IR249	8	8	2 ICLK
0008 711Bh	ICU	DTC Transfer Request Enable Register 027	DTCER027	8	8	2 ICLK
0008 711Ch	ICU	DTC Transfer Request Enable Register 028	DTCER028	8	8	2 ICLK
0008 711Dh	ICU	DTC Transfer Request Enable Register 029	DTCER029	8	8	2 ICLK
0008 711Eh	ICU	DTC Transfer Request Enable Register 030	DTCER030	8	8	2 ICLK
0008 711Fh	ICU	DTC Transfer Request Enable Register 031	DTCER031	8	8	2 ICLK
0008 712Dh	ICU	DTC Transfer Request Enable Register 045	DTCER045	8	8	2 ICLK
0008 712Eh	ICU	DTC Transfer Request Enable Register 046	DTCER046	8	8	2 ICLK
0008 7130h	ICU	DTC Transfer Request Enable Register 048*2	DTCER048	8	8	2 ICLK
0008 7131h	ICU	DTC Transfer Request Enable Register 049*2	DTCER049	8	8	2 ICLK
0008 7132h	ICU	DTC Transfer Request Enable Register 050*2	DTCER050	8	8	2 ICLK
0008 7133h	ICU	DTC Transfer Request Enable Register 051*2	DTCER051	8	8	2 ICLK
0008 7135h	ICU	DTC Transfer Request Enable Register 053*2	DTCER053	8	8	2 ICLK
0008 7136h	ICU	DTC Transfer Request Enable Register 054*2	DTCER054	8	8	2 ICLK
0008 7137h	ICU	DTC Transfer Request Enable Register 055*2	DTCER055	8	8	2 ICLK
0008 7138h	ICU	DTC Transfer Request Enable Register 056*2	DTCER056	8	8	2 ICLK
0008 713Bh	ICU	DTC Transfer Request Enable Register 059*2	DTCER059	8	8	2 ICLK
0008 7140h	ICU	DTC Transfer Request Enable Register 064	DTCER064	8	8	2 ICLK
0008 7141h	ICU	DTC Transfer Request Enable Register 065	DTCER065	8	8	2 ICLK
0008 7142h	ICU	DTC Transfer Request Enable Register 066	DTCER066	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (11/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
0008 8006h	CMT0	Compare Match Constant Register	CMCOR	16	16	2 or 3 PCLKB
0008 8008h	CMT1	Compare Match Timer Control Register	CMCR	16	16	2 or 3 PCLKB
0008 800Ah	CMT1	Compare Match Counter	CMCNT	16	16	2 or 3 PCLKB
0008 800Ch	CMT1	Compare Match Constant Register	CMCOR	16	16	2 or 3 PCLKB
0008 8010h	CMT	Compare Match Timer Start Register 1	CMSTR1	16	16	2 or 3 PCLKB
0008 8012h	CMT2	Compare Match Timer Control Register	CMCR	16	16	2 or 3 PCLKB
0008 8014h	CMT2	Compare Match Counter	CMCNT	16	16	2 or 3 PCLKB
0008 8016h	CMT2	Compare Match Constant Register	CMCOR	16	16	2 or 3 PCLKB
0008 8018h	CMT3	Compare Match Timer Control Register	CMCR	16	16	2 or 3 PCLKB
0008 801Ah	CMT3	Compare Match Counter	CMCNT	16	16	2 or 3 PCLKB
0008 801Ch	CMT3	Compare Match Constant Register	CMCOR	16	16	2 or 3 PCLKB
0008 8030h	IWDT	IWDT Refresh Register	IWDTRR	8	8	2 or 3 PCLKB
0008 8032h	IWDT	IWDT Control Register	IWDTCR	16	16	2 or 3 PCLKB
0008 8034h	IWDT	IWDT Status Register	IWDTSR	16	16	2 or 3 PCLKB
0008 8036h	IWDT	IWDT Reset Control Register	IWDTRCR	8	8	2 or 3 PCLKB
0008 8038h	IWDT	IWDT Count Stop Control Register	IWDTCSTPR	8	8	2 or 3 PCLKB
0008 80C0h	DA	D/A Data Register 0	DADR0	16	16	2 or 3 PCLKB
0008 80C2h	DA	D/A Data Register 1*2	DADR1	16	16	2 or 3 PCLKB
0008 80C4h	DA	D/A Control Register	DACR	8	8	2 or 3 PCLKB
0008 80C5h	DA	DADRm Format Select Register	DADPR	8	8	2 or 3 PCLKB
0008 80C6h	DA	D/A A/D Synchronous Start Control Register*2	DAADSCR	8	8	2 or 3 PCLKB
0008 8200h	TMR0	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8201h	TMR1	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8202h	TMR0	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8203h	TMR1	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8204h	TMR0	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB
0008 8205h	TMR1	Time Constant Register A	TCORA	8	8*1	2 or 3 PCLKB
0008 8206h	TMR0	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB
0008 8207h	TMR1	Time Constant Register B	TCORB	8	8*1	2 or 3 PCLKB
0008 8208h	TMR0	Timer Counter	TCNT	8	8	2 or 3 PCLKB
0008 8209h	TMR1	Timer Counter	TCNT	8	8*1	2 or 3 PCLKB
0008 820Ah	TMR0	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB
0008 820Bh	TMR1	Timer Counter Control Register	TCCR	8	8*1	2 or 3 PCLKB
0008 8210h	TMR2	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8211h	TMR3	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8212h	TMR2	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8213h	TMR3	Timer Control/Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8214h	TMR2	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB
0008 8215h	TMR3	Time Constant Register A	TCORA	8	8*1	2 or 3 PCLKB
0008 8216h	TMR2	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB
0008 8217h	TMR3	Time Constant Register B	TCORB	8	8*1	2 or 3 PCLKB
0008 8218h	TMR2	Timer Counter	TCNT	8	8	2 or 3 PCLKB
0008 8219h	TMR3	Timer Counter	TCNT	8	8*1	2 or 3 PCLKB
0008 821Ah	TMR2	Timer Counter Control Register	TCCR	8	8	2 or 3 PCLKB
0008 821Bh	TMR3	Timer Counter Control Register	TCCR	8	8*1	2 or 3 PCLKB
0008 8220h	TMR4	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8221h	TMR5	Timer Control Register	TCR	8	8	2 or 3 PCLKB
0008 8222h	TMR4	Timer Control / Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8223h	TMR5	Timer Control / Status Register	TCSR	8	8	2 or 3 PCLKB
0008 8224h	TMR4	Time Constant Register A	TCORA	8	8	2 or 3 PCLKB
0008 8225h	TMR5	Time Constant Register A	TCORA	8	8*1	2 or 3 PCLKB
0008 8226h	TMR4	Time Constant Register B	TCORB	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (18/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 C09Ah	PORTD	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C09Bh	PORTD	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C09Ch	PORTE	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C09Dh	PORTE	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C0C0h	PORT0	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C1h	PORT1	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C2h	PORT2	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C3h	PORT3	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C4h	PORT4	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C5h	PORT5	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C6h	PORT6	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C7h	PORT7	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C8h	PORT8	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C9h	PORT9	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CAh	PORTA	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CBh	PORTB	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CDh	PORTD	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CEh	PORTE	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0E0h	PORT0	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0E1h	PORT1	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0E2h	PORT2	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0E3h	PORT3	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0E7h	PORT7	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0E8h	PORT8	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0E9h	PORT9	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0EAh	PORTA	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0EBh	PORTB	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0EDh	PORTD	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0EEh	PORTE	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C11Fh	MPC	Write-Protect Register	PWPR	8	8	2 or 3 PCLKB
0008 C140h	MPC	P00 Pin Function Control Register	P00PFS	8	8	2 or 3 PCLKB
0008 C141h	MPC	P01 Pin Function Control Register	P01PFS	8	8	2 or 3 PCLKB
0008 C142h	MPC	P02 Pin Function Control Register	P02PFS	8	8	2 or 3 PCLKB
0008 C148h	MPC	P10 Pin Function Control Register	P10PFS	8	8	2 or 3 PCLKB
0008 C149h	MPC	P11 Pin Function Control Register	P11PFS	8	8	2 or 3 PCLKB
0008 C150h	MPC	P20 Pin Function Control Register	P20PFS	8	8	2 or 3 PCLKB
0008 C151h	MPC	P21 Pin Function Control Register	P21PFS	8	8	2 or 3 PCLKB
0008 C152h	MPC	P22 Pin Function Control Register	P22PFS	8	8	2 or 3 PCLKB
0008 C153h	MPC	P23 Pin Function Control Register	P23PFS	8	8	2 or 3 PCLKB
0008 C154h	MPC	P24 Pin Function Control Register	P24PFS	8	8	2 or 3 PCLKB
0008 C158h	MPC	P30 Pin Function Control Register	P30PFS	8	8	2 or 3 PCLKB
0008 C159h	MPC	P31 Pin Function Control Register	P31PFS	8	8	2 or 3 PCLKB
0008 C15Ah	MPC	P32 Pin Function Control Register	P32PFS	8	8	2 or 3 PCLKB
0008 C15Bh	MPC	P33 Pin Function Control Register	P33PFS	8	8	2 or 3 PCLKB
0008 C160h	MPC	P40 Pin Function Control Register	P40PFS	8	8	2 or 3 PCLKB
0008 C161h	MPC	P41 Pin Function Control Register	P41PFS	8	8	2 or 3 PCLKB
0008 C162h	MPC	P42 Pin Function Control Register	P42PFS	8	8	2 or 3 PCLKB
0008 C163h	MPC	P43 Pin Function Control Register	P43PFS	8	8	2 or 3 PCLKB
0008 C164h	MPC	P44 Pin Function Control Register	P44PFS	8	8	2 or 3 PCLKB
0008 C165h	MPC	P45 Pin Function Control Register	P45PFS	8	8	2 or 3 PCLKB
0008 C166h	MPC	P46 Pin Function Control Register	P46PFS	8	8	2 or 3 PCLKB
0008 C167h	MPC	P47 Pin Function Control Register	P47PFS	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (32/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
000C 1A4Dh	MTU7	Timer Control Register 2	TCR2	8	8	4 or 5 PCLKA
000C 1A50h	MTU6	Timer Synchronous Clear Register	TSYCR	8	8	4 or 5 PCLKA
000C 1A60h	MTU	Timer Waveform Control Register B	TWCRB	8	8	4 or 5 PCLKA
000C 1A70h	MTU	Timer Mode Register 2B	TMDR2B	8	8	4 or 5 PCLKA
000C 1A72h	MTU6	Timer General Register E	TGRE	16	16	4 or 5 PCLKA
000C 1A74h	MTU7	Timer General Register E	TGRE	16	16	4 or 5 PCLKA
000C 1A76h	MTU7	Timer General Register F	TGRF	16	16	4 or 5 PCLKA
000C 1A80h	MTU	Timer Start Register B	TSTRB	8	8, 16	4 or 5 PCLKA
000C 1A81h	MTU	Timer Synchronous Register B	TSYRB	8	8	4 or 5 PCLKA
000C 1A84h	MTU	Timer Read/Write Enable Register B	TRWERB	8	8	4 or 5 PCLKA
000C 1A93h	MTU6	Noise Filter Control Register 6	NFCR6	8	8	4 or 5 PCLKA
000C 1A94h	MTU7	Noise Filter Control Register 7	NFCR7	8	8	4 or 5 PCLKA
000C 1A95h	MTU5	Noise Filter Control Register 5	NFCR5	8	8	4 or 5 PCLKA
000C 1C80h	MTU5	Timer Counter U	TCNTU	16	16, 32	4 or 5 PCLKA
000C 1C82h	MTU5	Timer General Register U	TGRU	16	16	4 or 5 PCLKA
000C 1C84h	MTU5	Timer Control Register U	TCRU	8	8	4 or 5 PCLKA
000C 1C85h	MTU5	Timer Control Register 2U	TCR2U	8	8	4 or 5 PCLKA
000C 1C86h	MTU5	Timer I/O Control Register U	TIORU	8	8	4 or 5 PCLKA
000C 1C90h	MTU5	Timer Counter V	TCNTV	16	16, 32	4 or 5 PCLKA
000C 1C92h	MTU5	Timer General Register V	TGRV	16	16	4 or 5 PCLKA
000C 1C94h	MTU5	Timer Control Register V	TCRV	8	8	4 or 5 PCLKA
000C 1C95h	MTU5	Timer Control Register 2V	TCR2V	8	8	4 or 5 PCLKA
000C 1C96h	MTU5	Timer I/O Control Register V	TIORV	8	8	4 or 5 PCLKA
000C 1CA0h	MTU5	Timer Counter W	TCNTW	16	16, 32	4 or 5 PCLKA
000C 1CA2h	MTU5	Timer General Register W	TGRW	16	16	4 or 5 PCLKA
000C 1CA4h	MTU5	Timer Control Register W	TCRW	8	8	4 or 5 PCLKA
000C 1CA5h	MTU5	Timer Control Register 2W	TCR2W	8	8	4 or 5 PCLKA
000C 1CA6h	MTU5	Timer I/O Control Register W	TIORW	8	8	4 or 5 PCLKA
000C 1CB2h	MTU5	Timer Interrupt Enable Register	TIER	8	8	4 or 5 PCLKA
000C 1CB4h	MTU5	Timer Start Register	TSTR	8	8	4 or 5 PCLKA
000C 1CB6h	MTU5	Timer Compare Match Clear Register	TCNTCMPCLR	8	8	4 or 5 PCLKA
000C 1D30h	MTU	A/D Conversion Start Request Select Register 0	TADSTRGR0	8	8	4 or 5 PCLKA
000C 1D32h	MTU	A/D Conversion Start Request Select Register 1	TADSTRGR1	8	8	4 or 5 PCLKA
000C 2000h	GPT	General PWM Timer Software Start Register*2	GTSTR	16	8, 16, 32	4 or 5 PCLKA
000C 2002h	GPT	Noise Filter Control Register*2	NFCR	16	16, 32	4 or 5 PCLKA
000C 2004h	GPT	General PWM Timer Hardware Source Start/Stop Control Register 0*2	GTHSCR	16	8, 16, 32	4 or 5 PCLKA
000C 2006h	GPT	General PWM Timer Hardware Source Clear Control Register*2	GTHCCR	16	8, 16, 32	4 or 5 PCLKA
000C 2008h	GPT	General PWM Timer Hardware Start Source Select Register*2	GTHSSR	16	8, 16, 32	4 or 5 PCLKA
000C 200Ah	GPT	General PWM Timer Hardware Stop/Clear Source Select Register*2	GTHPSR	16	8, 16, 32	4 or 5 PCLKA
000C 200Ch	GPT	General PWM Timer Write-Protection Register*2	GTWP	16	8, 16, 32	4 or 5 PCLKA
000C 200Eh	GPT	General PWM Timer Sync Register*2	GTSYNC	16	8, 16, 32	4 or 5 PCLKA
000C 2010h	GPT	General PWM Timer External Trigger Input Interrupt Register*2	GTETINT	16	8, 16, 32	4 or 5 PCLKA
000C 2014h	GPT	General PWM Timer Buffer Operation Disable Register*2	GTBDR	16	8, 16, 32	4 or 5 PCLKA
000C 2018h	GPT	General PWM Timer Start Write-Protection Register*2	GTSWP	16	8, 16, 32	4 or 5 PCLKA
000C 201Ch	GPT	General PWM Timer Clearing Write-Protection Register*2	GTCWP	16	8, 16, 32	4 or 5 PCLKA
000C 2020h	GPT	General PWM Timer Common Register Write-Protection Register*2	GTCMNWP	16	8, 16, 32	4 or 5 PCLKA
000C 2024h	GPT	General PWM Timer Mode Register*2	GTMDR	16	8, 16, 32	4 or 5 PCLKA
000C 2028h	GPT	General PWM Timer External Clock Noise Filter Control Register*2	GTECNFCR	32	8, 16, 32	4 or 5 PCLKA

Table 4.1 List of I/O Registers (Address Order) (34/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
000C 21A0h	GPT1	General PWM Timer Period Setting Double Buffer Register*2	GTPDBR	16	16, 32	4 or 5 PCLKA
000C 21A4h	GPT1	A/D Converter Start Request Timing Register A*2	GTADTRA	16	16, 32	4 or 5 PCLKA
000C 21A6h	GPT1	A/D Converter Start Request Timing Buffer Register A*2	GTADTBRA	16	16, 32	4 or 5 PCLKA
000C 21A8h	GPT1	A/D Converter Start Request Timing Double Buffer Register A*2	GTADTDBRA	16	16, 32	4 or 5 PCLKA
000C 21ACh	GPT1	A/D Converter Start Request Timing Register B*2	GTADTRB	16	16, 32	4 or 5 PCLKA
000C 21AEh	GPT1	A/D Converter Start Request Timing Buffer Register B*2	GTADTBRB	16	16, 32	4 or 5 PCLKA
000C 21B0h	GPT1	A/D Converter Start Request Timing Double Buffer Register B*2	GTADTDBRB	16	16, 32	4 or 5 PCLKA
000C 21B4h	GPT1	General PWM Timer Output Negate Control Register*2	GTONCR	16	16, 32	4 or 5 PCLKA
000C 21B6h	GPT1	General PWM Timer Dead Time Control Register*2	GTDTCR	16	16, 32	4 or 5 PCLKA
000C 21B8h	GPT1	General PWM Timer Dead Time Value Register U*2	GTDVU	16	16, 32	4 or 5 PCLKA
000C 21BAh	GPT1	General PWM Timer Dead Time Value Register D*2	GTDVD	16	16, 32	4 or 5 PCLKA
000C 21BCh	GPT1	General PWM Timer Dead Time Buffer Register U*2	GTDBU	16	16, 32	4 or 5 PCLKA
000C 21BEh	GPT1	General PWM Timer Dead Time Buffer Register D*2	GTDBD	16	16, 32	4 or 5 PCLKA
000C 21C0h	GPT1	General PWM Timer Output Protection Function Status Register*2	GTSOS	16	16, 32	4 or 5 PCLKA
000C 21C2h	GPT1	General PWM Timer Output Protection Function Temporary Release Register*2	GTSOTR	16	16, 32	4 or 5 PCLKA
000C 2200h	GPT2	General PWM Timer I/O Control Register*2	GTIOR	16	8, 16, 32	4 or 5 PCLKA
000C 2202h	GPT2	General PWM Timer Interrupt Output Setting Register*2	GTINTAD	16	8, 16, 32	4 or 5 PCLKA
000C 2204h	GPT2	General PWM Timer Control Register*2	GTCR	16	8, 16, 32	4 or 5 PCLKA
000C 2206h	GPT2	General PWM Timer Buffer Enable Register*2	GTBER	16	8, 16, 32	4 or 5 PCLKA
000C 2208h	GPT2	General PWM Timer Count Direction Register*2	GTUDC	16	8, 16, 32	4 or 5 PCLKA
000C 220Ah	GPT2	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register*2	GTITC	16	8, 16, 32	4 or 5 PCLKA
000C 220Ch	GPT2	General PWM Timer Status Register*2	GTST	16	8, 16, 32	4 or 5 PCLKA
000C 220Eh	GPT2	General PWM Timer Counter*2	GTCNT	16	16	4 or 5 PCLKA
000C 2210h	GPT2	General PWM Timer Compare Capture Register A*2	GTCCRA	16	16, 32	4 or 5 PCLKA
000C 2212h	GPT2	General PWM Timer Compare Capture Register B*2	GTCCRB	16	16, 32	4 or 5 PCLKA
000C 2214h	GPT2	General PWM Timer Compare Capture Register C*2	GTCCRC	16	16, 32	4 or 5 PCLKA
000C 2216h	GPT2	General PWM Timer Compare Capture Register D*2	GTCCRD	16	16, 32	4 or 5 PCLKA
000C 2218h	GPT2	General PWM Timer Compare Capture Register E*2	GTCCRE	16	16, 32	4 or 5 PCLKA
000C 221Ah	GPT2	General PWM Timer Compare Capture Register F*2	GTCCRF	16	16, 32	4 or 5 PCLKA
000C 221Ch	GPT2	General PWM Timer Period Setting Register*2	GTPR	16	16, 32	4 or 5 PCLKA
000C 221Eh	GPT2	General PWM Timer Period Setting Buffer Register*2	GTPBR	16	16, 32	4 or 5 PCLKA
000C 2220h	GPT2	General PWM Timer Period Setting Double Buffer Register*2	GTPDBR	16	16, 32	4 or 5 PCLKA
000C 2224h	GPT2	A/D Converter Start Request Timing Register A*2	GTADTRA	16	16, 32	4 or 5 PCLKA
000C 2226h	GPT2	A/D Converter Start Request Timing Buffer Register A*2	GTADTBRA	16	16, 32	4 or 5 PCLKA
000C 2228h	GPT2	A/D Converter Start Request Timing Double Buffer Register A*2	GTADTDBRA	16	16, 32	4 or 5 PCLKA
000C 222Ch	GPT2	A/D Converter Start Request Timing Register B*2	GTADTRB	16	16, 32	4 or 5 PCLKA
000C 222Eh	GPT2	A/D Converter Start Request Timing Buffer Register B*2	GTADTBRB	16	16, 32	4 or 5 PCLKA
000C 2230h	GPT2	A/D Converter Start Request Timing Double Buffer Register B*2	GTADTDBRB	16	16, 32	4 or 5 PCLKA
000C 2234h	GPT2	General PWM Timer Output Negate Control Register*2	GTONCR	16	16, 32	4 or 5 PCLKA
000C 2236h	GPT2	General PWM Timer Dead Time Control Register*2	GTDTCR	16	16, 32	4 or 5 PCLKA
000C 2238h	GPT2	General PWM Timer Dead Time Value Register U*2	GTDVU	16	16, 32	4 or 5 PCLKA
000C 223Ah	GPT2	General PWM Timer Dead Time Value Register D*2	GTDVD	16	16, 32	4 or 5 PCLKA
000C 223Ch	GPT2	General PWM Timer Dead Time Buffer Register U*2	GTDBU	16	16, 32	4 or 5 PCLKA
000C 223Eh	GPT2	General PWM Timer Dead Time Buffer Register D*2	GTDBD	16	16, 32	4 or 5 PCLKA
000C 2240h	GPT2	General PWM Timer Output Protection Function Status Register*2	GTSOS	16	16, 32	4 or 5 PCLKA
000C 2242h	GPT2	General PWM Timer Output Protection Function Temporary Release Register*2	GTSOTR	16	16, 32	4 or 5 PCLKA

Table 4.1 List of I/O Registers (Address Order) (35/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
000C 2280h	GPT3	General PWM Timer I/O Control Register*2	GTIOR	16	8, 16, 32	4 or 5 PCLKA
000C 2282h	GPT3	General PWM Timer Interrupt Output Setting Register*2	GTINTAD	16	8, 16, 32	4 or 5 PCLKA
000C 2284h	GPT3	General PWM Timer Control Register*2	GTCR	16	8, 16, 32	4 or 5 PCLKA
000C 2286h	GPT3	General PWM Timer Buffer Enable Register*2	GTBER	16	8, 16, 32	4 or 5 PCLKA
000C 2288h	GPT3	General PWM Timer Count Direction Register*2	GTUDC	16	8, 16, 32	4 or 5 PCLKA
000C 228Ah	GPT3	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register*2	GTITC	16	8, 16, 32	4 or 5 PCLKA
000C 228Ch	GPT3	General PWM Timer Status Register*2	GTST	16	8, 16, 32	4 or 5 PCLKA
000C 228Eh	GPT3	General PWM Timer Counter*2	GTCNT	16	16	4 or 5 PCLKA
000C 2290h	GPT3	General PWM Timer Compare Capture Register A*2	GTCCRA	16	16, 32	4 or 5 PCLKA
000C 2292h	GPT3	General PWM Timer Compare Capture Register B*2	GTCCRB	16	16, 32	4 or 5 PCLKA
000C 2294h	GPT3	General PWM Timer Compare Capture Register C*2	GTCCRC	16	16, 32	4 or 5 PCLKA
000C 2296h	GPT3	General PWM Timer Compare Capture Register D*2	GTCCRD	16	16, 32	4 or 5 PCLKA
000C 2298h	GPT3	General PWM Timer Compare Capture Register E*2	GTCCRE	16	16, 32	4 or 5 PCLKA
000C 229Ah	GPT3	General PWM Timer Compare Capture Register F*2	GTCCRF	16	16, 32	4 or 5 PCLKA
000C 229Ch	GPT3	General PWM Timer Period Setting Register*2	GTPR	16	16, 32	4 or 5 PCLKA
000C 229Eh	GPT3	General PWM Timer Period Setting Buffer Register*2	GTPBR	16	16, 32	4 or 5 PCLKA
000C 22A0h	GPT3	General PWM Timer Period Setting Double Buffer Register*2	GTPDBR	16	16, 32	4 or 5 PCLKA
000C 22A4h	GPT3	A/D Converter Start Request Timing Register A*2	GTADTRA	16	16, 32	4 or 5 PCLKA
000C 22A6h	GPT3	A/D Converter Start Request Timing Buffer Register A*2	GTADTBRA	16	16, 32	4 or 5 PCLKA
000C 22A8h	GPT3	A/D Converter Start Request Timing Double Buffer Register A*2	GTADTDBRA	16	16, 32	4 or 5 PCLKA
000C 22ACh	GPT3	A/D Converter Start Request Timing Register B*2	GTADTRB	16	16, 32	4 or 5 PCLKA
000C 22AEh	GPT3	A/D Converter Start Request Timing Buffer Register B*2	GTADTBRB	16	16, 32	4 or 5 PCLKA
000C 22B0h	GPT3	A/D Converter Start Request Timing Double Buffer Register B*2	GTADTDBRB	16	16, 32	4 or 5 PCLKA
000C 22B4h	GPT3	General PWM Timer Output Negate Control Register*2	GTONCR	16	16, 32	4 or 5 PCLKA
000C 22B6h	GPT3	General PWM Timer Dead Time Control Register*2	GTDTCR	16	16, 32	4 or 5 PCLKA
000C 22B8h	GPT3	General PWM Timer Dead Time Value Register U*2	GTDVU	16	16, 32	4 or 5 PCLKA
000C 22BAh	GPT3	General PWM Timer Dead Time Value Register D*2	GTDVD	16	16, 32	4 or 5 PCLKA
000C 22BCh	GPT3	General PWM Timer Dead Time Buffer Register U*2	GTDBU	16	16, 32	4 or 5 PCLKA
000C 22BEh	GPT3	General PWM Timer Dead Time Buffer Register D*2	GTDBD	16	16, 32	4 or 5 PCLKA
000C 22C0h	GPT3	General PWM Timer Output Protection Function Status Register*2	GTSOS	16	16, 32	4 or 5 PCLKA
000C 22C2h	GPT3	General PWM Timer Output Protection Function Temporary Release Register*2	GTSOTR	16	16, 32	4 or 5 PCLKA
000C 2300h	GPT01	General PWM Timer Longword Counter*2	GTCNTLW	32	32	4 or 5 PCLKA
000C 2304h	GPT01	General PWM Timer Longword Compare Capture Register A*2	GTCCRALW	32	32	4 or 5 PCLKA
000C 2308h	GPT01	General PWM Timer Longword Compare Capture Register B*2	GTCCRBLW	32	32	4 or 5 PCLKA
000C 230Ch	GPT01	General PWM Timer Longword Compare Capture Register C*2	GTCCRCLW	32	32	4 or 5 PCLKA
000C 2310h	GPT01	General PWM Timer Longword Compare Capture Register D*2	GTCCRDLW	32	32	4 or 5 PCLKA
000C 2314h	GPT01	General PWM Timer Longword Compare Capture Register E*2	GTCCRELW	32	32	4 or 5 PCLKA
000C 2318h	GPT01	General PWM Timer Longword Compare Capture Register F*2	GTCCRFLW	32	32	4 or 5 PCLKA
000C 231Ch	GPT01	General PWM Timer Longword Period Setting Register*2	GTPRLW	32	32	4 or 5 PCLKA
000C 2320h	GPT01	General PWM Timer Longword Period Setting Buffer Register*2	GTPBRLW	32	32	4 or 5 PCLKA
000C 2324h	GPT01	General PWM Timer Longword Period Setting Double Buffer Register*2	GTPDBRLW	32	32	4 or 5 PCLKA
000C 2328h	GPT01	Longword A/D Converter Start Request Timing Register A*2	GTADTRALW	32	32	4 or 5 PCLKA
000C 232Ch	GPT01	Longword A/D Converter Start Request Timing Buffer Register A*2	GTADTBRALW	32	32	4 or 5 PCLKA

Table 5.16 Clock Timing

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time	t_{Xcyc}	50	—	—	ns	Figure 5.22
EXTAL external clock input high pulse width	t_{XH}	20	—	—	ns	
EXTAL external clock input low pulse width	t_{XL}	20	—	—	ns	
EXTAL external clock rise time	t_{Xr}	—	—	5	ns	
EXTAL external clock fall time	t_{Xf}	—	—	5	ns	
EXTAL external clock input wait time*1	t_{XWT}	0.5	—	—	μs	
Main clock oscillator oscillation frequency	f_{MAIN}	1	—	20	MHz	
Main clock oscillation stabilization time (crystal)*2	$t_{MAINOSC}$	—	3	—	ms	Figure 5.23
Main clock oscillation stabilization time (ceramic resonator)*2	$t_{MAINOSC}$	—	50	—	μs	
LOCO clock oscillation frequency	f_{LOCO}	3.44	4.0	4.56	MHz	
LOCO clock oscillation stabilization time	t_{LOCO}	—	—	0.5	μs	Figure 5.24
HOCO clock oscillation frequency	f_{HOCO} (32MHz)	31.52	32	32.48	MHz	T_a = –40 to –20°C
		31.68	32	32.32	MHz	T_a = –20 to +75°C
		31.52	32	32.48	MHz	T_a = +75 to +85°C
	f_{HOCO} (64MHz)	63.04	64	64.96	MHz	T_a = –40 to –20°C
		63.36	64	64.64	MHz	T_a = –20 to +75°C
		63.04	64	64.96	MHz	T_a = +75 to +85°C
HOCO clock oscillation stabilization time	t_{HOCO} (32MHz)	—	—	37.1	μs	Figure 5.26
	t_{HOCO} (64MHz)	—	—	80.6	μs	Figure 5.26
IWDT-dedicated clock oscillation frequency	f_{ILOCO}	12.75	15	17.25	kHz	
IWDT-dedicated clock oscillation stabilization time	t_{ILOCO}	—	—	50	μs	Figure 5.27
PLL circuit oscillation frequency	f_{PLL}	40	—	80	MHz	
PLL clock oscillation stabilization time	t_{PLL}	—	—	50	μs	Figure 5.28
PLL free-running oscillation frequency	f_{PLLFR}	—	8	—	MHz	

Note 1. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating) when the external clock is stable.

Note 2. Reference values when an 8-MHz resonator is used.
When specifying the main clock oscillator stabilization time, set the MOSCWTCR register with a stabilization time value that is equal to or greater than the resonator-manufacturer-recommended value.
After changing the setting of the MOSCCR.MOSTP bit so that the main clock oscillator operates, read the OSCOVFSR.MOOVF flag to confirm that is has become 1, and then start using the main clock.

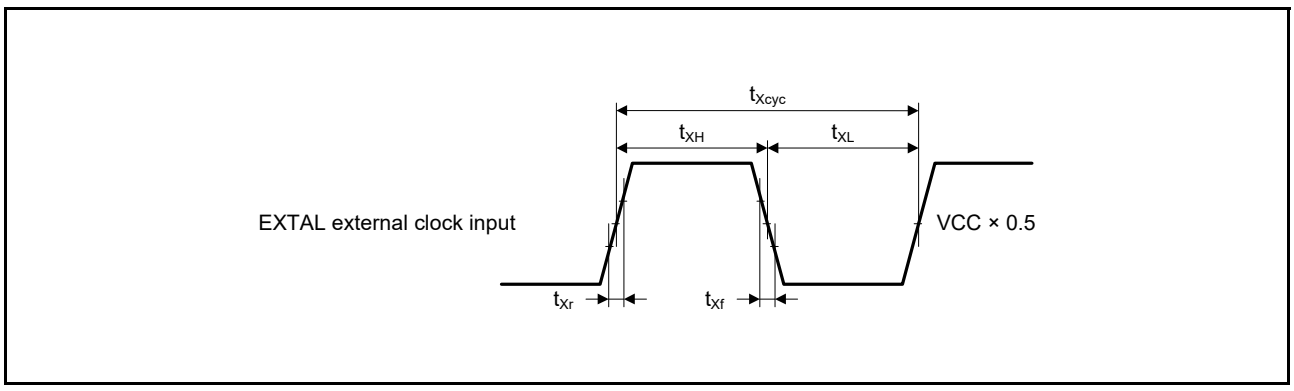


Figure 5.22 EXTAL External Clock Input Timing

5.3.4 Control Signal Timing

Table 5.22 Control Signal Timing

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled (NMIFLTE.NFLTEN = 0)	$t_{Pcyc} \times 2 \le 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		NMI digital filter enabled (NMIFLTE.NFLTEN = 1)	$t_{NMICK} \times 3 \le 200$ ns
		$t_{NMICK} \times 3.5$*2	—	—			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled (IRQFLTE0.FLTENi = 0)	$t_{Pcyc} \times 2 \le 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		IRQ digital filter enabled (IRQFLTE0.FLTENi = 1)	$t_{IRQCK} \times 3 \le 200$ ns
		$t_{IRQCK} \times 3.5$*3	—	—			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in software standby mode.
Note 1. t_{Pcyc} indicates the cycle of PCLKB.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

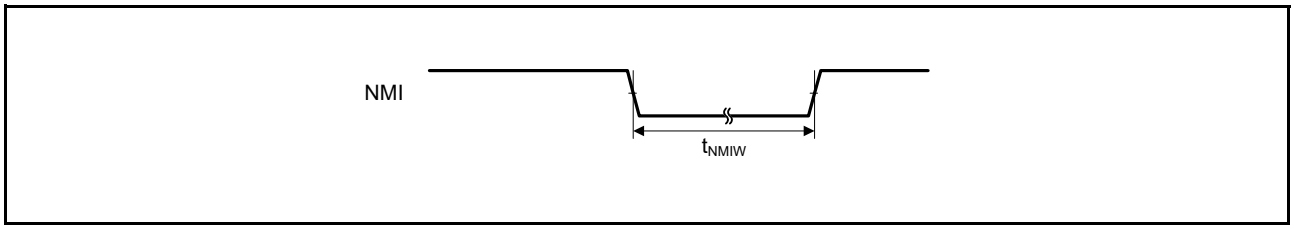


Figure 5.34 NMI Interrupt Input Timing

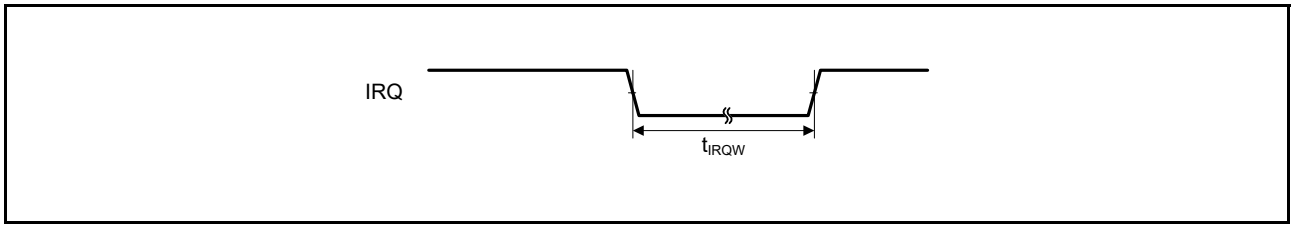


Figure 5.35 IRQ Interrupt Input Timing

Table 5.24 Timing of On-Chip Peripheral Modules (2)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 =AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C, C = 30pF

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc}	Figure 5.47
		Slave			6	—		
	RSPCK clock high pulse width	Master	VCC = 4.0 V or above	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 5$	—	ns	
			VCC = 2.7 V or above		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 8$	—		
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width	Master	VCC = 4.0 V or above	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 5$	—	ns	
			VCC = 2.7 V or above		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 8$	—		
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/fall time	Output	VCC = 4.0 V or above	t_{SPCKr}, t_{SPCKf}	—	6	ns	
			VCC = 2.7 V or above		—	10		
		Input			—	0.1	μs/V	
	Data input setup time	Master	VCC = 4.0 V or above	t_{SU}	10	—	ns	Figure 5.48 to Figure 5.51
			VCC = 2.7 V or above		26	—		
		Slave			20	—		
	Data input hold time	Master	RSPCK set to a division ratio other than PCLKB divided by 2	t_H	t_{Pcyc}	—	ns	
			RSPCK set to PCLKB divided by 2	t_{HF}	0	—		
		Slave		t_H	0	—		
	SSL setup time	Master		t_{LEAD}	–30 + N*2 × t_{SPcyc}	—	ns	
		Slave			6	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	–30 + N*3 × t_{SPcyc}	—	ns	
		Slave			6	—	t_{Pcyc}	
	Data output delay time	Master	VCC = 4.0 V or above	t_{OD}	—	10	ns	
			VCC = 2.7 V or above		—	14		
		Slave			—	65		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$6 \times t_{Pcyc}$	—		
	MOSI and MISO rise/fall time	Output		t_{Dr}, t_{Df}	—	10	ns	
		Input			—	1	μs	
	SSL rise/fall time	Output		t_{SSLr}, t_{SSLf}	—	10	ns	
		Input			—	1	μs	
	Slave access time			t_{SA}	—	6	t_{Pcyc}	Figure 5.50, Figure 5.51
	Slave output release time			t_{REL}	—	5	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle
Note 2. N: An integer from 1 to 8 that can be set by the RSPI clock delay register (SPCKD)
Note 3. N: An integer from 1 to 8 that can be set by the RSPI slave select negation delay register (SSLND)

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

5.11 E2 DataFlash Characteristics

Table 5.42 E2 DataFlash Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Reprogramming/erasure cycle*1		N_{DPEC}	100000	1000000	—	Times	
Data hold time	After 10000 times of N_{DPEC}	t_{DDRP}	20*2, *3	—	—	Year	T_a = +85°C
	After 100000 times of N_{DPEC}		5*2, *3	—	—	Year	
	After 1000000 times of N_{DPEC}		—	1*2, *3	—	Year	T_a = +25°C

Note 1. Definition of reprogram/erase cycle: The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 1-byte programming is performed 1000 times for different addresses in 1-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. Characteristic when using the flash memory programmer and the self-programming library provided from Renesas Electronics.
Note 3. This result is obtained from reliability testing.

Table 5.43 E2 DataFlash Characteristics (2): High-Speed Operating Mode

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V,
Temperature range for the programming/erasure operation: T_a = –40 to +85°C

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1-byte	t_{Dp1}	—	95.0	797.0	—	40.8	375.5	µs
Erasure time	1-Kbyte	t_{DE1K}	—	19.5	498.5	—	6.2	229.4	ms
	8-Kbyte	t_{DE8K}	—	119.8	2555.7	—	12.9	367.2	ms
Blank check time	1-byte	t_{DBC1}	—	—	55.0	—	—	16.1	µs
	1-Kbyte	t_{DBC1K}	—	—	7216.0	—	—	495.7	µs
Erase operation forcible stop time		t_{DSED}	—	—	16.0	—	—	10.7	µs
Data flash-module stop release time		t_{DSTOP}	5.0	—	—	5.0	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK should be ±3.5%.

Table 5.44 E2 DataFlash Characteristics (3): Middle-Speed Operating Mode

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V,
Temperature range for the programming/erasure operation: T_a = –40 to +85°C

Item		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1-byte	t_{Dp1}	—	135.0	1197.0	—	86.5	822.5	µs
Erasure time	1-Kbyte	t_{DE1K}	—	19.6	500.1	—	8.0	264.1	ms
	8-Kbyte	t_{DE8K}	—	119.9	2557.4	—	27.7	668.2	ms
Blank check time	1-byte	t_{DBC1}	—	—	85.0	—	—	50.9	µs
	1-Kbyte	t_{DBC1K}	—	—	7246.0	—	—	1457.5	µs
Erase operation forcible stop time		t_{DSED}	—	—	28.0	—	—	21.3	µs
Data flash-module stop release time		t_{DSTOP}	0.72	—	—	0.72	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK should be ±3.5%.

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.