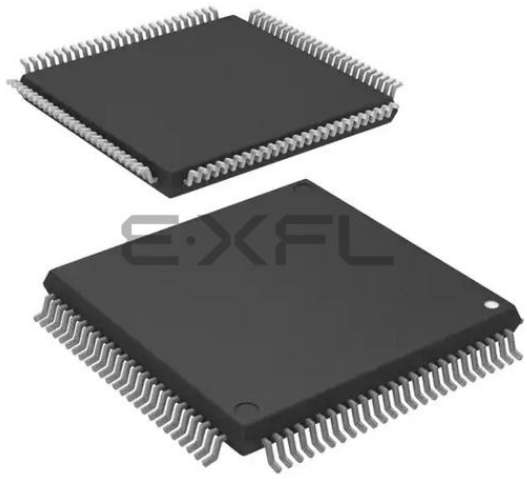
Renesas Electronics America Inc - R5F524TAADFP#31 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

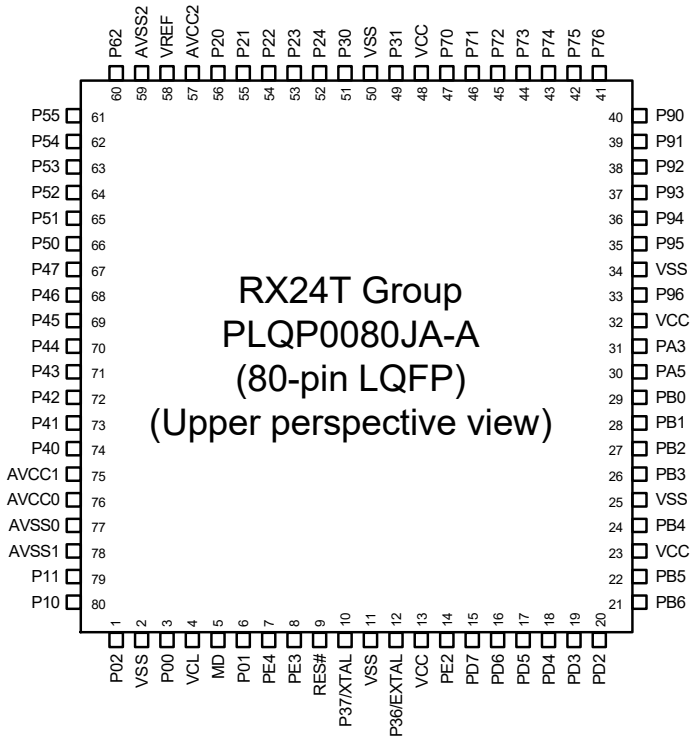
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	80
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 22x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f524taadfp-31

Table 1.4 Pin Functions (4/4)

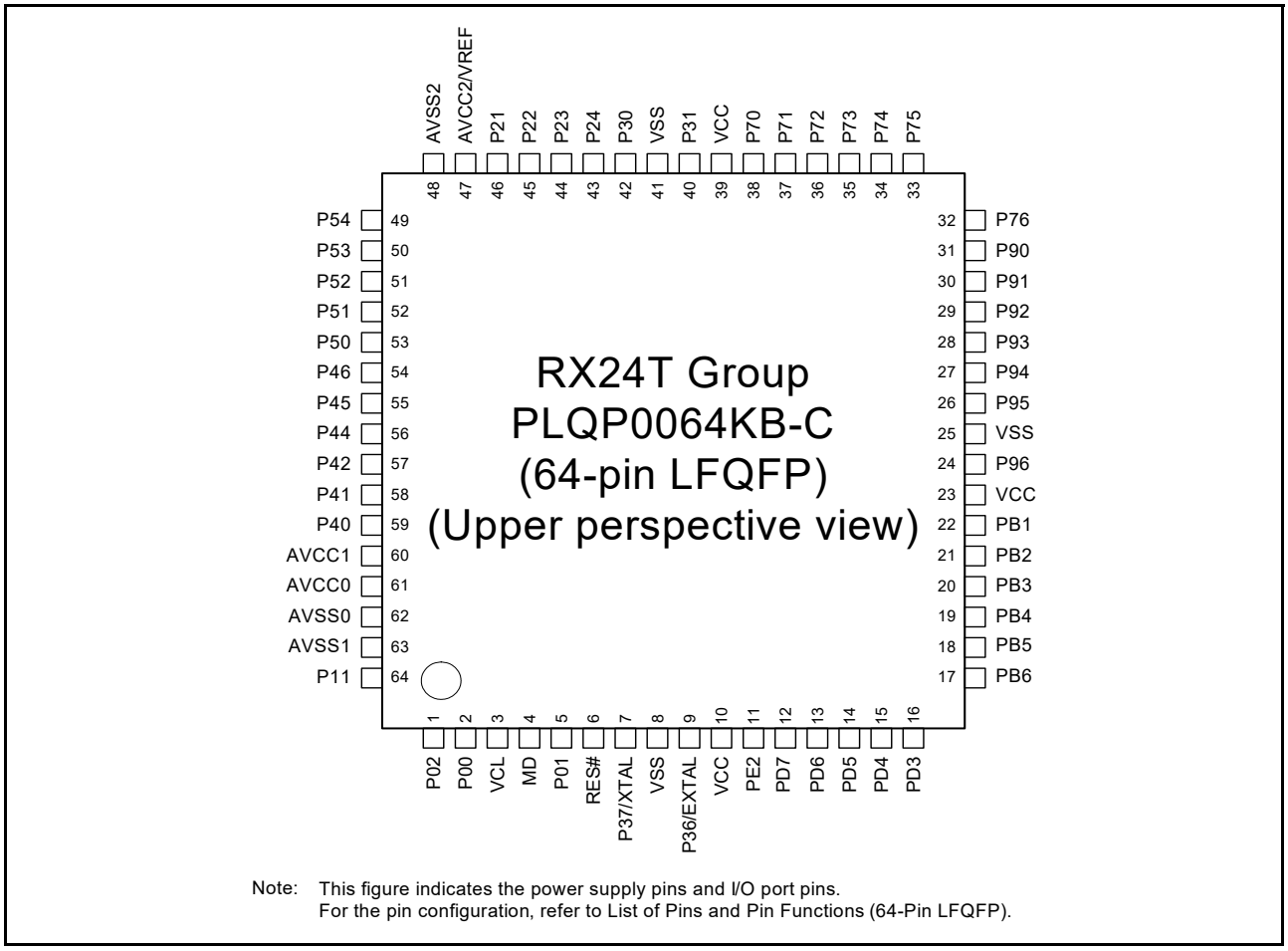
Classifications	Pin Name	I/O	Description
I/O ports	P00 to P02	I/O	3-bit input/output pins.
	P10, P11	I/O	2-bit input/output pins.
	P20 to P24	I/O	5-bit input/output pins.
	P30 to P33, P36, P37	I/O	6-bit input/output pins.
	P40 to P47	I/O	8-bit input/output pins.
	P50 to P55	I/O	6-bit input/output pins.
	P60 to P65	I/O	6-bit input/output pins.
	P70 to P76	I/O	7-bit input/output pins.
	P80 to P82	I/O	3-bit input/output pins.
	P90 to P96	I/O	7-bit input/output pins.
	PA0 to PA5	I/O	6-bit input/output pins.
	PB0 to PB7	I/O	8-bit input/output pins.
	PD0 to PD7	I/O	8-bit input/output pins.
	PE0 to PE5	I/O	6-bit input/output pins (PE2: input).

Note: When the A/D converter, D/A converter, and comparator C are not used, connect the AVCC0, AVCC1, AVCC2, and VREF pins to VCC, and connect the AVSS0, AVSS1 and AVSS2 pins to VSS, respectively.



Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, refer to List of Pins and Pin Functions (80-Pin LQFP/LFQFP).

Figure 1.4 Pin Assignments of the 80-Pin LQFP



Note: This figure indicates the power supply pins and I/O port pins.
For the pin configuration, refer to List of Pins and Pin Functions (64-Pin LFQFP).

Figure 1.6 Pin Assignments of the 64-Pin LFQFP

Table 1.5 List of Pins and Pin Functions (100-Pin LFQFP, Chip Version B) (3/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (TMR, MTU, POE, CAC, GPT)	Communications (SCI, RSPI, RIIC, RSCAN)	Others
94	AVSS0				
95	AVSS1				
96		P82	MTIC5U, MTIC5U#, TMO4	SCK6	
97		P81	MTIC5V, MTIC5V#, TMCI4	TXD6, SMOSI6, SSDA6	
98		P80	MTIC5W, MTIC5W#, TMRI4	RXD6, SMISO6, SSCL6	
99		P11	MTIOC3A, MTIOC3A#, MTCLKC, MTCLKC#, TMO3		IRQ1
100		P10	MTIOC9B, MTIOC9B#, MTCLKD, MTCLKD#, TMRI3, POE12#	CTS6#, RTS6#, SS6#	IRQ0

Table 1.6 List of Pins and Pin Functions (100-Pin LFQFP, Chip Version A) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE, CAC)	Communications (SCI, RSPI, RIIC)	Others
55		P72	MTIOC4A		
56		P71	MTIOC3B		
57		P70	POE0#		IRQ5
58		P33	MTIOC3A, MTCLKA, TMO0	SSLA3	
59		P32	MTIOC3C, MTCLKB, TMO6	SSLA2	
60	VCC				
61		P31	MTIOC0A, MTCLKC, TMRI6	SSLA1	IRQ6
62	VSS				
63		P30	MTIOC0B, MTCLKD, TMCI6	SSLA0	IRQ7, COMP3
64		P24	MTIC5U, TMCI2, TMO6	RSPCKA	COMP0
65		P23	MTIC5V, TMO2, CACREF	MOSIA	COMP1
66		P22	MTIC5W, TMRI2, TMO4	MISOA	ADTRG2#, COMP2
67		P21	MTCLKA, MTIOC9A, TMCI4		IRQ6, ADTRG1#, AN116, CVREFC1
68		P20	MTCLKB, MTIOC9C, TMRI4		IRQ7, ADTRG0#, AN016, CVREFC0
69		P65			AN205
70		P64			AN204
71	AVCC2				
72	VREF				
73	AVSS2				
74		P63			AN203, IRQ7
75		P62			AN202, IRQ6
76		P61			AN201, IRQ5
77		P60			AN200, IRQ4
78		P55			AN211, IRQ3
79		P54			AN210, IRQ2
80		P53			AN209, IRQ1
81		P52			AN208, IRQ0
82		P51			AN207
83		P50			AN206
84		P47			AN103
85		P46			AN102, CMPC12, CMPC13, CMPC30, CMPC31
86		P45			AN101, CMPC02, CMPC03, CMPC20, CMPC21
87		P44			AN100, CMPC10, CMPC11, CMPC32, CMPC33
88		P43			AN003
89		P42			AN002
90		P41			AN001
91		P40			AN000, CMPC00, CMPC01, CMPC22, CMPC23
92	AVCC1				
93	AVCC0				
94	AVSS0				
95	AVSS1				
96		P82	MTIC5U, TMO4	SCK6	
97		P81	MTIC5V, TMCI4	TXD6, SMOSI6, SSDA6	
98		P80	MTIC5W, TMRI4	RXD6, SMISO6, SSCL6	
99		P11	MTIOC3A, MTCLKC, TMO3		IRQ1
100		P10	MTIOC9B, MTCLKD, TMRI3, POE12#	CTS6#, RTS6#, SS6#	IRQ0

Table 1.8 List of Pins and Pin Functions (64-Pin LFQFP) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE, CAC)	Communications (SCI, RSPI, RIIC)	Others
1		P02	MTIOC9D	CTS1#, RTS1#, SS1#	IRQ5, ADST0
2		P00			IRQ2, ADST1
3	VCL				
4	MD				FINED
5		P01	POE12#		IRQ4, ADST2
6	RES#				
7	XTAL	P37			
8	VSS				
9	EXTAL	P36			
10	VCC				
11		PE2	POE10#		NMI
12		PD7	MTIOC9A, TMRI1, TMRI5	SSLA1	
13		PD6	MTIOC9C, TMO1	CTS1#, RTS1#, SS1#	
14		PD5	TMRI0, TMRI6	RXD1, SMISO1, SSCL1	
15		PD4	TMCI0, TMCI6	SCK1	IRQ2
16		PD3	TMO0	TXD1, SMOSI1, SSDA1	
17		PB6		RXD5, SMISO5, SSCL5	IRQ5
18		PB5		TXD5, SMOSI5, SSDA5	
19		PB4	POE8#	CTS5#, RTS5#, SS5#	IRQ3
20		PB3	MTIOC0A, CACREF	SCK6, RSPCKA	
21		PB2	MTIOC0B, TMRI0, ADSM0	TXD6, SMOSI6, SSDA6, SDA0	
22		PB1	MTIOC0C, TMCI0, ADSM1	RXD6, SMISO6, SSCL6, SCL0	
23	VCC				
24		P96	POE4#		IRQ4
25	VSS				
26		P95	MTIOC6B		
27		P94	MTIOC7A		
28		P93	MTIOC7B		
29		P92	MTIOC6D		
30		P91	MTIOC7C		
31		P90	MTIOC7D		
32		P76	MTIOC4D		
33		P75	MTIOC4C		
34		P74	MTIOC3D		
35		P73	MTIOC4B		
36		P72	MTIOC4A		
37		P71	MTIOC3B		
38		P70	POE0#		IRQ5
39	VCC				
40		P31	MTIOC0A, MTCLKC, TMRI6	SSLA1	IRQ6
41	VSS				
42		P30	MTIOC0B, MTCLKD, TMCI6	SSLA0	IRQ7, COMP3
43		P24	MTIC5U, TMCI2, TMO6	RSPCKA	COMP0
44		P23	MTIC5V, TMO2, CACREF	MOSIA	COMP1
45		P22	MTIC5W, TMRI2, TMO4	MISOA	ADTRG2#, COMP2
46		P21	MTCLKA, MTIOC9A, TMCI4		IRQ6, ADTRG1#, AN116, CVREFC1
47	AVCC2/VREF				
48	AVSS2				
49		P54			AN210, IRQ2
50		P53			AN209, IRQ1
51		P52			AN208, IRQ0
52		P51			AN207
53		P50			AN206

3. Address Space

3.1 Address Space

This MCU has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.
Figure 3.1 shows the memory maps.

Table 4.1 List of I/O Registers (Address Order) (4/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 708Fh	ICU	Interrupt Request Register 143	IR143	8	8	2 ICLK
0008 7090h	ICU	Interrupt Request Register 144	IR144	8	8	2 ICLK
0008 7091h	ICU	Interrupt Request Register 145	IR145	8	8	2 ICLK
0008 7092h	ICU	Interrupt Request Register 146	IR146	8	8	2 ICLK
0008 7095h	ICU	Interrupt Request Register 149	IR149	8	8	2 ICLK
0008 7096h	ICU	Interrupt Request Register 150	IR150	8	8	2 ICLK
0008 7097h	ICU	Interrupt Request Register 151	IR151	8	8	2 ICLK
0008 7098h	ICU	Interrupt Request Register 152	IR152	8	8	2 ICLK
0008 7099h	ICU	Interrupt Request Register 153	IR153	8	8	2 ICLK
0008 709Fh	ICU	Interrupt Request Register 159	IR159	8	8	2 ICLK
0008 70A0h	ICU	Interrupt Request Register 160	IR160	8	8	2 ICLK
0008 70A1h	ICU	Interrupt Request Register 161	IR161	8	8	2 ICLK
0008 70A2h	ICU	Interrupt Request Register 162	IR162	8	8	2 ICLK
0008 70A3h	ICU	Interrupt Request Register 163	IR163	8	8	2 ICLK
0008 70A4h	ICU	Interrupt Request Register 164	IR164	8	8	2 ICLK
0008 70A5h	ICU	Interrupt Request Register 165	IR165	8	8	2 ICLK
0008 70A8h	ICU	Interrupt Request Register 168	IR168	8	8	2 ICLK
0008 70A9h	ICU	Interrupt Request Register 169	IR169	8	8	2 ICLK
0008 70AAh	ICU	Interrupt Request Register 170	IR170	8	8	2 ICLK
0008 70ABh	ICU	Interrupt Request Register 171	IR171	8	8	2 ICLK
0008 70ACh	ICU	Interrupt Request Register 172	IR172	8	8	2 ICLK
0008 70ADh	ICU	Interrupt Request Register 173	IR173	8	8	2 ICLK
0008 70AEh	ICU	Interrupt Request Register 174	IR174	8	8	2 ICLK
0008 70AFh	ICU	Interrupt Request Register 175	IR175	8	8	2 ICLK
0008 70B0h	ICU	Interrupt Request Register 176	IR176	8	8	2 ICLK
0008 70B1h	ICU	Interrupt Request Register 177	IR177	8	8	2 ICLK
0008 70B2h	ICU	Interrupt Request Register 178	IR178	8	8	2 ICLK
0008 70B3h	ICU	Interrupt Request Register 179	IR179	8	8	2 ICLK
0008 70B4h	ICU	Interrupt Request Register 180	IR180	8	8	2 ICLK
0008 70B5h	ICU	Interrupt Request Register 181	IR181	8	8	2 ICLK
0008 70B6h	ICU	Interrupt Request Register 182	IR182	8	8	2 ICLK
0008 70B7h	ICU	Interrupt Request Register 183	IR183	8	8	2 ICLK
0008 70B8h	ICU	Interrupt Request Register 184	IR184	8	8	2 ICLK
0008 70B9h	ICU	Interrupt Request Register 185	IR185	8	8	2 ICLK
0008 70BAh	ICU	Interrupt Request Register 186	IR186	8	8	2 ICLK
0008 70BBh	ICU	Interrupt Request Register 187	IR187	8	8	2 ICLK
0008 70BCh	ICU	Interrupt Request Register 188	IR188	8	8	2 ICLK
0008 70BDh	ICU	Interrupt Request Register 189	IR189	8	8	2 ICLK
0008 70BEh	ICU	Interrupt Request Register 190	IR190	8	8	2 ICLK
0008 70BFh	ICU	Interrupt Request Register 191	IR191	8	8	2 ICLK
0008 70C0h	ICU	Interrupt Request Register 192	IR192	8	8	2 ICLK
0008 70C1h	ICU	Interrupt Request Register 193	IR193	8	8	2 ICLK
0008 70C2h	ICU	Interrupt Request Register 194	IR194	8	8	2 ICLK
0008 70C3h	ICU	Interrupt Request Register 195	IR195	8	8	2 ICLK
0008 70C4h	ICU	Interrupt Request Register 196	IR196	8	8	2 ICLK
0008 70C5h	ICU	Interrupt Request Register 197	IR197	8	8	2 ICLK
0008 70CAh	ICU	Interrupt Request Register 202*2	IR202	8	8	2 ICLK
0008 70CBh	ICU	Interrupt Request Register 203*2	IR203	8	8	2 ICLK
0008 70CCh	ICU	Interrupt Request Register 204*2	IR204	8	8	2 ICLK
0008 70CDh	ICU	Interrupt Request Register 205*2	IR205	8	8	2 ICLK
0008 70CEh	ICU	Interrupt Request Register 206*2	IR206	8	8	2 ICLK
0008 70CFh	ICU	Interrupt Request Register 207*2	IR207	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (14/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 9214h	S12AD1	A/D Channel Select Register B0	ADANSB0	16	16	2 or 3 PCLKB
0008 9216h	S12AD1	A/D Channel Select Register B1	ADANSB1	16	16	2 or 3 PCLKB
0008 9218h	S12AD1	A/D Data Duplication Register	ADDBLDR	16	16	2 or 3 PCLKB
0008 921Eh	S12AD1	A/D Self-Diagnosis Data Register	ADRD	16	16	2 or 3 PCLKB
0008 9220h	S12AD1	A/D Data Register 0	ADDR0	16	16	2 or 3 PCLKB
0008 9222h	S12AD1	A/D Data Register 1	ADDR1	16	16	2 or 3 PCLKB
0008 9224h	S12AD1	A/D Data Register 2	ADDR2	16	16	2 or 3 PCLKB
0008 9226h	S12AD1	A/D Data Register 3	ADDR3	16	16	2 or 3 PCLKB
0008 9240h	S12AD1	A/D Data Register 16	ADDR16	16	16	2 or 3 PCLKB
0008 9266h	S12AD1	A/D Sample-and-hold Circuit Control Register	ADSHCR	16	16	2 or 3 PCLKB
0008 927Ah	S12AD1	A/D Disconnection Detection Control Register	ADDISCR	8	8	2 or 3 PCLKB
0008 9280h	S12AD1	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2 or 3 PCLKB
0008 9284h	S12AD1	A/D Data Duplication Register A	ADDBLDRA	16	16	2 or 3 PCLKB
0008 9286h	S12AD1	A/D Data Duplication Register B	ADDBLDRB	16	16	2 or 3 PCLKB
0008 92D4h	S12AD1	A/D Channel Select Register C0	ADANSC0	16	16	2 or 3 PCLKB
0008 92D6h	S12AD1	A/D Channel Select Register C1	ADANSC1	16	16	2 or 3 PCLKB
0008 92D9h	S12AD1	A/D Group C Trigger Select Register	ADGCTRGR	8	8	2 or 3 PCLKB
0008 92DDh	S12AD1	A/D Sampling State Register L	ADSSTRL	8	8	2 or 3 PCLKB
0008 92E0h	S12AD1	A/D Sampling State Register 0	ADSSTR0	8	8	2 or 3 PCLKB
0008 92E1h	S12AD1	A/D Sampling State Register 1	ADSSTR1	8	8	2 or 3 PCLKB
0008 92E2h	S12AD1	A/D Sampling State Register 2	ADSSTR2	8	8	2 or 3 PCLKB
0008 92E3h	S12AD1	A/D Sampling State Register 3	ADSSTR3	8	8	2 or 3 PCLKB
0008 93A0h	S12AD1	A/D Programmable Gain Amplifier Control Register	ADPGACR	16	16	2 or 3 PCLKB
0008 93A2h	S12AD1	A/D Programmable Gain Amplifier Gain Setting Register 0	ADPGAGS0	16	16	2 or 3 PCLKB
0008 9400h	S12AD2	A/D Control Register	ADCSR	16	16	2 or 3 PCLKB
0008 9404h	S12AD2	A/D Channel Select Register A0	ADANSA0	16	16	2 or 3 PCLKB
0008 9408h	S12AD2	A/D-Converted Value Addition/Average Function Channel Select Register 0	ADADS0	16	16	2 or 3 PCLKB
0008 940Ch	S12AD2	A/D-Converted Value Addition/Average Count Select Register	ADADC	8	8	2 or 3 PCLKB
0008 940Eh	S12AD2	A/D Control Extended Register	ADCER	16	16	2 or 3 PCLKB
0008 9410h	S12AD2	A/D Conversion Start Trigger Select Register	ADSTRGR	16	16	2 or 3 PCLKB
0008 9412h	S12AD2	A/D Conversion Extended Input Control Register	ADEXICR	16	16	2 or 3 PCLKB
0008 9414h	S12AD2	A/D Channel Select Register B0	ADANSB0	16	16	2 or 3 PCLKB
0008 9418h	S12AD2	A/D Data Duplication Register	ADDBLDR	16	16	2 or 3 PCLKB
0008 941Ch	S12AD2	A/D Internal Reference Voltage Data Register	ADOCDR	16	16	2 or 3 PCLKB
0008 941Eh	S12AD2	A/D Self-Diagnosis Data Register	ADRD	16	16	2 or 3 PCLKB
0008 9420h	S12AD2	A/D Data Register 0	ADDR0	16	16	2 or 3 PCLKB
0008 9422h	S12AD2	A/D Data Register 1	ADDR1	16	16	2 or 3 PCLKB
0008 9424h	S12AD2	A/D Data Register 2	ADDR2	16	16	2 or 3 PCLKB
0008 9426h	S12AD2	A/D Data Register 3	ADDR3	16	16	2 or 3 PCLKB
0008 9428h	S12AD2	A/D Data Register 4	ADDR4	16	16	2 or 3 PCLKB
0008 942Ah	S12AD2	A/D Data Register 5	ADDR5	16	16	2 or 3 PCLKB
0008 942Ch	S12AD2	A/D Data Register 6	ADDR6	16	16	2 or 3 PCLKB
0008 942Eh	S12AD2	A/D Data Register 7	ADDR7	16	16	2 or 3 PCLKB
0008 9430h	S12AD2	A/D Data Register 8	ADDR8	16	16	2 or 3 PCLKB
0008 9432h	S12AD2	A/D Data Register 9	ADDR9	16	16	2 or 3 PCLKB
0008 9434h	S12AD2	A/D Data Register 10	ADDR10	16	16	2 or 3 PCLKB
0008 9436h	S12AD2	A/D Data Register 11	ADDR11	16	16	2 or 3 PCLKB
0008 947Ah	S12AD2	A/D Disconnection Detection Control Register	ADDISCR	8	8	2 or 3 PCLKB
0008 9480h	S12AD2	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2 or 3 PCLKB
0008 9484h	S12AD2	A/D Data Duplication Register A	ADDBLDRA	16	16	2 or 3 PCLKB
0008 9486h	S12AD2	A/D Data Duplication Register B	ADDBLDRB	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (22/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
000A 836Dh	RSCAN0	Transmit Buffer Status Register 1*2	TMSTS1	8	8	1 or 2 PCLKB
000A 836Eh	RSCAN0	Transmit Buffer Status Register 2*2	TMSTS2	8	8	1 or 2 PCLKB
000A 836Fh	RSCAN0	Transmit Buffer Status Register 3*2	TMSTS3	8	8	1 or 2 PCLKB
000A 8374h	RSCAN0	Transmit Buffer Transmit Request Status Register*2	TMTRSTS	16	16	2 or 3 PCLKB
000A 8376h	RSCAN0	Transmit Buffer Transmit Complete Status Register*2	TMTCSTS	16	16	2 or 3 PCLKB
000A 8378h	RSCAN0	Transmit Buffer Transmit Abort Status Register*2	TMTASTS	16	16	2 or 3 PCLKB
000A 837Ah	RSCAN0	Transmit Buffer Interrupt Enable Register*2	TMIEC	16	16	2 or 3 PCLKB
000A 837Ch	RSCAN0	Transmit History Buffer Control Register*2	THLCC0	16	16	2 or 3 PCLKB
000A 8380h	RSCAN0	Transmit History Buffer Status Register*2	THLSTS0	16	16	2 or 3 PCLKB
000A 8384h	RSCAN0	Transmit History Buffer Pointer Control Register*2	THLPCTR0	16	16	2 or 3 PCLKB
000A 8388h	RSCAN	Global Transmit Interrupt Status Register*2	GTINTSTS	16	16	2 or 3 PCLKB
000A 838Ah	RSCAN	Global RAM Window Control Register*2	GRWCR	16	16	2 or 3 PCLKB
000A 838Ch	RSCAN	Global Test Configuration Register*2	GTSTCFG	16	16	2 or 3 PCLKB
000A 838Eh	RSCAN	Global Test Control Register*2	GTSTCTRL	8	8	1 or 2 PCLKB
000A 8394h	RSCAN	Global Test Protection Unlock Register*2	GLOCKK	16	16	2 or 3 PCLKB
000A 83A0h	RSCAN	Receive Rule Entry Register 0AL*2	GAFLIDL0	16	16	2 or 3 PCLKB
000A 83A0h	RSCAN	Receive Buffer Register 0AL*2	RMIDL0	16	16	2 or 3 PCLKB
000A 83A2h	RSCAN	Receive Rule Entry Register 0AH*2	GAFLIDH0	16	16	2 or 3 PCLKB
000A 83A2h	RSCAN	Receive Buffer Register 0AH*2	RMIDH0	16	16	2 or 3 PCLKB
000A 83A4h	RSCAN	Receive Rule Entry Register 0BL*2	GAFLML0	16	16	2 or 3 PCLKB
000A 83A4h	RSCAN	Receive Buffer Register 0BL*2	RMTS0	16	16	2 or 3 PCLKB
000A 83A6h	RSCAN	Receive Rule Entry Register 0BH*2	GAFLMH0	16	16	2 or 3 PCLKB
000A 83A6h	RSCAN	Receive Buffer Register 0BH*2	RMPTR0	16	16	2 or 3 PCLKB
000A 83A8h	RSCAN	Receive Rule Entry Register 0CL*2	GAFLPL0	16	16	2 or 3 PCLKB
000A 83A8h	RSCAN	Receive Buffer Register 0CL*2	RMDF00	16	16	2 or 3 PCLKB
000A 83AAh	RSCAN	Receive Rule Entry Register 0CH*2	GAFLPH0	16	16	2 or 3 PCLKB
000A 83AAh	RSCAN	Receive Buffer Register 0CH*2	RMDF10	16	16	2 or 3 PCLKB
000A 83ACh	RSCAN	Receive Rule Entry Register 1AL*2	GAFLIDL1	16	16	2 or 3 PCLKB
000A 83ACh	RSCAN	Receive Buffer Register 0DL*2	RMDF20	16	16	2 or 3 PCLKB
000A 83AEh	RSCAN	Receive Rule Entry Register 1AH*2	GAFLIDH1	16	16	2 or 3 PCLKB
000A 83AEh	RSCAN	Receive Buffer Register 0DH*2	RMDF30	16	16	2 or 3 PCLKB
000A 83B0h	RSCAN	Receive Rule Entry Register 1BL*2	GAFLML1	16	16	2 or 3 PCLKB
000A 83B0h	RSCAN	Receive Buffer Register 1AL*2	RMIDL1	16	16	2 or 3 PCLKB
000A 83B2h	RSCAN	Receive Rule Entry Register 1BH*2	GAFLMH1	16	16	2 or 3 PCLKB
000A 83B2h	RSCAN	Receive Buffer Register 1AH*2	RMIDH1	16	16	2 or 3 PCLKB
000A 83B4h	RSCAN	Receive Rule Entry Register 1CL*2	GAFLPL1	16	16	2 or 3 PCLKB
000A 83B4h	RSCAN	Receive Buffer Register 1BL*2	RMTS1	16	16	2 or 3 PCLKB
000A 83B6h	RSCAN	Receive Rule Entry Register 1CH*2	GAFLPH1	16	16	2 or 3 PCLKB
000A 83B6h	RSCAN	Receive Buffer Register 1BH*2	RMPTR1	16	16	2 or 3 PCLKB
000A 83B8h	RSCAN	Receive Rule Entry Register 2AL*2	GAFLIDL2	16	16	2 or 3 PCLKB
000A 83B8h	RSCAN	Receive Buffer Register 1CL*2	RMDF01	16	16	2 or 3 PCLKB
000A 83BAh	RSCAN	Receive Rule Entry Register 2AH*2	GAFLIDH2	16	16	2 or 3 PCLKB
000A 83BAh	RSCAN	Receive Buffer Register 1CH*2	RMDF11	16	16	2 or 3 PCLKB
000A 83BCh	RSCAN	Receive Rule Entry Register 2BL*2	GAFLML2	16	16	2 or 3 PCLKB
000A 83BCh	RSCAN	Receive Buffer Register 1DL*2	RMDF21	16	16	2 or 3 PCLKB
000A 83BEh	RSCAN	Receive Rule Entry Register 2BH*2	GAFLMH2	16	16	2 or 3 PCLKB
000A 83BEh	RSCAN	Receive Buffer Register 1DH*2	RMDF31	16	16	2 or 3 PCLKB
000A 83C0h	RSCAN	Receive Rule Entry Register 2CL*2	GAFLPL2	16	16	2 or 3 PCLKB
000A 83C0h	RSCAN	Receive Buffer Register 2AL*2	RMIDL2	16	16	2 or 3 PCLKB
000A 83C2h	RSCAN	Receive Rule Entry Register 2CH*2	GAFLPH2	16	16	2 or 3 PCLKB
000A 83C2h	RSCAN	Receive Buffer Register 2AH*2	RMIDH2	16	16	2 or 3 PCLKB
000A 83C4h	RSCAN	Receive Rule Entry Register 3AL*2	GAFLIDL3	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (25/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
000A 842Ch	RSCAN	Receive Buffer Register 8DL*2	RMDF28	16	16	2 or 3 PCLKB
000A 842Eh	RSCAN	Receive Rule Entry Register 11CH*2	GAFLPH11	16	16	2 or 3 PCLKB
000A 842Eh	RSCAN	Receive Buffer Register 8DH*2	RMDF38	16	16	2 or 3 PCLKB
000A 8430h	RSCAN	Receive Rule Entry Register 12AL*2	GAFLIDL12	16	16	2 or 3 PCLKB
000A 8430h	RSCAN	Receive Buffer Register 9AL*2	RMIDL9	16	16	2 or 3 PCLKB
000A 8432h	RSCAN	Receive Rule Entry Register 12AH*2	GAFLIDH12	16	16	2 or 3 PCLKB
000A 8432h	RSCAN	Receive Buffer Register 9AH*2	RMIDH9	16	16	2 or 3 PCLKB
000A 8434h	RSCAN	Receive Rule Entry Register 12BL*2	GAFLML12	16	16	2 or 3 PCLKB
000A 8434h	RSCAN	Receive Buffer Register 9BL*2	RMTS9	16	16	2 or 3 PCLKB
000A 8436h	RSCAN	Receive Rule Entry Register 12BH*2	GAFLMH12	16	16	2 or 3 PCLKB
000A 8436h	RSCAN	Receive Buffer Register 9BH*2	RMPTR9	16	16	2 or 3 PCLKB
000A 8438h	RSCAN	Receive Rule Entry Register 12CL*2	GAFLPL12	16	16	2 or 3 PCLKB
000A 8438h	RSCAN	Receive Buffer Register 9CL*2	RMDF09	16	16	2 or 3 PCLKB
000A 843Ah	RSCAN	Receive Rule Entry Register 12CH*2	GAFLPH12	16	16	2 or 3 PCLKB
000A 843Ah	RSCAN	Receive Buffer Register 9CH*2	RMDF19	16	16	2 or 3 PCLKB
000A 843Ch	RSCAN	Receive Rule Entry Register 13AL*2	GAFLIDL13	16	16	2 or 3 PCLKB
000A 843Ch	RSCAN	Receive Buffer Register 9DL*2	RMDF29	16	16	2 or 3 PCLKB
000A 843Eh	RSCAN	Receive Rule Entry Register 13AH*2	GAFLIDH13	16	16	2 or 3 PCLKB
000A 843Eh	RSCAN	Receive Buffer Register 9DH*2	RMDF39	16	16	2 or 3 PCLKB
000A 8440h	RSCAN	Receive Rule Entry Register 13BL*2	GAFLML13	16	16	2 or 3 PCLKB
000A 8440h	RSCAN	Receive Buffer Register 10AL*2	RMIDL10	16	16	2 or 3 PCLKB
000A 8442h	RSCAN	Receive Rule Entry Register 13BH*2	GAFLMH13	16	16	2 or 3 PCLKB
000A 8442h	RSCAN	Receive Buffer Register 10AH*2	RMIDH10	16	16	2 or 3 PCLKB
000A 8444h	RSCAN	Receive Rule Entry Register 13CL*2	GAFLPL13	16	16	2 or 3 PCLKB
000A 8444h	RSCAN	Receive Buffer Register 10BL*2	RMTS10	16	16	2 or 3 PCLKB
000A 8446h	RSCAN	Receive Rule Entry Register 13CH*2	GAFLPH13	16	16	2 or 3 PCLKB
000A 8446h	RSCAN	Receive Buffer Register 10BH*2	RMPTR10	16	16	2 or 3 PCLKB
000A 8448h	RSCAN	Receive Rule Entry Register 14AL*2	GAFLIDL14	16	16	2 or 3 PCLKB
000A 8448h	RSCAN	Receive Buffer Register 10CL*2	RMDF010	16	16	2 or 3 PCLKB
000A 844Ah	RSCAN	Receive Rule Entry Register 14AH*2	GAFLIDH14	16	16	2 or 3 PCLKB
000A 844Ah	RSCAN	Receive Buffer Register 10CH*2	RMDF110	16	16	2 or 3 PCLKB
000A 844Ch	RSCAN	Receive Rule Entry Register 14BL*2	GAFLML14	16	16	2 or 3 PCLKB
000A 844Ch	RSCAN	Receive Buffer Register 10DL*2	RMDF210	16	16	2 or 3 PCLKB
000A 844Eh	RSCAN	Receive Rule Entry Register 14BH*2	GAFLMH14	16	16	2 or 3 PCLKB
000A 844Eh	RSCAN	Receive Buffer Register 10DH*2	RMDF310	16	16	2 or 3 PCLKB
000A 8450h	RSCAN	Receive Rule Entry Register 14CL*2	GAFLPL14	16	16	2 or 3 PCLKB
000A 8450h	RSCAN	Receive Buffer Register 11AL*2	RMIDL11	16	16	2 or 3 PCLKB
000A 8452h	RSCAN	Receive Rule Entry Register 14CH*2	GAFLPH14	16	16	2 or 3 PCLKB
000A 8452h	RSCAN	Receive Buffer Register 11AH*2	RMIDH11	16	16	2 or 3 PCLKB
000A 8454h	RSCAN	Receive Rule Entry Register 15AL*2	GAFLIDL15	16	16	2 or 3 PCLKB
000A 8454h	RSCAN	Receive Buffer Register 11BL*2	RMTS11	16	16	2 or 3 PCLKB
000A 8456h	RSCAN	Receive Rule Entry Register 15AH*2	GAFLIDH15	16	16	2 or 3 PCLKB
000A 8456h	RSCAN	Receive Buffer Register 11BH*2	RMPTR11	16	16	2 or 3 PCLKB
000A 8458h	RSCAN	Receive Rule Entry Register 15BL*2	GAFLML15	16	16	2 or 3 PCLKB
000A 8458h	RSCAN	Receive Buffer Register 11CL*2	RMDF011	16	16	2 or 3 PCLKB
000A 845Ah	RSCAN	Receive Rule Entry Register 15BH*2	GAFLMH15	16	16	2 or 3 PCLKB
000A 845Ah	RSCAN	Receive Buffer Register 11CH*2	RMDF111	16	16	2 or 3 PCLKB
000A 845Ch	RSCAN	Receive Rule Entry Register 15CL*2	GAFLPL15	16	16	2 or 3 PCLKB
000A 845Ch	RSCAN	Receive Buffer Register 11DL*2	RMDF211	16	16	2 or 3 PCLKB
000A 845Eh	RSCAN	Receive Rule Entry Register 15CH*2	GAFLPH15	16	16	2 or 3 PCLKB
000A 845Eh	RSCAN	Receive Buffer Register 11DH*2	RMDF311	16	16	2 or 3 PCLKB
000A 8460h	RSCAN	Receive Buffer Register 12AL*2	RMIDL12	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (32/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
000C 1A4Dh	MTU7	Timer Control Register 2	TCR2	8	8	4 or 5 PCLKA
000C 1A50h	MTU6	Timer Synchronous Clear Register	TSYCR	8	8	4 or 5 PCLKA
000C 1A60h	MTU	Timer Waveform Control Register B	TWCRB	8	8	4 or 5 PCLKA
000C 1A70h	MTU	Timer Mode Register 2B	TMDR2B	8	8	4 or 5 PCLKA
000C 1A72h	MTU6	Timer General Register E	TGRE	16	16	4 or 5 PCLKA
000C 1A74h	MTU7	Timer General Register E	TGRE	16	16	4 or 5 PCLKA
000C 1A76h	MTU7	Timer General Register F	TGRF	16	16	4 or 5 PCLKA
000C 1A80h	MTU	Timer Start Register B	TSTRB	8	8, 16	4 or 5 PCLKA
000C 1A81h	MTU	Timer Synchronous Register B	TSYRB	8	8	4 or 5 PCLKA
000C 1A84h	MTU	Timer Read/Write Enable Register B	TRWERB	8	8	4 or 5 PCLKA
000C 1A93h	MTU6	Noise Filter Control Register 6	NFCR6	8	8	4 or 5 PCLKA
000C 1A94h	MTU7	Noise Filter Control Register 7	NFCR7	8	8	4 or 5 PCLKA
000C 1A95h	MTU5	Noise Filter Control Register 5	NFCR5	8	8	4 or 5 PCLKA
000C 1C80h	MTU5	Timer Counter U	TCNTU	16	16, 32	4 or 5 PCLKA
000C 1C82h	MTU5	Timer General Register U	TGRU	16	16	4 or 5 PCLKA
000C 1C84h	MTU5	Timer Control Register U	TCRU	8	8	4 or 5 PCLKA
000C 1C85h	MTU5	Timer Control Register 2U	TCR2U	8	8	4 or 5 PCLKA
000C 1C86h	MTU5	Timer I/O Control Register U	TIORU	8	8	4 or 5 PCLKA
000C 1C90h	MTU5	Timer Counter V	TCNTV	16	16, 32	4 or 5 PCLKA
000C 1C92h	MTU5	Timer General Register V	TGRV	16	16	4 or 5 PCLKA
000C 1C94h	MTU5	Timer Control Register V	TCRV	8	8	4 or 5 PCLKA
000C 1C95h	MTU5	Timer Control Register 2V	TCR2V	8	8	4 or 5 PCLKA
000C 1C96h	MTU5	Timer I/O Control Register V	TIORV	8	8	4 or 5 PCLKA
000C 1CA0h	MTU5	Timer Counter W	TCNTW	16	16, 32	4 or 5 PCLKA
000C 1CA2h	MTU5	Timer General Register W	TGRW	16	16	4 or 5 PCLKA
000C 1CA4h	MTU5	Timer Control Register W	TCRW	8	8	4 or 5 PCLKA
000C 1CA5h	MTU5	Timer Control Register 2W	TCR2W	8	8	4 or 5 PCLKA
000C 1CA6h	MTU5	Timer I/O Control Register W	TIORW	8	8	4 or 5 PCLKA
000C 1CB2h	MTU5	Timer Interrupt Enable Register	TIER	8	8	4 or 5 PCLKA
000C 1CB4h	MTU5	Timer Start Register	TSTR	8	8	4 or 5 PCLKA
000C 1CB6h	MTU5	Timer Compare Match Clear Register	TCNTCMPCLR	8	8	4 or 5 PCLKA
000C 1D30h	MTU	A/D Conversion Start Request Select Register 0	TADSTRGR0	8	8	4 or 5 PCLKA
000C 1D32h	MTU	A/D Conversion Start Request Select Register 1	TADSTRGR1	8	8	4 or 5 PCLKA
000C 2000h	GPT	General PWM Timer Software Start Register*2	GTSTR	16	8, 16, 32	4 or 5 PCLKA
000C 2002h	GPT	Noise Filter Control Register*2	NFCR	16	16, 32	4 or 5 PCLKA
000C 2004h	GPT	General PWM Timer Hardware Source Start/Stop Control Register 0*2	GTHSCR	16	8, 16, 32	4 or 5 PCLKA
000C 2006h	GPT	General PWM Timer Hardware Source Clear Control Register*2	GTHCCR	16	8, 16, 32	4 or 5 PCLKA
000C 2008h	GPT	General PWM Timer Hardware Start Source Select Register*2	GTHSSR	16	8, 16, 32	4 or 5 PCLKA
000C 200Ah	GPT	General PWM Timer Hardware Stop/Clear Source Select Register*2	GTHPSR	16	8, 16, 32	4 or 5 PCLKA
000C 200Ch	GPT	General PWM Timer Write-Protection Register*2	GTWP	16	8, 16, 32	4 or 5 PCLKA
000C 200Eh	GPT	General PWM Timer Sync Register*2	GTSYNC	16	8, 16, 32	4 or 5 PCLKA
000C 2010h	GPT	General PWM Timer External Trigger Input Interrupt Register*2	GTETINT	16	8, 16, 32	4 or 5 PCLKA
000C 2014h	GPT	General PWM Timer Buffer Operation Disable Register*2	GTBDR	16	8, 16, 32	4 or 5 PCLKA
000C 2018h	GPT	General PWM Timer Start Write-Protection Register*2	GTSWP	16	8, 16, 32	4 or 5 PCLKA
000C 201Ch	GPT	General PWM Timer Clearing Write-Protection Register*2	GTCWP	16	8, 16, 32	4 or 5 PCLKA
000C 2020h	GPT	General PWM Timer Common Register Write-Protection Register*2	GTCMNWP	16	8, 16, 32	4 or 5 PCLKA
000C 2024h	GPT	General PWM Timer Mode Register*2	GTMDR	16	8, 16, 32	4 or 5 PCLKA
000C 2028h	GPT	General PWM Timer External Clock Noise Filter Control Register*2	GTECNFCR	32	8, 16, 32	4 or 5 PCLKA

Table 5.4 DC Characteristics (2)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	RES#, MD, port E2	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V, VCC
Three-state leakage current (off-state)	Port 4, port 5, port 6	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0 V, VREF
	Ports except for 5-V tolerant ports and port 4, port 5, port 6		—	—	0.2		V_{in} = 0 V, VCC
	Ports for 5 V tolerant		—	—	1.0		V_{in} = 0 V, 5.8 V
Input capacitance	All input pins	C_{in}	—	4	15	pF	V_{in} = 0 mV, f = 1 MHz, T_a = 25°C
Input pull-up resistor	All ports (except for port E2)	R_U	10	20	50	kΩ	V_{in} = 0 V

Table 5.5 DC Characteristics (3)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item					Symbol	Chip Version A		Chip Version B		Unit	Test Conditions
						Typ. *7	Max.	Typ. *7	Max.		
Supply current *1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 80 MHz	I_{CC}	26.0	—	26.0	—	mA	
				ICLK = 64 MHz		20.7	—	20.7	—		
				ICLK = 32 MHz		11.8	—	11.8	—		
				ICLK = 16 MHz		7.0	—	7.0	—		
				ICLK = 8 MHz		4.7	—	4.7	—		
			All peripheral operation: Normal	ICLK = 80 MHz*3		35.0	—	40.5	—		
				ICLK = 64 MHz*4		28.5	—	32.5	—		
				ICLK = 32 MHz*5		18.5	—	20.9	—		
				ICLK = 16 MHz*5		10.5	—	11.7	—		
				ICLK = 8 MHz*5		6.4	—	7.0	—		
			All peripheral operation: Max.	ICLK = 80 MHz*3		—	70.0	—	80.0		
				ICLK = 64 MHz*4		—	60.0	—	70.0		
				ICLK = 32 MHz*5		—	40.0	—	45.0		
		Sleep mode	No peripheral operation*2	ICLK = 80 MHz		7.2	—	7.2	—		
				ICLK = 64 MHz		6.1	—	6.1	—		
				ICLK = 32 MHz		4.4	—	4.4	—		
				ICLK = 16 MHz		3.4	—	3.4	—		
				ICLK = 8 MHz		2.9	—	2.9	—		
			All peripheral operation: Normal	ICLK = 80 MHz*3		22.4	—	26.9	—		
				ICLK = 64 MHz*4		18.4	—	21.9	—		
				ICLK = 32 MHz*5		13.5	—	15.5	—		
				ICLK = 16 MHz*5		8.0	—	9.0	—		
				ICLK = 8 MHz*5		5.2	—	5.7	—		

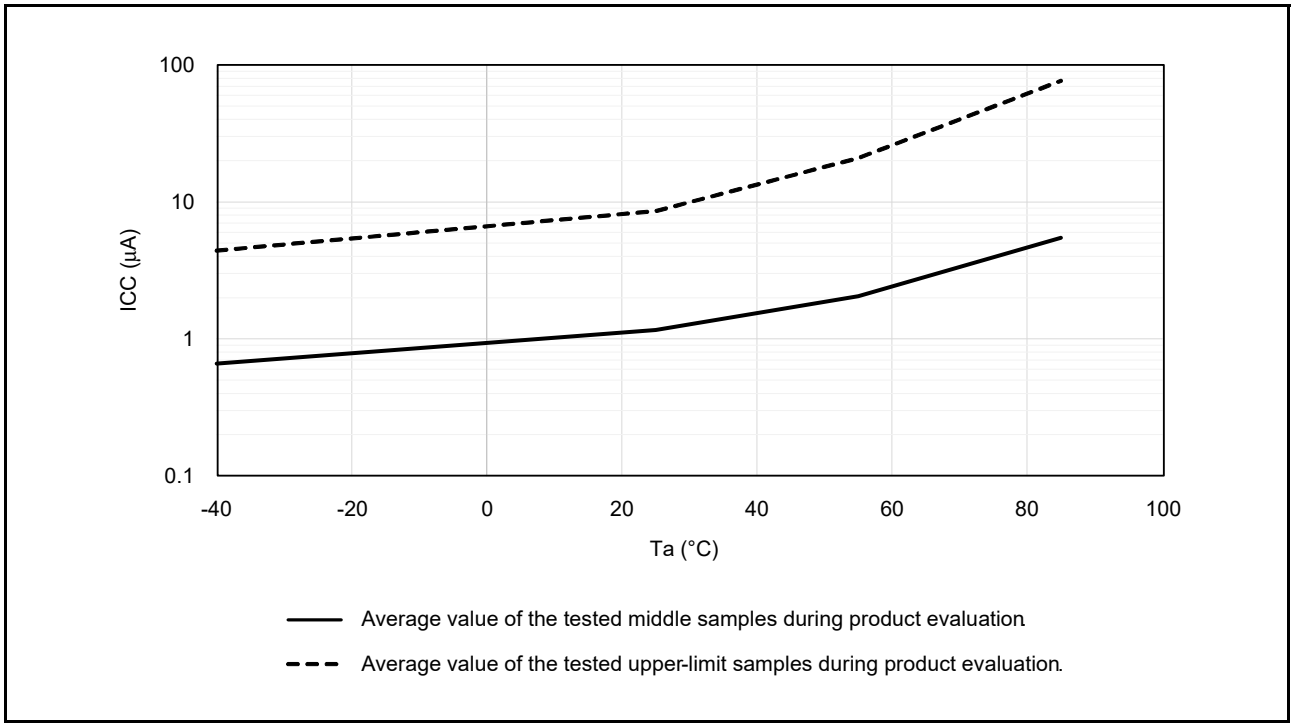


Figure 5.3 Temperature Dependency in Software Standby Mode (Chip Version A) (Reference Data)

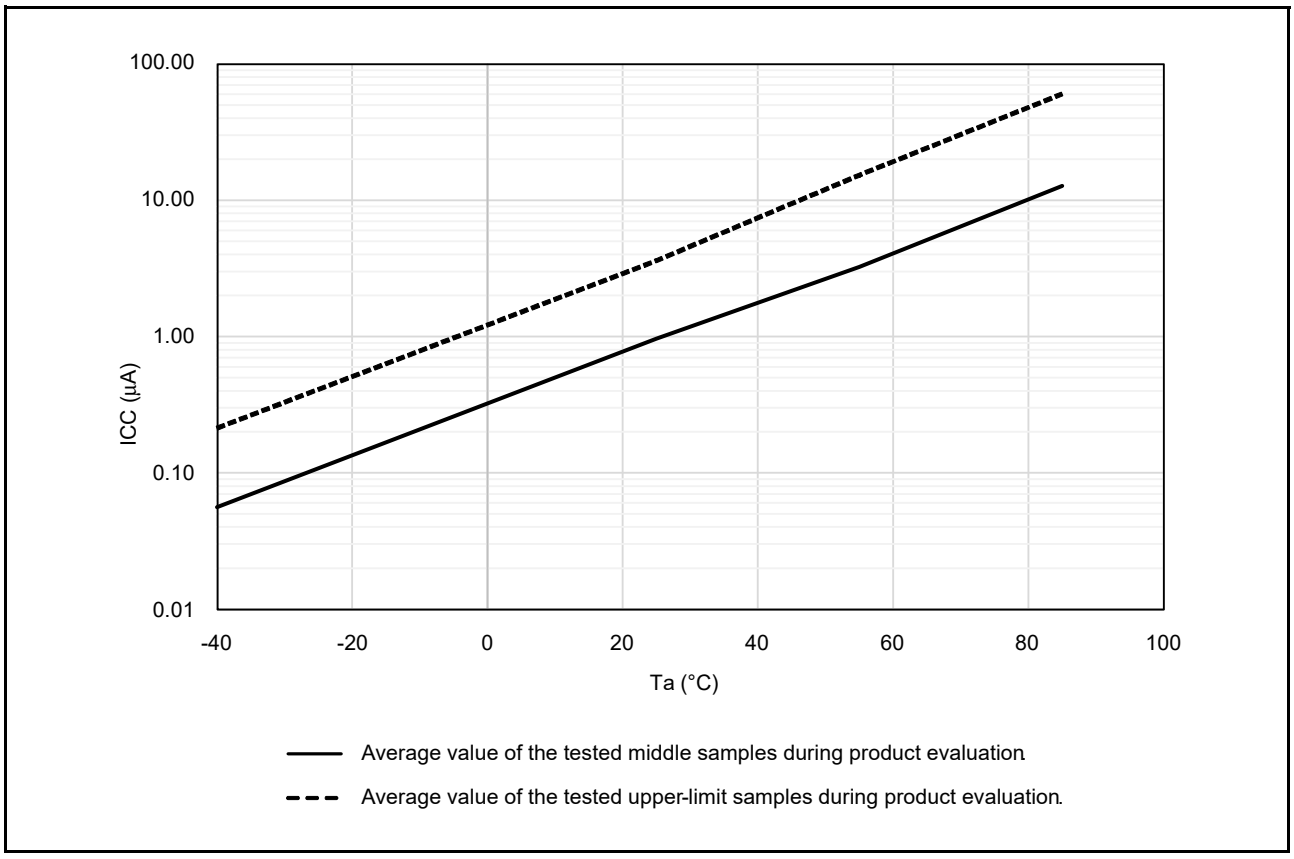


Figure 5.4 Temperature Dependency in Software Standby Mode (Chip Version B) (Reference Data)

5.3.3 Timing of Recovery from Low Power Consumption Modes

Table 5.18 Timing of Recovery from Low Power Consumption Modes (1)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	High-speed mode	Crystal connected to main clock oscillator	Main clock oscillator operating*2	t_{SBYMC}	—	2	3	ms	Figure 5.32
			Main clock oscillator and PLL circuit operating*3	t_{SBYPC}	—	2	3	ms	
		External clock input to main clock oscillator	Main clock oscillator operating*4	t_{SBYEX}	—	35	50	µs	
			Main clock oscillator and PLL circuit operating*5	t_{SBYPE}	—	70	95	µs	
		HOCO clock operation	HOCO clock oscillator operation 1*6	t_{SBYHO}	—	40	55	µs	
			HOCO clock oscillator operation 2*7		—	75	90	µs	
			HOCO clock oscillator, PLL circuit operation*8	t_{SBYPH}	—	110	130	µs	
		LOCO clock oscillator operating*9		t_{SBYLO}	—	40	55	µs	

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. The recovery time when multiple oscillators are operating varies depending on the operating state of the oscillators that are not selected as the system clock source. The above table applies when only the corresponding clock is operating.

Note 2. When the frequency of crystal is 20 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are not divided.

Note 3. When the frequency of PLL is 80 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
When the frequencies of ICLK and PCLKA are set to 80 MHz, PCLKB and PCLKD are set to 40 MHz, and FCLK is set to 20 MHz.

Note 4. When the frequency of the external clock is 20 MHz.
When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are not divided.

Note 5. When the frequency of PLL is 80 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.
When the frequencies of ICLK and PCLKA are set to 80 MHz, PCLKB and PCLKD are set to 40 MHz, and FCLK is set to 20 MHz.

Note 6. When the frequency of the high-speed on-chip oscillator is 32 MHz. When the high-speed on-chip oscillator wait control register (HOCOWTCR) is set to 05h. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are not divided.

Note 7. When the frequency of the high-speed on-chip oscillator is 64 MHz. Set the high-speed on-chip oscillator wait control register (HOCOWTCR) is set to 06h. When the frequencies of ICLK and PCLKA are set to 64 MHz, and the frequencies of PCLKB, PCLKD, and FCLK are set to 32 MHz.

Note 8. When the frequency of the high-speed on-chip oscillator is 32 MHz, and the frequency of PLL is 80 MHz. When the high-speed on-chip oscillator wait control register (HOCOWTCR) is set to 05h. When the frequencies of ICLK and PCLKA are set to 80 MHz, the frequencies of PCLKB and PCLKD are set to 40 MHz, and the frequency of FCLK is set to 20MHz.

Note 9. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are not divided.

5.3.4 Control Signal Timing

Table 5.22 Control Signal Timing

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter disabled (NMIFLTE.NFLTEN = 0)	$t_{Pcyc} \times 2 \le 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		NMI digital filter enabled (NMIFLTE.NFLTEN = 1)	$t_{NMICK} \times 3 \le 200$ ns
		$t_{NMICK} \times 3.5$*2	—	—			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter disabled (IRQFLTE0.FLTENi = 0)	$t_{Pcyc} \times 2 \le 200$ ns
		$t_{Pcyc} \times 2$*1	—	—			$t_{Pcyc} \times 2 > 200$ ns
		200	—	—		IRQ digital filter enabled (IRQFLTE0.FLTENi = 1)	$t_{IRQCK} \times 3 \le 200$ ns
		$t_{IRQCK} \times 3.5$*3	—	—			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in software standby mode.
Note 1. t_{Pcyc} indicates the cycle of PCLKB.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

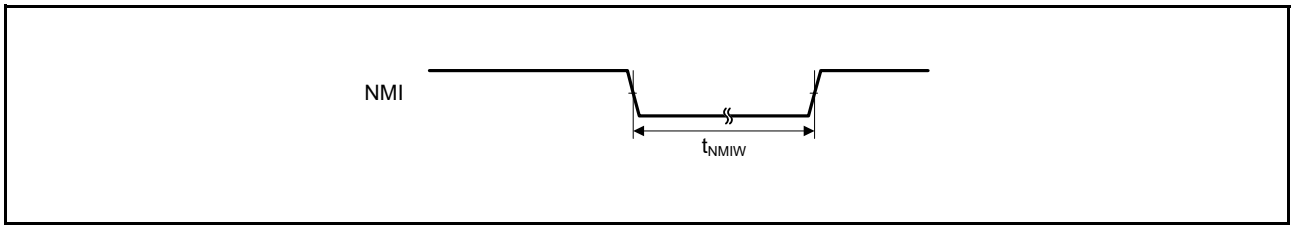


Figure 5.34 NMI Interrupt Input Timing

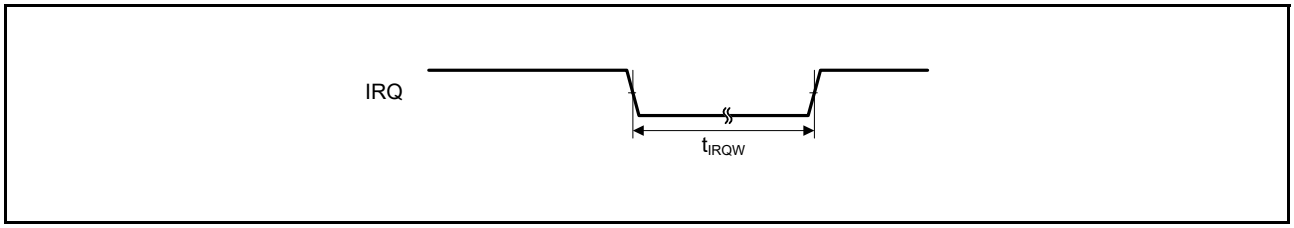


Figure 5.35 IRQ Interrupt Input Timing

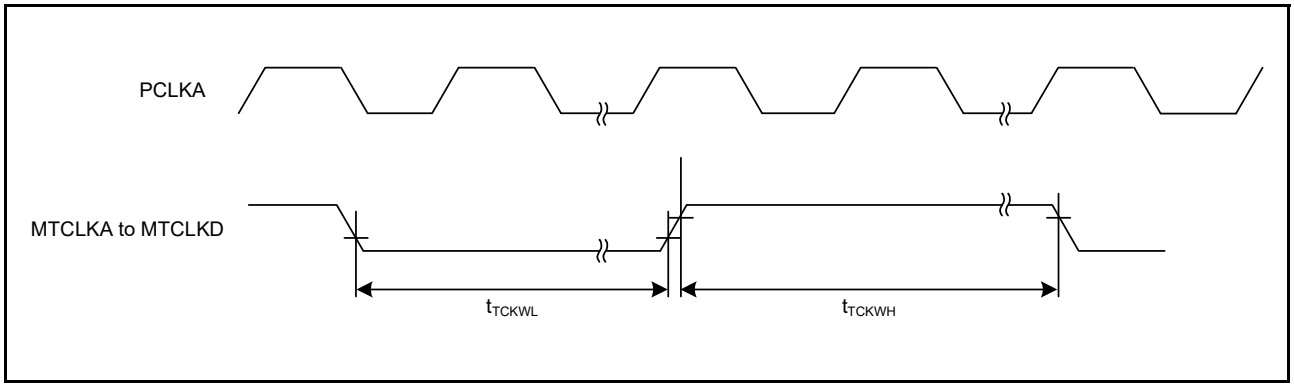


Figure 5.38 MTU3 Clock Input Timing

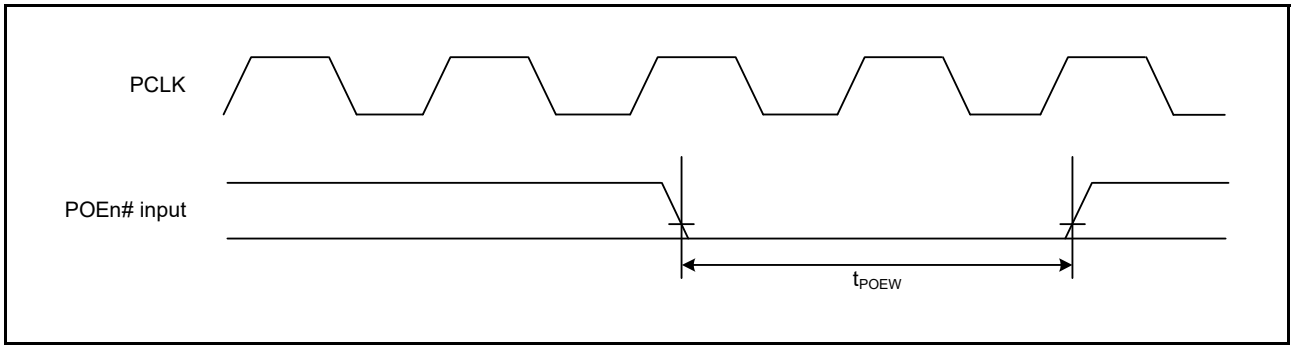


Figure 5.39 POE# Input Timing

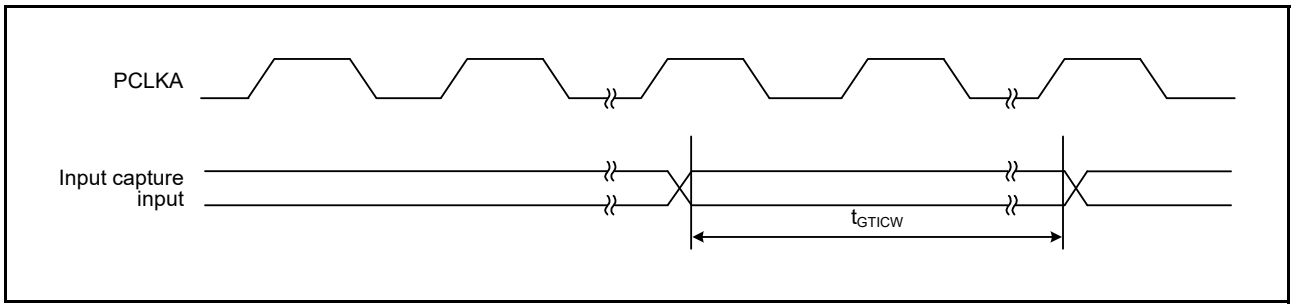


Figure 5.40 Input Timing of GPT Input Capture

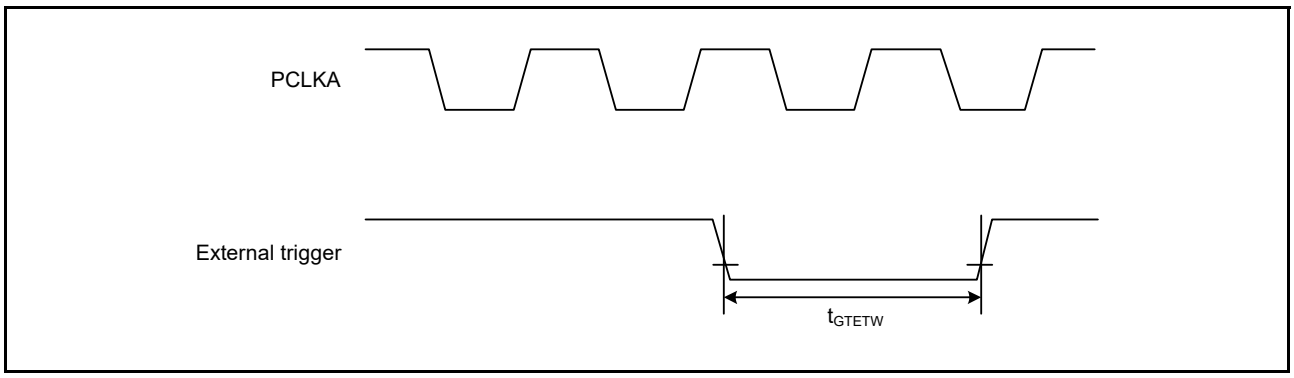


Figure 5.41 Timing of the GPT External Trigger Input

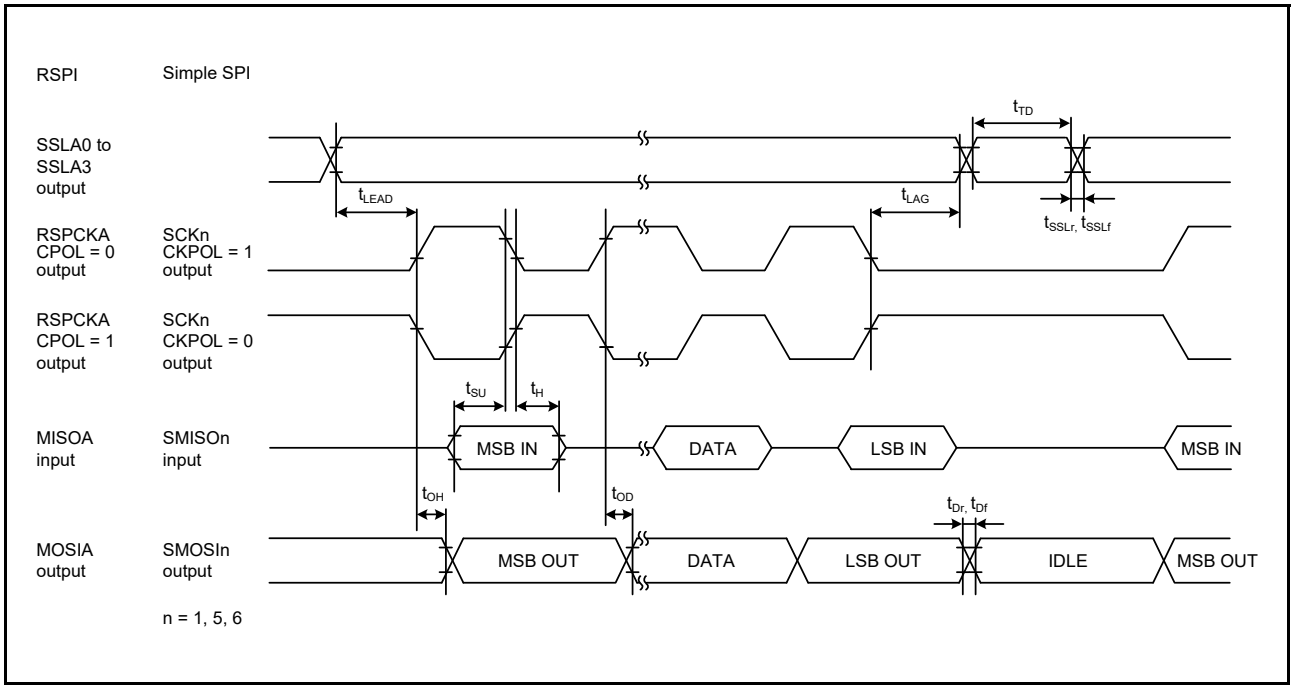


Figure 5.49 RSPI Timing (Master, CPHA = 1) and Simple SPI Clock Timing (Master, CKPH = 0)

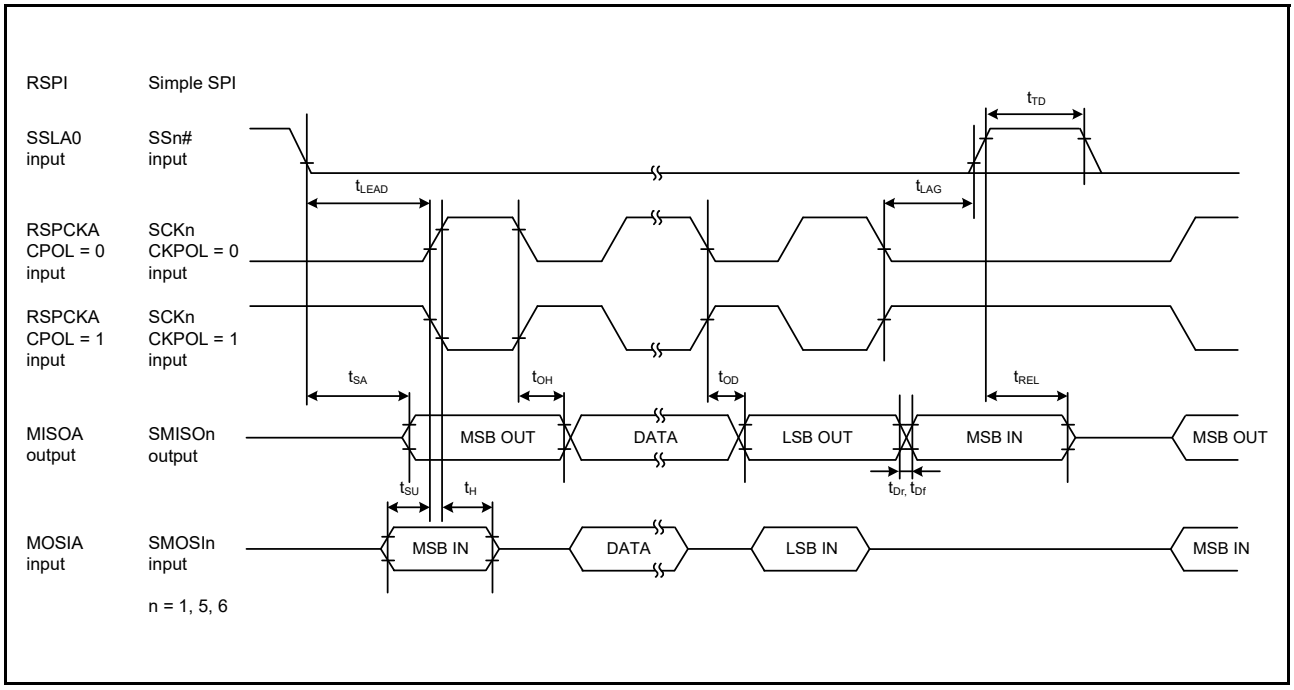


Figure 5.50 RSPI Timing (Slave, CPHA = 0) and Simple SPI Clock Timing (Slave, CKPH = 1)

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

5.6 Comparator Characteristics

Table 5.33 Comparator Characteristics

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Offset voltage	V_{cioff}	—	—	40	mV	
Reference input voltage range	V_{cref}	0	—	VREF	V	
Response time	t_{cr}	—	—	200	ns	VOD = 100 mV CMPCTL.CDFS = 0
	t_{cf}	—	—	200	ns	
Stabilization wait time for input selection	t_{cwait}	300	—	—	ns	
Operation stabilization wait time	t_{cmp}		—	1	µs	

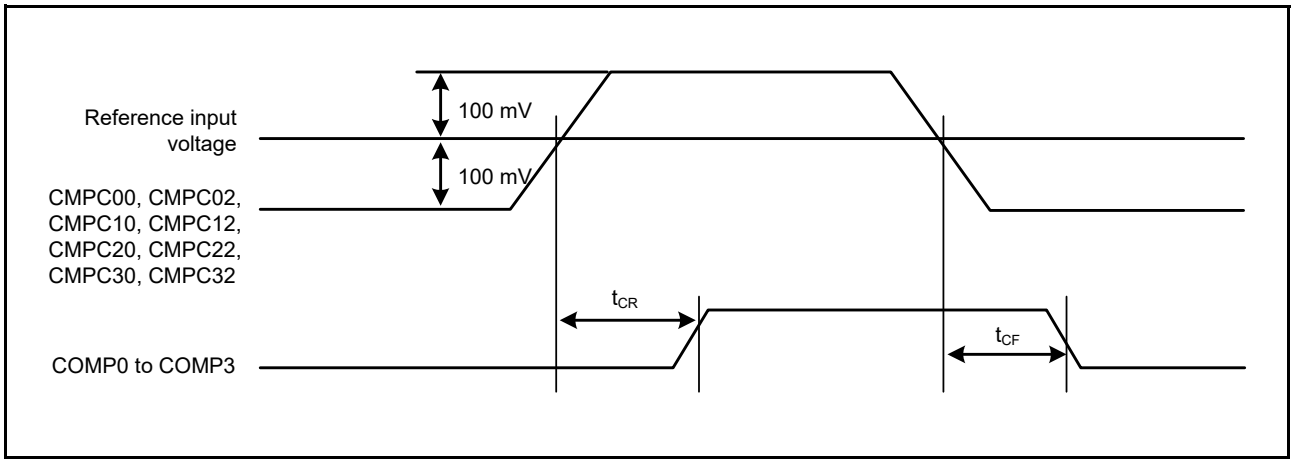


Figure 5.54 Comparator Response Time