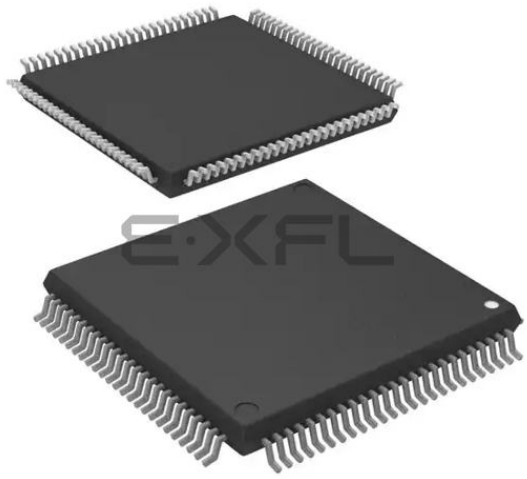
Renesas Electronics America Inc - R5F524TBADFP#31 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	80
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 22x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f524tbadfp-31

Table 1.1 Outline of Specifications (2/4)

Classification	Module/Function	Description
Interrupt	Interrupt controller (ICUb)	• Interrupt vectors: 163 • External interrupts: 9 (NMI, IRQ0 to IRQ7 pins) • Non-maskable interrupts: 5 (NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, and IWDT interrupt) • 16 levels specifiable for the order of priority
DMA	Data transfer controller (DTCa)	• Transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Interrupts • Chain transfer function
I/O ports	General I/O ports	100-pin/80-pin/64-pin • I/O: 80/60/48 • Input: 1/1/1 • Pull-up resistors: 80/60/48 • Open-drain outputs: 60/45/37 • 5-V tolerance: 2/2/2
Multi-function pin controller (MPC)		Capable of selecting the input/output function from multiple pins
Timers	Multi-function timer pulse unit 3 (MTU3d)	• 9 units (16 bits × 9 channels) • Provides up to 28 pulse-input/output lines and three pulse-input lines • Select from among fourteen counter-input clock signals for each channel (PCLK/1, PCLK/2, PCLK/4, PCLK/8, PCLK/16, PCLK/32, PCLK/64, PCLK/256, PCLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD, MTIOC1A) other than channel 1/3/4/6/7, for which only eleven signals are available, channel 2 for 12, channel 5 for 10 • 43 general registers including 28 output compare/input capture registers • Counter clear operation (with compare match- or input capture-sourced simultaneous counter clear capability) • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous register input/output by synchronous counter operation • Buffer operation • Cascaded operation • 45 interrupt sources • Automatic transfer of register data • Pulse output modes: Toggle/PWM/complementary PWM/reset-synchronized PWM • Complementary PWM output mode 3-phase non-overlapping waveform output for inverter control Automatic dead time setting Adjustable PWM duty cycle: from 0 to 100% A/D conversion request delaying function Interrupt at crest/trough can be skipped Double buffer function • Reset-synchronized PWM mode Outputs three phases each for positive and negative PWM waveforms in user-specified duty cycle • Phase counting modes: 16-bit mode (channel 1 and 2)/32-bit mode (channel 1 and 2) • Dead time compensation counter function • A/D converter start trigger can be generated • A/D converter start triggers can be skipped • Signals from the input capture and external counter clock pins are input via a digital filter
	Port output enable 3 (POE3b, POE3A)	• POE3b Control of the high-impedance state of the MTU3's waveform output pins Startup by input from signal sources on 6 pins (POE0#, POE4#, POE8#, POE10#, POE11#, and POE12#) Startup by detection of short-circuited outputs (detection of simultaneous PMW output at the active level) Startup by detection of oscillation stopping or by a comparator, or under software control Control of addition of pins for output control is programmable • POE3A (The following functions are added to the POE3b) Control of the high-impedance state of GPT's waveform output pins Control of the MTU3/GPT waveform output pins and switching them to operate as general I/O ports A comparator detection interrupt source can be set for each output pin group

Table 1.5 List of Pins and Pin Functions (100-Pin LFQFP, Chip Version B) (3/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (TMR, MTU, POE, CAC, GPT)	Communications (SCI, RSPI, RIIC, RSCAN)	Others
94	AVSS0				
95	AVSS1				
96		P82	MTIC5U, MTIC5U#, TMO4	SCK6	
97		P81	MTIC5V, MTIC5V#, TMCI4	TXD6, SMOSI6, SSDA6	
98		P80	MTIC5W, MTIC5W#, TMRI4	RXD6, SMISO6, SSCL6	
99		P11	MTIOC3A, MTIOC3A#, MTCLKC, MTCLKC#, TMO3		IRQ1
100		P10	MTIOC9B, MTIOC9B#, MTCLKD, MTCLKD#, TMRI3, POE12#	CTS6#, RTS6#, SS6#	IRQ0

Table 1.8 List of Pins and Pin Functions (64-Pin LFQFP) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE, CAC)	Communications (SCI, RSPI, RIIC)	Others
1		P02	MTIOC9D	CTS1#, RTS1#, SS1#	IRQ5, ADST0
2		P00			IRQ2, ADST1
3	VCL				
4	MD				FINED
5		P01	POE12#		IRQ4, ADST2
6	RES#				
7	XTAL	P37			
8	VSS				
9	EXTAL	P36			
10	VCC				
11		PE2	POE10#		NMI
12		PD7	MTIOC9A, TMRI1, TMRI5	SSLA1	
13		PD6	MTIOC9C, TMO1	CTS1#, RTS1#, SS1#	
14		PD5	TMRI0, TMRI6	RXD1, SMISO1, SSCL1	
15		PD4	TMCI0, TMCI6	SCK1	IRQ2
16		PD3	TMO0	TXD1, SMOSI1, SSDA1	
17		PB6		RXD5, SMISO5, SSCL5	IRQ5
18		PB5		TXD5, SMOSI5, SSDA5	
19		PB4	POE8#	CTS5#, RTS5#, SS5#	IRQ3
20		PB3	MTIOC0A, CACREF	SCK6, RSPCKA	
21		PB2	MTIOC0B, TMRI0, ADSM0	TXD6, SMOSI6, SSDA6, SDA0	
22		PB1	MTIOC0C, TMCI0, ADSM1	RXD6, SMISO6, SSCL6, SCL0	
23	VCC				
24		P96	POE4#		IRQ4
25	VSS				
26		P95	MTIOC6B		
27		P94	MTIOC7A		
28		P93	MTIOC7B		
29		P92	MTIOC6D		
30		P91	MTIOC7C		
31		P90	MTIOC7D		
32		P76	MTIOC4D		
33		P75	MTIOC4C		
34		P74	MTIOC3D		
35		P73	MTIOC4B		
36		P72	MTIOC4A		
37		P71	MTIOC3B		
38		P70	POE0#		IRQ5
39	VCC				
40		P31	MTIOC0A, MTCLKC, TMRI6	SSLA1	IRQ6
41	VSS				
42		P30	MTIOC0B, MTCLKD, TMCI6	SSLA0	IRQ7, COMP3
43		P24	MTIC5U, TMCI2, TMO6	RSPCKA	COMP0
44		P23	MTIC5V, TMO2, CACREF	MOSIA	COMP1
45		P22	MTIC5W, TMRI2, TMO4	MISOA	ADTRG2#, COMP2
46		P21	MTCLKA, MTIOC9A, TMCI4		IRQ6, ADTRG1#, AN116, CVREFC1
47	AVCC2/VREF				
48	AVSS2				
49		P54			AN210, IRQ2
50		P53			AN209, IRQ1
51		P52			AN208, IRQ0
52		P51			AN207
53		P50			AN206

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
0008 0000h	SYSTEM	Mode Monitor Register	MDMONR	16	16	3 ICLK
0008 0008h	SYSTEM	System Control Register 1	SYSCR1	16	16	3 ICLK
0008 000Ch	SYSTEM	Standby Control Register	SBYCR	16	16	3 ICLK
0008 0010h	SYSTEM	Module Stop Control Register A	MSTPCRA	32	32	3 ICLK
0008 0014h	SYSTEM	Module Stop Control Register B	MSTPCRB	32	32	3 ICLK
0008 0018h	SYSTEM	Module Stop Control Register C	MSTPCRC	32	32	3 ICLK
0008 0020h	SYSTEM	System Clock Control Register	SCKCR	32	32	3 ICLK
0008 0026h	SYSTEM	System Clock Control Register 3	SCKCR3	16	16	3 ICLK
0008 0028h	SYSTEM	PLL Control Register	PLLCR	16	16	3 ICLK
0008 002Ah	SYSTEM	PLL Control Register 2	PLLCR2	8	8	3 ICLK
0008 0031h	SYSTEM	Memory Wait Cycle Setting Register	MEMWAIT	8	8	3 ICLK
0008 0032h	SYSTEM	Main Clock Oscillator Control Register	MOSCCR	8	8	3 ICLK
0008 0034h	SYSTEM	Low-Speed On-Chip Oscillator Control Register	LOCOCR	8	8	3 ICLK
0008 0035h	SYSTEM	IWDT-Dedicated On-Chip Oscillator Control Register	ILOCOCR	8	8	3 ICLK
0008 0036h	SYSTEM	High-Speed On-Chip Oscillator Control Register	HOCOCR	8	8	3 ICLK
0008 0037h	SYSTEM	High-Speed On-Chip Oscillator Control Register 2	HOCOCR2	8	8	3 ICLK
0008 003Ch	SYSTEM	Oscillation Stabilization Flag Register	OSCOVFSR	8	8	3 ICLK
0008 0040h	SYSTEM	Oscillation Stop Detection Control Register	OSTDCR	8	8	3 ICLK
0008 0041h	SYSTEM	Oscillation Stop Detection Status Register	OSTDSR	8	8	3 ICLK
0008 00A0h	SYSTEM	Operating Power Control Register	OPCCR	8	8	3 ICLK
0008 00A2h	SYSTEM	Main Clock Oscillator Wait Control Register	MOSCWTCR	8	8	3 ICLK
0008 00A5h	SYSTEM	High-Speed On-Chip Oscillator Wait Control Register	HOCOWTCR	8	8	3 ICLK
0008 00C0h	SYSTEM	Reset Status Register 2	RSTSR2	8	8	3 ICLK
0008 00C2h	SYSTEM	Software Reset Register	SWRR	16	16	3 ICLK
0008 00E0h	SYSTEM	Voltage Monitoring 1 Circuit Control Register 1	LVD1CR1	8	8	3 ICLK
0008 00E1h	SYSTEM	Voltage Monitoring 1 Circuit Status Register	LVD1SR	8	8	3 ICLK
0008 00E2h	SYSTEM	Voltage Monitoring 2 Circuit Control Register 1	LVD2CR1	8	8	3 ICLK
0008 00E3h	SYSTEM	Voltage Monitoring 2 Circuit Status Register	LVD2SR	8	8	3 ICLK
0008 03FEh	SYSTEM	Protect Register	PRCR	16	16	3 ICLK
0008 1000h	FLASH	ROM Cache Enable Register	ROMCE	16	16	3 ICLK
0008 1004h	FLASH	ROM Cache Invalidate Register	ROMCIV	16	16	3 ICLK
0008 1300h	BSC	Bus Error Status Clear Register	BERCLR	8	8	2 ICLK
0008 1304h	BSC	Bus Error Monitoring Enable Register	BEREN	8	8	2 ICLK
0008 1308h	BSC	Bus Error Status Register 1	BERSR1	8	8	2 ICLK
0008 130Ah	BSC	Bus Error Status Register 2	BERSR2	16	16	2 ICLK
0008 1310h	BSC	Bus Priority Control Register	BUSPRI	16	16	2 ICLK
0008 2400h	DTC	DTC Control Register	DTCCR	8	8	2 ICLK
0008 2404h	DTC	DTC Vector Base Register	DTCVBR	32	32	2 ICLK
0008 2408h	DTC	DTC Address Mode Register	DTCADMOD	8	8	2 ICLK
0008 240Ch	DTC	DTC Module Start Register	DTCST	8	8	2 ICLK
0008 240Eh	DTC	DTC Status Register	DTCSTS	16	16	2 ICLK
0008 6400h	MPU	Region-0 Start Page Number Register	RSPAGE0	32	32	1 ICLK
0008 6404h	MPU	Region-0 End Page Number Register	REPAGE0	32	32	1 ICLK
0008 6408h	MPU	Region-1 Start Page Number Register	RSPAGE1	32	32	1 ICLK
0008 640Ch	MPU	Region-1 End Page Number Register	REPAGE1	32	32	1 ICLK
0008 6410h	MPU	Region-2 Start Page Number Register	RSPAGE2	32	32	1 ICLK
0008 6414h	MPU	Region-2 End Page Number Register	REPAGE2	32	32	1 ICLK
0008 6418h	MPU	Region-3 Start Page Number Register	RSPAGE3	32	32	1 ICLK
0008 641Ch	MPU	Region-3 End Page Number Register	REPAGE3	32	32	1 ICLK

Table 4.1 List of I/O Registers (Address Order) (4/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
0008 708Fh	ICU	Interrupt Request Register 143	IR143	8	8	2 ICLK
0008 7090h	ICU	Interrupt Request Register 144	IR144	8	8	2 ICLK
0008 7091h	ICU	Interrupt Request Register 145	IR145	8	8	2 ICLK
0008 7092h	ICU	Interrupt Request Register 146	IR146	8	8	2 ICLK
0008 7095h	ICU	Interrupt Request Register 149	IR149	8	8	2 ICLK
0008 7096h	ICU	Interrupt Request Register 150	IR150	8	8	2 ICLK
0008 7097h	ICU	Interrupt Request Register 151	IR151	8	8	2 ICLK
0008 7098h	ICU	Interrupt Request Register 152	IR152	8	8	2 ICLK
0008 7099h	ICU	Interrupt Request Register 153	IR153	8	8	2 ICLK
0008 709Fh	ICU	Interrupt Request Register 159	IR159	8	8	2 ICLK
0008 70A0h	ICU	Interrupt Request Register 160	IR160	8	8	2 ICLK
0008 70A1h	ICU	Interrupt Request Register 161	IR161	8	8	2 ICLK
0008 70A2h	ICU	Interrupt Request Register 162	IR162	8	8	2 ICLK
0008 70A3h	ICU	Interrupt Request Register 163	IR163	8	8	2 ICLK
0008 70A4h	ICU	Interrupt Request Register 164	IR164	8	8	2 ICLK
0008 70A5h	ICU	Interrupt Request Register 165	IR165	8	8	2 ICLK
0008 70A8h	ICU	Interrupt Request Register 168	IR168	8	8	2 ICLK
0008 70A9h	ICU	Interrupt Request Register 169	IR169	8	8	2 ICLK
0008 70AAh	ICU	Interrupt Request Register 170	IR170	8	8	2 ICLK
0008 70ABh	ICU	Interrupt Request Register 171	IR171	8	8	2 ICLK
0008 70ACh	ICU	Interrupt Request Register 172	IR172	8	8	2 ICLK
0008 70ADh	ICU	Interrupt Request Register 173	IR173	8	8	2 ICLK
0008 70AEh	ICU	Interrupt Request Register 174	IR174	8	8	2 ICLK
0008 70AFh	ICU	Interrupt Request Register 175	IR175	8	8	2 ICLK
0008 70B0h	ICU	Interrupt Request Register 176	IR176	8	8	2 ICLK
0008 70B1h	ICU	Interrupt Request Register 177	IR177	8	8	2 ICLK
0008 70B2h	ICU	Interrupt Request Register 178	IR178	8	8	2 ICLK
0008 70B3h	ICU	Interrupt Request Register 179	IR179	8	8	2 ICLK
0008 70B4h	ICU	Interrupt Request Register 180	IR180	8	8	2 ICLK
0008 70B5h	ICU	Interrupt Request Register 181	IR181	8	8	2 ICLK
0008 70B6h	ICU	Interrupt Request Register 182	IR182	8	8	2 ICLK
0008 70B7h	ICU	Interrupt Request Register 183	IR183	8	8	2 ICLK
0008 70B8h	ICU	Interrupt Request Register 184	IR184	8	8	2 ICLK
0008 70B9h	ICU	Interrupt Request Register 185	IR185	8	8	2 ICLK
0008 70BAh	ICU	Interrupt Request Register 186	IR186	8	8	2 ICLK
0008 70BBh	ICU	Interrupt Request Register 187	IR187	8	8	2 ICLK
0008 70BCh	ICU	Interrupt Request Register 188	IR188	8	8	2 ICLK
0008 70BDh	ICU	Interrupt Request Register 189	IR189	8	8	2 ICLK
0008 70BEh	ICU	Interrupt Request Register 190	IR190	8	8	2 ICLK
0008 70BFh	ICU	Interrupt Request Register 191	IR191	8	8	2 ICLK
0008 70C0h	ICU	Interrupt Request Register 192	IR192	8	8	2 ICLK
0008 70C1h	ICU	Interrupt Request Register 193	IR193	8	8	2 ICLK
0008 70C2h	ICU	Interrupt Request Register 194	IR194	8	8	2 ICLK
0008 70C3h	ICU	Interrupt Request Register 195	IR195	8	8	2 ICLK
0008 70C4h	ICU	Interrupt Request Register 196	IR196	8	8	2 ICLK
0008 70C5h	ICU	Interrupt Request Register 197	IR197	8	8	2 ICLK
0008 70CAh	ICU	Interrupt Request Register 202*2	IR202	8	8	2 ICLK
0008 70CBh	ICU	Interrupt Request Register 203*2	IR203	8	8	2 ICLK
0008 70CCh	ICU	Interrupt Request Register 204*2	IR204	8	8	2 ICLK
0008 70CDh	ICU	Interrupt Request Register 205*2	IR205	8	8	2 ICLK
0008 70CEh	ICU	Interrupt Request Register 206*2	IR206	8	8	2 ICLK
0008 70CFh	ICU	Interrupt Request Register 207*2	IR207	8	8	2 ICLK

Table 4.1 List of I/O Registers (Address Order) (13/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 838Fh	RSPI0	RSPI Control Register 2	SPCR2	8	8	2 or 3 PCLKB
0008 8390h	RSPI0	RSPI Command Register 0	SPCMD0	16	16	2 or 3 PCLKB
0008 8392h	RSPI0	RSPI Command Register 1	SPCMD1	16	16	2 or 3 PCLKB
0008 8394h	RSPI0	RSPI Command Register 2	SPCMD2	16	16	2 or 3 PCLKB
0008 8396h	RSPI0	RSPI Command Register 3	SPCMD3	16	16	2 or 3 PCLKB
0008 8398h	RSPI0	RSPI Command Register 4	SPCMD4	16	16	2 or 3 PCLKB
0008 839Ah	RSPI0	RSPI Command Register 5	SPCMD5	16	16	2 or 3 PCLKB
0008 839Ch	RSPI0	RSPI Command Register 6	SPCMD6	16	16	2 or 3 PCLKB
0008 839Eh	RSPI0	RSPI Command Register 7	SPCMD7	16	16	2 or 3 PCLKB
0008 9000h	S12AD	A/D Control Register	ADCSR	16	16	2 or 3 PCLKB
0008 9004h	S12AD	A/D Channel Select Register A0	ADANSA0	16	16	2 or 3 PCLKB
0008 9006h	S12AD	A/D Channel Select Register A1	ADANSA1	16	16	2 or 3 PCLKB
0008 9008h	S12AD	A/D-Converted Value Addition/Average Function Channel Select Register 0	ADADS0	16	16	2 or 3 PCLKB
0008 900Ah	S12AD	A/D-Converted Value Addition/Average Function Channel Select Register 1	ADADS1	16	16	2 or 3 PCLKB
0008 900Ch	S12AD	A/D-Converted Value Addition/Average Count Select Register	ADADC	8	8	2 or 3 PCLKB
0008 900Eh	S12AD	A/D Control Extended Register	ADCER	16	16	2 or 3 PCLKB
0008 9010h	S12AD	A/D Conversion Start Trigger Select Register	ADSTRGR	16	16	2 or 3 PCLKB
0008 9014h	S12AD	A/D Channel Select Register B0	ADANSB0	16	16	2 or 3 PCLKB
0008 9016h	S12AD	A/D Channel Select Register B1	ADANSB1	16	16	2 or 3 PCLKB
0008 9018h	S12AD	A/D Data Duplication Register	ADDBLDR	16	16	2 or 3 PCLKB
0008 901Eh	S12AD	A/D Self-Diagnosis Data Register	ADRD	16	16	2 or 3 PCLKB
0008 9020h	S12AD	A/D Data Register 0	ADDR0	16	16	2 or 3 PCLKB
0008 9022h	S12AD	A/D Data Register 1	ADDR1	16	16	2 or 3 PCLKB
0008 9024h	S12AD	A/D Data Register 2	ADDR2	16	16	2 or 3 PCLKB
0008 9026h	S12AD	A/D Data Register 3	ADDR3	16	16	2 or 3 PCLKB
0008 9040h	S12AD	A/D Data Register 16	ADDR16	16	16	2 or 3 PCLKB
0008 907Ah	S12AD	A/D Disconnection Detection Control Register	ADDISCR	8	8	2 or 3 PCLKB
0008 9080h	S12AD	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2 or 3 PCLKB
0008 9084h	S12AD	A/D Data Duplication Register A	ADDBLDRA	16	16	2 or 3 PCLKB
0008 9086h	S12AD	A/D Data Duplication Register B	ADDBLDRB	16	16	2 or 3 PCLKB
0008 90D4h	S12AD	A/D Channel Select Register C0	ADANSC0	16	16	2 or 3 PCLKB
0008 90D6h	S12AD	A/D Channel Select Register C1	ADANSC1	16	16	2 or 3 PCLKB
0008 90D9h	S12AD	A/D Group C Trigger Select Register	ADGCTRGR	8	8	2 or 3 PCLKB
0008 90DDh	S12AD	A/D Sampling State Register L	ADSSTRL	8	8	2 or 3 PCLKB
0008 90E0h	S12AD	A/D Sampling State Register 0	ADSSTR0	8	8	2 or 3 PCLKB
0008 90E1h	S12AD	A/D Sampling State Register 1	ADSSTR1	8	8	2 or 3 PCLKB
0008 90E2h	S12AD	A/D Sampling State Register 2	ADSSTR2	8	8	2 or 3 PCLKB
0008 90E3h	S12AD	A/D Sampling State Register 3	ADSSTR3	8	8	2 or 3 PCLKB
0008 91A0h	S12AD	A/D Programmable Gain Amplifier Control Register	ADPGACR	16	16	2 or 3 PCLKB
0008 91A2h	S12AD	A/D Programmable Gain Amplifier Gain Setting Register 0	ADPGAGS0	16	16	2 or 3 PCLKB
0008 9200h	S12AD1	A/D Control Register	ADCSR	16	16	2 or 3 PCLKB
0008 9204h	S12AD1	A/D Channel Select Register A0	ADANSA0	16	16	2 or 3 PCLKB
0008 9206h	S12AD1	A/D Channel Select Register A1	ADANSA1	16	16	2 or 3 PCLKB
0008 9208h	S12AD1	A/D-Converted Value Addition/Average Function Channel Select Register 0	ADADS0	16	16	2 or 3 PCLKB
0008 920Ah	S12AD1	A/D-Converted Value Addition/Average Function Channel Select Register 1	ADADS1	16	16	2 or 3 PCLKB
0008 920Ch	S12AD1	A/D-Converted Value Addition/Average Count Select Register	ADADC	8	8	2 or 3 PCLKB
0008 920Eh	S12AD1	A/D Control Extended Register	ADCER	16	16	2 or 3 PCLKB
0008 9210h	S12AD1	A/D Conversion Start Trigger Select Register	ADSTRGR	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (14/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 9214h	S12AD1	A/D Channel Select Register B0	ADANSB0	16	16	2 or 3 PCLKB
0008 9216h	S12AD1	A/D Channel Select Register B1	ADANSB1	16	16	2 or 3 PCLKB
0008 9218h	S12AD1	A/D Data Duplication Register	ADDBLDR	16	16	2 or 3 PCLKB
0008 921Eh	S12AD1	A/D Self-Diagnosis Data Register	ADRD	16	16	2 or 3 PCLKB
0008 9220h	S12AD1	A/D Data Register 0	ADDR0	16	16	2 or 3 PCLKB
0008 9222h	S12AD1	A/D Data Register 1	ADDR1	16	16	2 or 3 PCLKB
0008 9224h	S12AD1	A/D Data Register 2	ADDR2	16	16	2 or 3 PCLKB
0008 9226h	S12AD1	A/D Data Register 3	ADDR3	16	16	2 or 3 PCLKB
0008 9240h	S12AD1	A/D Data Register 16	ADDR16	16	16	2 or 3 PCLKB
0008 9266h	S12AD1	A/D Sample-and-hold Circuit Control Register	ADSHCR	16	16	2 or 3 PCLKB
0008 927Ah	S12AD1	A/D Disconnection Detection Control Register	ADDISCR	8	8	2 or 3 PCLKB
0008 9280h	S12AD1	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2 or 3 PCLKB
0008 9284h	S12AD1	A/D Data Duplication Register A	ADDBLDRA	16	16	2 or 3 PCLKB
0008 9286h	S12AD1	A/D Data Duplication Register B	ADDBLDRB	16	16	2 or 3 PCLKB
0008 92D4h	S12AD1	A/D Channel Select Register C0	ADANSC0	16	16	2 or 3 PCLKB
0008 92D6h	S12AD1	A/D Channel Select Register C1	ADANSC1	16	16	2 or 3 PCLKB
0008 92D9h	S12AD1	A/D Group C Trigger Select Register	ADGCTRGR	8	8	2 or 3 PCLKB
0008 92DDh	S12AD1	A/D Sampling State Register L	ADSSTRL	8	8	2 or 3 PCLKB
0008 92E0h	S12AD1	A/D Sampling State Register 0	ADSSTR0	8	8	2 or 3 PCLKB
0008 92E1h	S12AD1	A/D Sampling State Register 1	ADSSTR1	8	8	2 or 3 PCLKB
0008 92E2h	S12AD1	A/D Sampling State Register 2	ADSSTR2	8	8	2 or 3 PCLKB
0008 92E3h	S12AD1	A/D Sampling State Register 3	ADSSTR3	8	8	2 or 3 PCLKB
0008 93A0h	S12AD1	A/D Programmable Gain Amplifier Control Register	ADPGACR	16	16	2 or 3 PCLKB
0008 93A2h	S12AD1	A/D Programmable Gain Amplifier Gain Setting Register 0	ADPGAGS0	16	16	2 or 3 PCLKB
0008 9400h	S12AD2	A/D Control Register	ADCSR	16	16	2 or 3 PCLKB
0008 9404h	S12AD2	A/D Channel Select Register A0	ADANSA0	16	16	2 or 3 PCLKB
0008 9408h	S12AD2	A/D-Converted Value Addition/Average Function Channel Select Register 0	ADADS0	16	16	2 or 3 PCLKB
0008 940Ch	S12AD2	A/D-Converted Value Addition/Average Count Select Register	ADADC	8	8	2 or 3 PCLKB
0008 940Eh	S12AD2	A/D Control Extended Register	ADCER	16	16	2 or 3 PCLKB
0008 9410h	S12AD2	A/D Conversion Start Trigger Select Register	ADSTRGR	16	16	2 or 3 PCLKB
0008 9412h	S12AD2	A/D Conversion Extended Input Control Register	ADEXICR	16	16	2 or 3 PCLKB
0008 9414h	S12AD2	A/D Channel Select Register B0	ADANSB0	16	16	2 or 3 PCLKB
0008 9418h	S12AD2	A/D Data Duplication Register	ADDBLDR	16	16	2 or 3 PCLKB
0008 941Ch	S12AD2	A/D Internal Reference Voltage Data Register	ADOCDR	16	16	2 or 3 PCLKB
0008 941Eh	S12AD2	A/D Self-Diagnosis Data Register	ADRD	16	16	2 or 3 PCLKB
0008 9420h	S12AD2	A/D Data Register 0	ADDR0	16	16	2 or 3 PCLKB
0008 9422h	S12AD2	A/D Data Register 1	ADDR1	16	16	2 or 3 PCLKB
0008 9424h	S12AD2	A/D Data Register 2	ADDR2	16	16	2 or 3 PCLKB
0008 9426h	S12AD2	A/D Data Register 3	ADDR3	16	16	2 or 3 PCLKB
0008 9428h	S12AD2	A/D Data Register 4	ADDR4	16	16	2 or 3 PCLKB
0008 942Ah	S12AD2	A/D Data Register 5	ADDR5	16	16	2 or 3 PCLKB
0008 942Ch	S12AD2	A/D Data Register 6	ADDR6	16	16	2 or 3 PCLKB
0008 942Eh	S12AD2	A/D Data Register 7	ADDR7	16	16	2 or 3 PCLKB
0008 9430h	S12AD2	A/D Data Register 8	ADDR8	16	16	2 or 3 PCLKB
0008 9432h	S12AD2	A/D Data Register 9	ADDR9	16	16	2 or 3 PCLKB
0008 9434h	S12AD2	A/D Data Register 10	ADDR10	16	16	2 or 3 PCLKB
0008 9436h	S12AD2	A/D Data Register 11	ADDR11	16	16	2 or 3 PCLKB
0008 947Ah	S12AD2	A/D Disconnection Detection Control Register	ADDISCR	8	8	2 or 3 PCLKB
0008 9480h	S12AD2	A/D Group Scan Priority Control Register	ADGSPCR	16	16	2 or 3 PCLKB
0008 9484h	S12AD2	A/D Data Duplication Register A	ADDBLDRA	16	16	2 or 3 PCLKB
0008 9486h	S12AD2	A/D Data Duplication Register B	ADDBLDRB	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (18/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 C09Ah	PORTD	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C09Bh	PORTD	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C09Ch	PORTE	Open Drain Control Register 0	ODR0	8	8, 16	2 or 3 PCLKB
0008 C09Dh	PORTE	Open Drain Control Register 1	ODR1	8	8, 16	2 or 3 PCLKB
0008 C0C0h	PORT0	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C1h	PORT1	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C2h	PORT2	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C3h	PORT3	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C4h	PORT4	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C5h	PORT5	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C6h	PORT6	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C7h	PORT7	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C8h	PORT8	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0C9h	PORT9	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CAh	PORTA	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CBh	PORTB	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CDh	PORTD	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0CEh	PORTE	Pull-Up Control Register	PCR	8	8	2 or 3 PCLKB
0008 C0E0h	PORT0	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0E1h	PORT1	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0E2h	PORT2	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0E3h	PORT3	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0E7h	PORT7	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0E8h	PORT8	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0E9h	PORT9	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0EAh	PORTA	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0EBh	PORTB	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0EDh	PORTD	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C0EEh	PORTE	Drive Capacity Control Register	DSCR	8	8	2 or 3 PCLKB
0008 C11Fh	MPC	Write-Protect Register	PWPR	8	8	2 or 3 PCLKB
0008 C140h	MPC	P00 Pin Function Control Register	P00PFS	8	8	2 or 3 PCLKB
0008 C141h	MPC	P01 Pin Function Control Register	P01PFS	8	8	2 or 3 PCLKB
0008 C142h	MPC	P02 Pin Function Control Register	P02PFS	8	8	2 or 3 PCLKB
0008 C148h	MPC	P10 Pin Function Control Register	P10PFS	8	8	2 or 3 PCLKB
0008 C149h	MPC	P11 Pin Function Control Register	P11PFS	8	8	2 or 3 PCLKB
0008 C150h	MPC	P20 Pin Function Control Register	P20PFS	8	8	2 or 3 PCLKB
0008 C151h	MPC	P21 Pin Function Control Register	P21PFS	8	8	2 or 3 PCLKB
0008 C152h	MPC	P22 Pin Function Control Register	P22PFS	8	8	2 or 3 PCLKB
0008 C153h	MPC	P23 Pin Function Control Register	P23PFS	8	8	2 or 3 PCLKB
0008 C154h	MPC	P24 Pin Function Control Register	P24PFS	8	8	2 or 3 PCLKB
0008 C158h	MPC	P30 Pin Function Control Register	P30PFS	8	8	2 or 3 PCLKB
0008 C159h	MPC	P31 Pin Function Control Register	P31PFS	8	8	2 or 3 PCLKB
0008 C15Ah	MPC	P32 Pin Function Control Register	P32PFS	8	8	2 or 3 PCLKB
0008 C15Bh	MPC	P33 Pin Function Control Register	P33PFS	8	8	2 or 3 PCLKB
0008 C160h	MPC	P40 Pin Function Control Register	P40PFS	8	8	2 or 3 PCLKB
0008 C161h	MPC	P41 Pin Function Control Register	P41PFS	8	8	2 or 3 PCLKB
0008 C162h	MPC	P42 Pin Function Control Register	P42PFS	8	8	2 or 3 PCLKB
0008 C163h	MPC	P43 Pin Function Control Register	P43PFS	8	8	2 or 3 PCLKB
0008 C164h	MPC	P44 Pin Function Control Register	P44PFS	8	8	2 or 3 PCLKB
0008 C165h	MPC	P45 Pin Function Control Register	P45PFS	8	8	2 or 3 PCLKB
0008 C166h	MPC	P46 Pin Function Control Register	P46PFS	8	8	2 or 3 PCLKB
0008 C167h	MPC	P47 Pin Function Control Register	P47PFS	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (25/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
000A 842Ch	RSCAN	Receive Buffer Register 8DL*2	RMDF28	16	16	2 or 3 PCLKB
000A 842Eh	RSCAN	Receive Rule Entry Register 11CH*2	GAFLPH11	16	16	2 or 3 PCLKB
000A 842Eh	RSCAN	Receive Buffer Register 8DH*2	RMDF38	16	16	2 or 3 PCLKB
000A 8430h	RSCAN	Receive Rule Entry Register 12AL*2	GAFLIDL12	16	16	2 or 3 PCLKB
000A 8430h	RSCAN	Receive Buffer Register 9AL*2	RMIDL9	16	16	2 or 3 PCLKB
000A 8432h	RSCAN	Receive Rule Entry Register 12AH*2	GAFLIDH12	16	16	2 or 3 PCLKB
000A 8432h	RSCAN	Receive Buffer Register 9AH*2	RMIDH9	16	16	2 or 3 PCLKB
000A 8434h	RSCAN	Receive Rule Entry Register 12BL*2	GAFLML12	16	16	2 or 3 PCLKB
000A 8434h	RSCAN	Receive Buffer Register 9BL*2	RMTS9	16	16	2 or 3 PCLKB
000A 8436h	RSCAN	Receive Rule Entry Register 12BH*2	GAFLMH12	16	16	2 or 3 PCLKB
000A 8436h	RSCAN	Receive Buffer Register 9BH*2	RMPTR9	16	16	2 or 3 PCLKB
000A 8438h	RSCAN	Receive Rule Entry Register 12CL*2	GAFLPL12	16	16	2 or 3 PCLKB
000A 8438h	RSCAN	Receive Buffer Register 9CL*2	RMDF09	16	16	2 or 3 PCLKB
000A 843Ah	RSCAN	Receive Rule Entry Register 12CH*2	GAFLPH12	16	16	2 or 3 PCLKB
000A 843Ah	RSCAN	Receive Buffer Register 9CH*2	RMDF19	16	16	2 or 3 PCLKB
000A 843Ch	RSCAN	Receive Rule Entry Register 13AL*2	GAFLIDL13	16	16	2 or 3 PCLKB
000A 843Ch	RSCAN	Receive Buffer Register 9DL*2	RMDF29	16	16	2 or 3 PCLKB
000A 843Eh	RSCAN	Receive Rule Entry Register 13AH*2	GAFLIDH13	16	16	2 or 3 PCLKB
000A 843Eh	RSCAN	Receive Buffer Register 9DH*2	RMDF39	16	16	2 or 3 PCLKB
000A 8440h	RSCAN	Receive Rule Entry Register 13BL*2	GAFLML13	16	16	2 or 3 PCLKB
000A 8440h	RSCAN	Receive Buffer Register 10AL*2	RMIDL10	16	16	2 or 3 PCLKB
000A 8442h	RSCAN	Receive Rule Entry Register 13BH*2	GAFLMH13	16	16	2 or 3 PCLKB
000A 8442h	RSCAN	Receive Buffer Register 10AH*2	RMIDH10	16	16	2 or 3 PCLKB
000A 8444h	RSCAN	Receive Rule Entry Register 13CL*2	GAFLPL13	16	16	2 or 3 PCLKB
000A 8444h	RSCAN	Receive Buffer Register 10BL*2	RMTS10	16	16	2 or 3 PCLKB
000A 8446h	RSCAN	Receive Rule Entry Register 13CH*2	GAFLPH13	16	16	2 or 3 PCLKB
000A 8446h	RSCAN	Receive Buffer Register 10BH*2	RMPTR10	16	16	2 or 3 PCLKB
000A 8448h	RSCAN	Receive Rule Entry Register 14AL*2	GAFLIDL14	16	16	2 or 3 PCLKB
000A 8448h	RSCAN	Receive Buffer Register 10CL*2	RMDF010	16	16	2 or 3 PCLKB
000A 844Ah	RSCAN	Receive Rule Entry Register 14AH*2	GAFLIDH14	16	16	2 or 3 PCLKB
000A 844Ah	RSCAN	Receive Buffer Register 10CH*2	RMDF110	16	16	2 or 3 PCLKB
000A 844Ch	RSCAN	Receive Rule Entry Register 14BL*2	GAFLML14	16	16	2 or 3 PCLKB
000A 844Ch	RSCAN	Receive Buffer Register 10DL*2	RMDF210	16	16	2 or 3 PCLKB
000A 844Eh	RSCAN	Receive Rule Entry Register 14BH*2	GAFLMH14	16	16	2 or 3 PCLKB
000A 844Eh	RSCAN	Receive Buffer Register 10DH*2	RMDF310	16	16	2 or 3 PCLKB
000A 8450h	RSCAN	Receive Rule Entry Register 14CL*2	GAFLPL14	16	16	2 or 3 PCLKB
000A 8450h	RSCAN	Receive Buffer Register 11AL*2	RMIDL11	16	16	2 or 3 PCLKB
000A 8452h	RSCAN	Receive Rule Entry Register 14CH*2	GAFLPH14	16	16	2 or 3 PCLKB
000A 8452h	RSCAN	Receive Buffer Register 11AH*2	RMIDH11	16	16	2 or 3 PCLKB
000A 8454h	RSCAN	Receive Rule Entry Register 15AL*2	GAFLIDL15	16	16	2 or 3 PCLKB
000A 8454h	RSCAN	Receive Buffer Register 11BL*2	RMTS11	16	16	2 or 3 PCLKB
000A 8456h	RSCAN	Receive Rule Entry Register 15AH*2	GAFLIDH15	16	16	2 or 3 PCLKB
000A 8456h	RSCAN	Receive Buffer Register 11BH*2	RMPTR11	16	16	2 or 3 PCLKB
000A 8458h	RSCAN	Receive Rule Entry Register 15BL*2	GAFLML15	16	16	2 or 3 PCLKB
000A 8458h	RSCAN	Receive Buffer Register 11CL*2	RMDF011	16	16	2 or 3 PCLKB
000A 845Ah	RSCAN	Receive Rule Entry Register 15BH*2	GAFLMH15	16	16	2 or 3 PCLKB
000A 845Ah	RSCAN	Receive Buffer Register 11CH*2	RMDF111	16	16	2 or 3 PCLKB
000A 845Ch	RSCAN	Receive Rule Entry Register 15CL*2	GAFLPL15	16	16	2 or 3 PCLKB
000A 845Ch	RSCAN	Receive Buffer Register 11DL*2	RMDF211	16	16	2 or 3 PCLKB
000A 845Eh	RSCAN	Receive Rule Entry Register 15CH*2	GAFLPH15	16	16	2 or 3 PCLKB
000A 845Eh	RSCAN	Receive Buffer Register 11DH*2	RMDF311	16	16	2 or 3 PCLKB
000A 8460h	RSCAN	Receive Buffer Register 12AL*2	RMIDL12	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (31/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
000C 15A0h	MTU9	Timer General Register E	TGRE	16	16, 32	4 or 5 PCLKA
000C 15A2h	MTU9	Timer General Register F	TGRF	16	16	4 or 5 PCLKA
000C 15A4h	MTU9	Timer Interrupt Enable Register 2	TIER2	8	8, 16	4 or 5 PCLKA
000C 15A6h	MTU9	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	4 or 5 PCLKA
000C 15A8h	MTU9	Timer Control Register 2	TCR2	8	8	4 or 5 PCLKA
000C 1A00h	MTU6	Timer Control Register	TCR	8	8, 16, 32	4 or 5 PCLKA
000C 1A01h	MTU7	Timer Control Register	TCR	8	8	4 or 5 PCLKA
000C 1A02h	MTU6	Timer Mode Register 1	TMDR1	8	8, 16	4 or 5 PCLKA
000C 1A03h	MTU7	Timer Mode Register 1	TMDR1	8	8	4 or 5 PCLKA
000C 1A04h	MTU6	Timer I/O Control Register H	TIORH	8	8, 16, 32	4 or 5 PCLKA
000C 1A05h	MTU6	Timer I/O Control Register L	TIORL	8	8	4 or 5 PCLKA
000C 1A06h	MTU7	Timer I/O Control Register H	TIORH	8	8, 16	4 or 5 PCLKA
000C 1A07h	MTU7	Timer I/O Control Register L	TIORL	8	8	4 or 5 PCLKA
000C 1A08h	MTU6	Timer Interrupt Enable Register	TIER	8	8, 16	4 or 5 PCLKA
000C 1A09h	MTU7	Timer Interrupt Enable Register	TIER	8	8	4 or 5 PCLKA
000C 1A0Ah	MTU	Timer Output Master Enable Register B	TOERB	8	8	4 or 5 PCLKA
000C 1A0Dh	MTU	Timer Gate Control Register	TGCRB	8	8	4 or 5 PCLKA
000C 1A0Eh	MTU	Timer Output Control Register 1B	TOCR1B	8	8, 16	4 or 5 PCLKA
000C 1A0Fh	MTU	Timer Output Control Register 2B	TOCR2B	8	8	4 or 5 PCLKA
000C 1A10h	MTU6	Timer Counter	TCNT	16	16, 32	4 or 5 PCLKA
000C 1A12h	MTU7	Timer Counter	TCNT	16	16	4 or 5 PCLKA
000C 1A14h	MTU	Timer Period Data Register B	TCDRB	16	16, 32	4 or 5 PCLKA
000C 1A16h	MTU	Timer Dead Time Data Register B	TDDRB	16	16	4 or 5 PCLKA
000C 1A18h	MTU6	Timer General Register A	TGRA	16	16, 32	4 or 5 PCLKA
000C 1A1Ah	MTU6	Timer General Register B	TGRB	16	16	4 or 5 PCLKA
000C 1A1Ch	MTU7	Timer General Register A	TGRA	16	16, 32	4 or 5 PCLKA
000C 1A1Eh	MTU7	Timer General Register B	TGRB	16	16	4 or 5 PCLKA
000C 1A20h	MTU	Timer Subcounters B	TCNTSB	16	16, 32	4 or 5 PCLKA
000C 1A22h	MTU	Timer Period Buffer Register B	TCBRB	16	16	4 or 5 PCLKA
000C 1A24h	MTU6	Timer General Register C	TGRC	16	16, 32	4 or 5 PCLKA
000C 1A26h	MTU6	Timer General Register D	TGRD	16	16	4 or 5 PCLKA
000C 1A28h	MTU7	Timer General Register C	TGRC	16	16, 32	4 or 5 PCLKA
000C 1A2Ah	MTU7	Timer General Register D	TGRD	16	16	4 or 5 PCLKA
000C 1A2Ch	MTU6	Timer Status Register	TSR	8	8, 16	4 or 5 PCLKA
000C 1A2Dh	MTU7	Timer Status Register	TSR	8	8	4 or 5 PCLKA
000C 1A30h	MTU	Timer Interrupt Skipping Set Register 1B	TITCR1B	8	8, 16	4 or 5 PCLKA
000C 1A31h	MTU	Timer Interrupt Skipping Counters 1B	TITCNT1B	8	8	4 or 5 PCLKA
000C 1A32h	MTU	Timer Buffer Transfer Set Register B	TBTERB	8	8	4 or 5 PCLKA
000C 1A34h	MTU	Timer Dead Time Enable Register B	TDERB	8	8	4 or 5 PCLKA
000C 1A36h	MTU	Timer Output Level Buffer Register B	TOLBRB	8	8	4 or 5 PCLKA
000C 1A38h	MTU6	Timer Buffer Operation Transfer Mode Register	TBTM	8	8, 16	4 or 5 PCLKA
000C 1A39h	MTU7	Timer Buffer Operation Transfer Mode Register	TBTM	8	8	4 or 5 PCLKA
000C 1A3Ah	MTU	Timer Interrupt Skipping Mode Register B	TITMRB	8	8	4 or 5 PCLKA
000C 1A3Bh	MTU	Timer Interrupt Skipping Set Register 2B	TITCR2B	8	8	4 or 5 PCLKA
000C 1A3Ch	MTU	Timer Interrupt Skipping Counters 2B	TITCNT2B	8	8	4 or 5 PCLKA
000C 1A40h	MTU7	Timer A/D Converter Start Request Control Register	TADCR	16	16	4 or 5 PCLKA
000C 1A44h	MTU7	Timer A/D Converter Start Request Cycle Set Register A	TADCORA	16	16, 32	4 or 5 PCLKA
000C 1A46h	MTU7	Timer A/D Converter Start Request Cycle Set Register B	TADCORB	16	16	4 or 5 PCLKA
000C 1A48h	MTU7	Timer A/D Converter Start Request Cycle Set Buffer Register A	TADCOBRA	16	16, 32	4 or 5 PCLKA
000C 1A4Ah	MTU7	Timer A/D Converter Start Request Cycle Set Buffer Register B	TADCOBRB	16	16	4 or 5 PCLKA
000C 1A4Ch	MTU6	Timer Control Register 2	TCR2	8	8	4 or 5 PCLKA

5.2.3 Standard I/O Pin Output Characteristics (3)

Figure 5.14 to Figure 5.17 show the output characteristics of the large current ports.

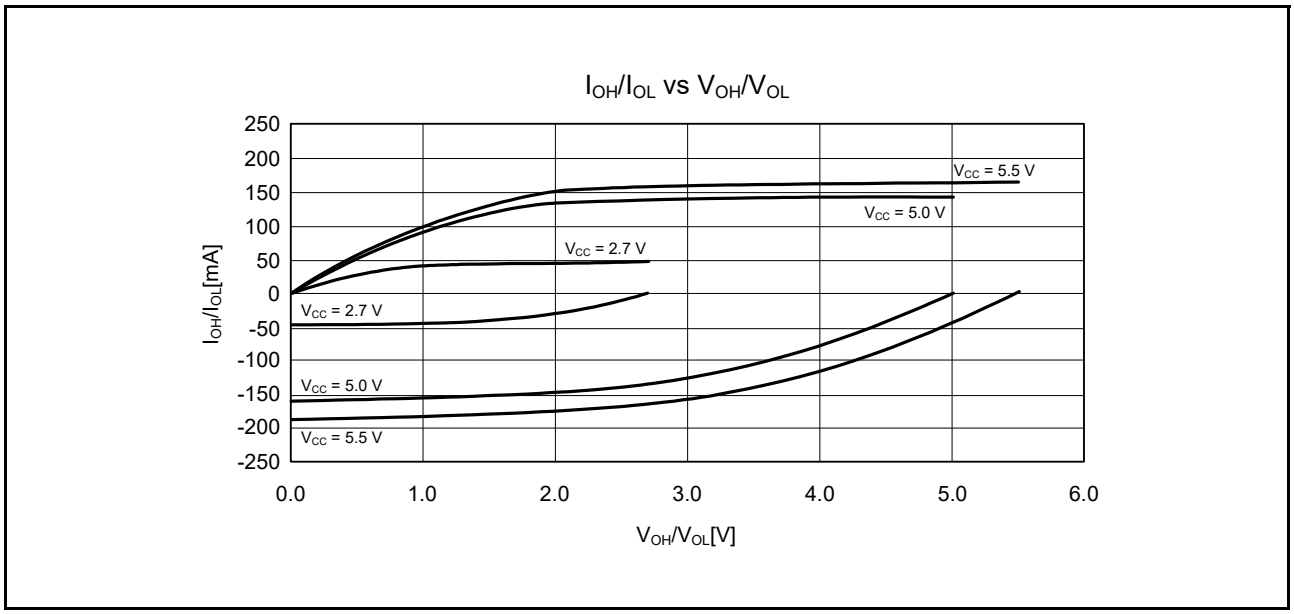


Figure 5.14 V_{OH}/V_{OL} and I_{OH}/I_{OL} Voltage Characteristics of Large Current Ports at T_a = 25°C (Reference Data)

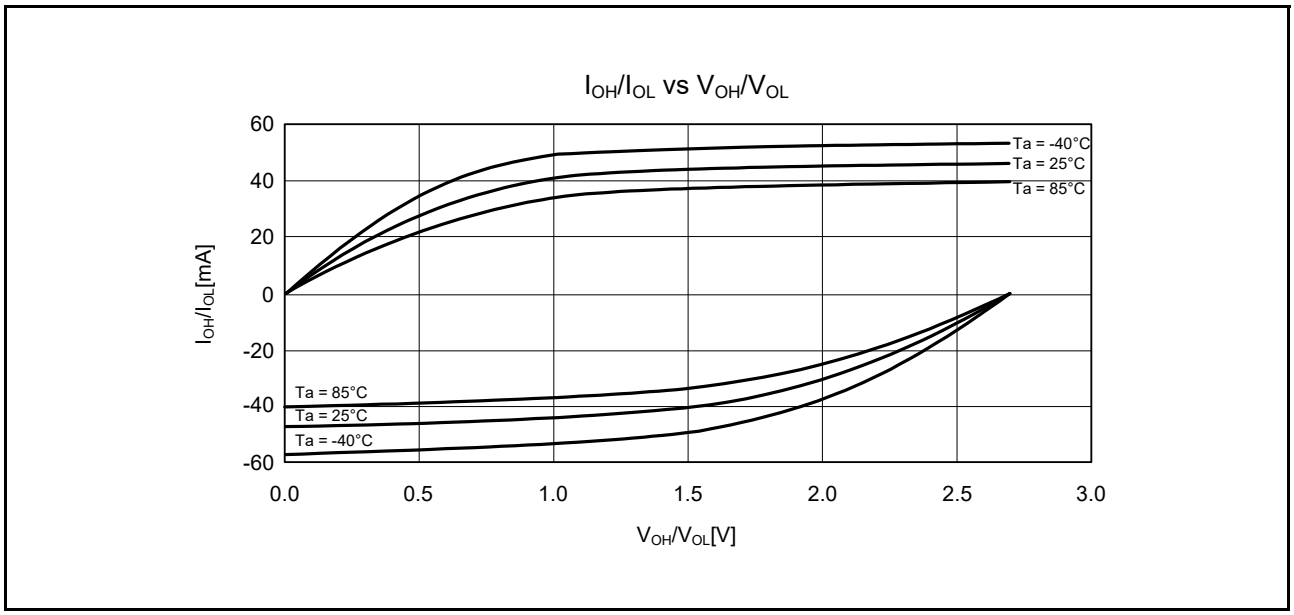


Figure 5.15 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics of Large Current Ports at VCC = 2.7 V (Reference Data)

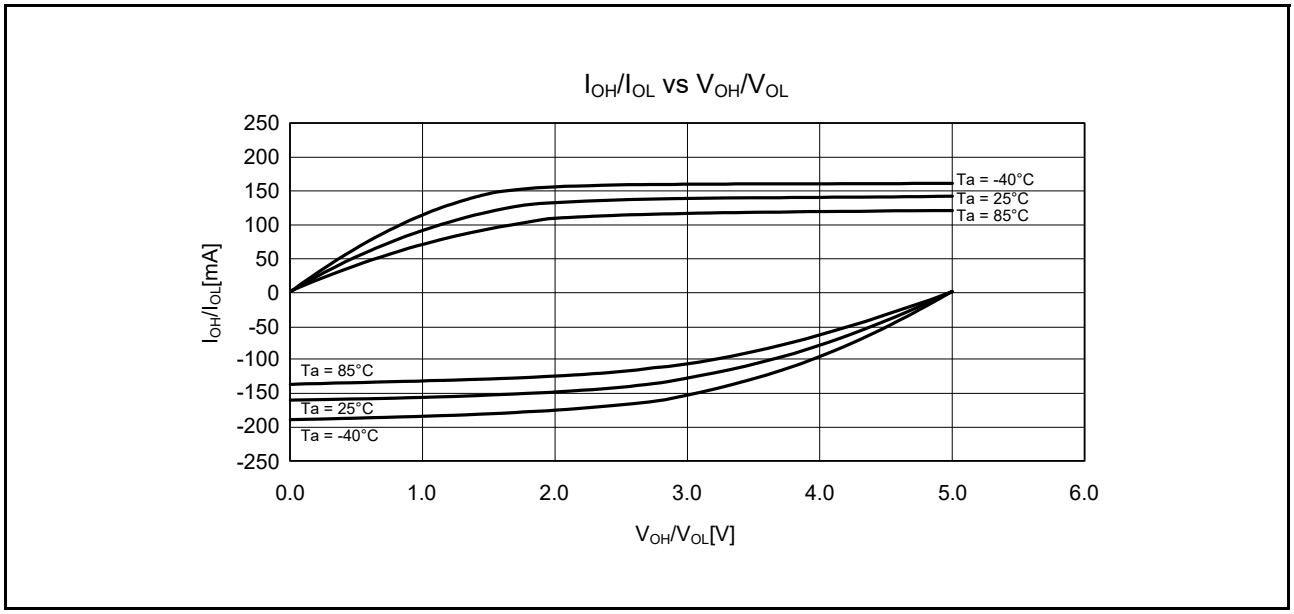


Figure 5.16 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics of Large Current Ports at VCC = 5.0 V (Reference Data)

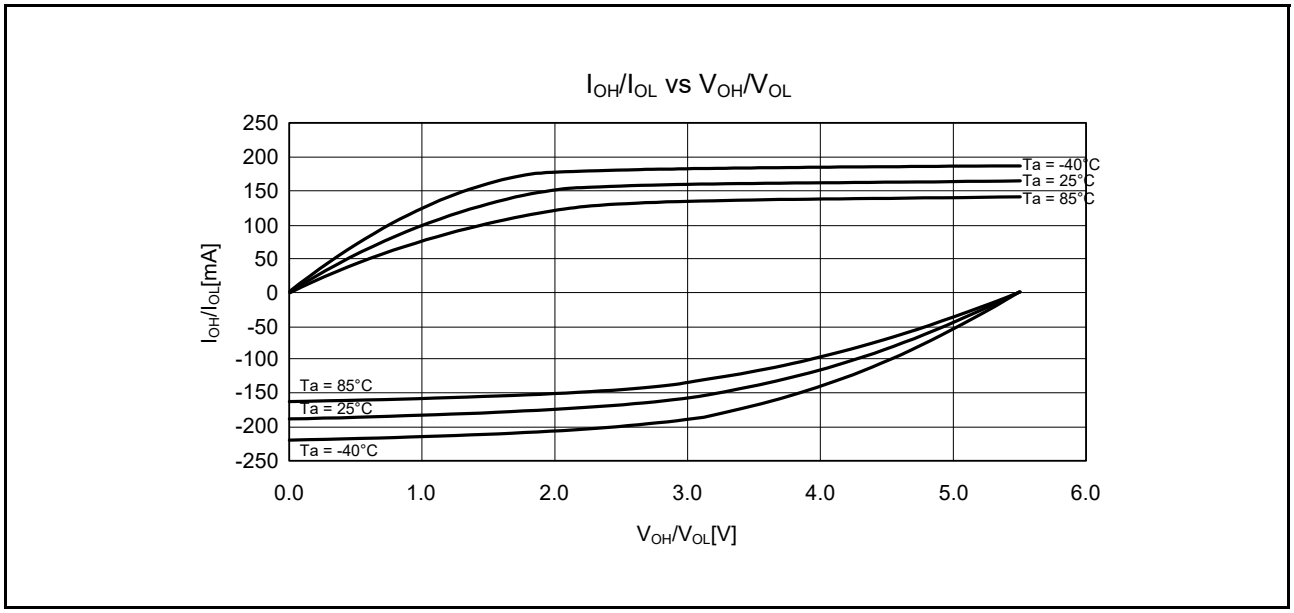


Figure 5.17 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics of Large Current Ports at VCC = 5.5 V (Reference Data)

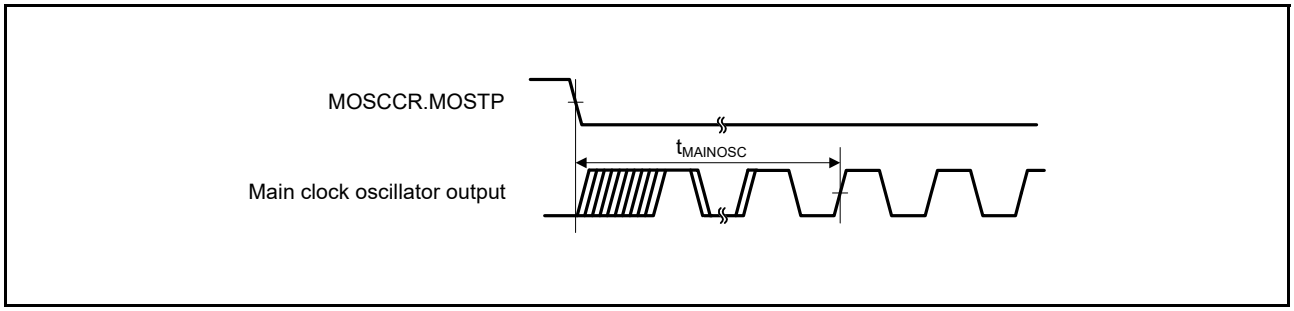


Figure 5.23 Main Clock Oscillation Start Timing

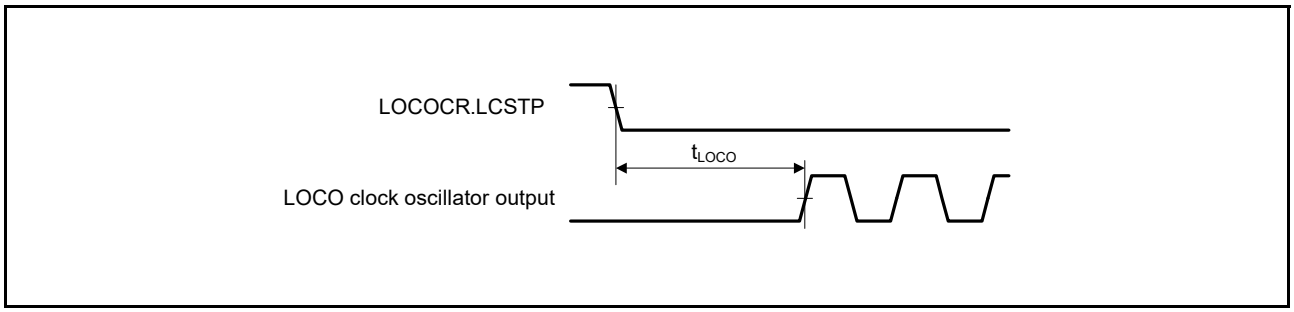


Figure 5.24 LOCO Clock Oscillation Start Timing

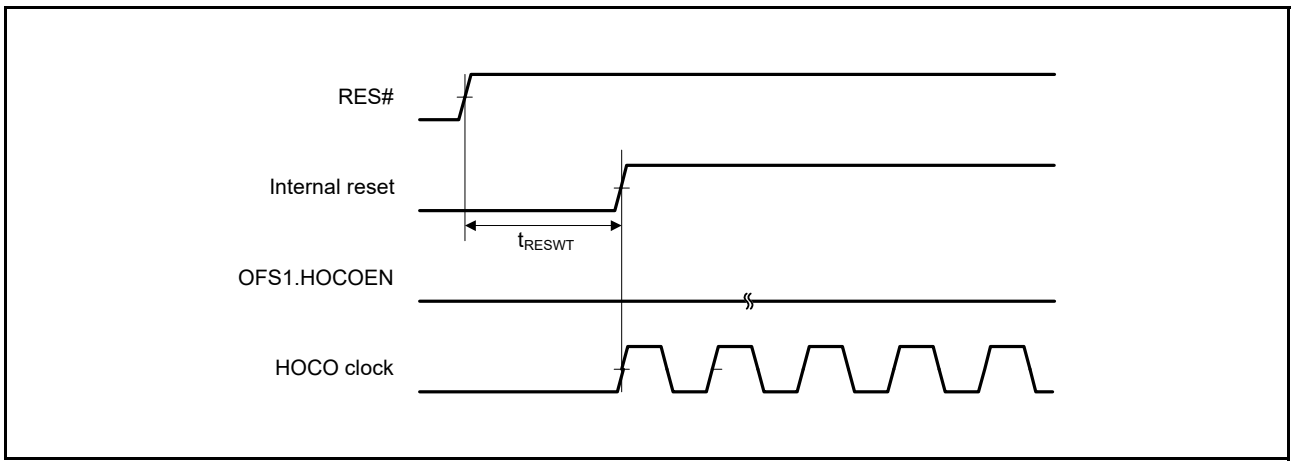


Figure 5.25 HOCO Clock Oscillation Start Timing (After Reset is Canceled by Setting OFS1.HOCOEN Bit to 0)

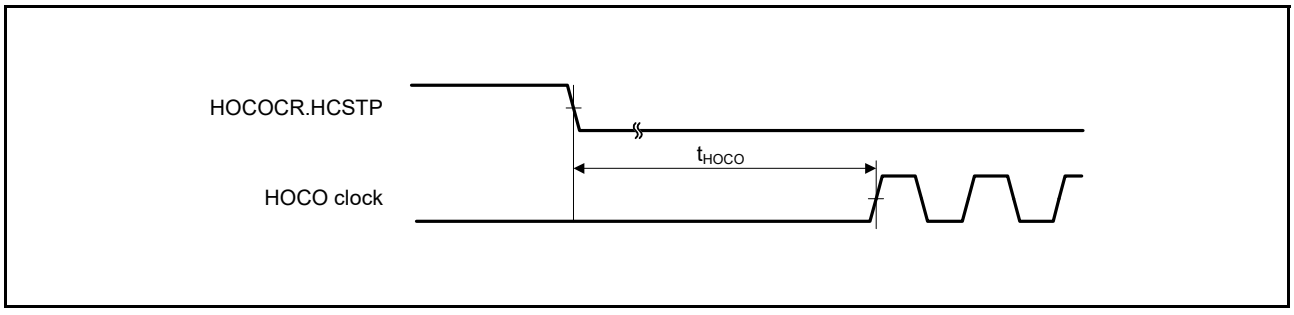


Figure 5.26 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting HOCOCR.HCSTP Bit)

5.3.5 Timing of On-Chip Peripheral Modules

Table 5.23 Timing of On-Chip Peripheral Modules (1)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item				Symbol	Min.	Max.	Unit *1	Test Conditions
I/O ports	Input data pulse width			t_{PRW}	1.5	—	t_{Pcyc}	Figure 5.36
MTU3	Input capture input pulse width		Single-edge setting	t_{TICW}	3	—	t_{PAcyc}	Figure 5.37
			Both-edge setting		5	—		
	Timer clock pulse width		Single-edge setting	t_{TCKWH}, t_{TCKWL}	3	—	t_{PAcyc}	Figure 5.38
			Both-edge setting		5	—		
			Phase counting mode		5	—		
POE3	POE# input pulse width			t_{POEW}	1.5	—	t_{Pcyc}	Figure 5.39
GPT	Input capture input pulse width		Single-edge setting	t_{GTICW}	1.5	—	t_{PAcyc}	Figure 5.40
			Both-edge setting		2.5	—		
	External trigger input pulse width		Single-edge setting	t_{GTETW}	1.5	—	t_{PAcyc}	Figure 5.41
			Both-edge setting		2.5	—		
	Timer clock pulse width			t_{GTCKWH}	1.5	—	t_{PAcyc}	Figure 5.42
				t_{GTCKWL}				
TMR	Timer clock pulse width		Single-edge setting	t_{TMCWH}, t_{TMCWL}	1.5	—	t_{Pcyc}	Figure 5.43
			Both-edge setting		2.5	—		
SCI	Input clock cycle		Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	Figure 5.44
			Clock synchronous		6	—		
	Input clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time			t_{SCKr}	—	20	ns	
	Input clock fall time			t_{SCKf}	—	20	ns	
	Output clock cycle		Asynchronous	t_{Scyc}	16	—	t_{Pcyc}	Figure 5.45
			Clock synchronous		4	—		
	Output clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time			t_{SCKr}	—	20	ns	
	Output clock fall time			t_{SCKf}	—	20	ns	
	Transmit data delay time (master)	Clock synchronous		t_{TXD}	—	40	ns	
	Transmit data delay time (slave)	Clock synchronous	VCC = 4.0 V or above		—	40	ns	
			VCC = 2.7 V or above		—	65	ns	
	Receive data setup time (master)	Clock synchronous	VCC = 4.0 V or above	t_{RXS}	40	—	ns	
			VCC = 2.7 V or above		65	—	ns	
	Receive data setup time (slave)	Clock synchronous			40	—	ns	
	Receive data hold time	Clock synchronous		t_{RXH}	40	—	ns	
A/D converter	Trigger input pulse width			t_{TRGW}	1.5	—	t_{Pcyc}	Figure 5.46
CAC	CACREF input pulse width		$t_{Pcyc} \le t_{cac}$ *2	t_{CACREF}	4.5 t_{cac} + 3 t_{Pcyc}	—	ns	
			$t_{Pcyc} > t_{cac}$ *2		5 t_{cac} + 6.5 t_{Pcyc}			

Note 1. t_{Pcyc}: PCLK cycle, t_{PAcyc}: PCLKA cycle
Note 2. t_{cac}: CAC count clock source cycle

5.4 A/D Conversion Characteristics

Table 5.28 A/D Conversion Characteristics (1)

Conditions: VCC = 4.5 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	40	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 40 MHz)	Permissible signal source impedance (Max.) = 1.0 kΩ Sample-and-hold circuit not in use	1.00	—	—	µs	High-precision channel ADSSTRn.SST[7:0] bits = 08h
		1.25	—	—	µs	Normal-precision channel ADSSTRn.SST[7:0] bits = 12h
	Permissible signal source impedance (Max.) = 1.0 kΩ Sample-and-hold circuit in use	1.65	—	—	µs	High-precision channel ADSSTRn.SST[7:0] bits = 08h ADSHCR.SSTSH[7:0] bits = 0Dh AN100 to 102 = 0.25 V to AVCC1 – 0.25 V
Analog input capacitance		—	—	12	pF	
Offset error		—	±2.0	±6.5	LSB	
Full-scale error		—	±2.0	±6.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy	Sample-and-hold circuit in use	—	±2.5	±8.0	LSB	AN100 to 102 = 0.25V to AVCC1 – 0.25
	Sample-and-hold circuit not in use	—	±3.0	±8.0	LSB	
DNL differential nonlinearity error		—	±0.5	±1.5	LSB	
INL integral nonlinearity error		—	±1.5	±4.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

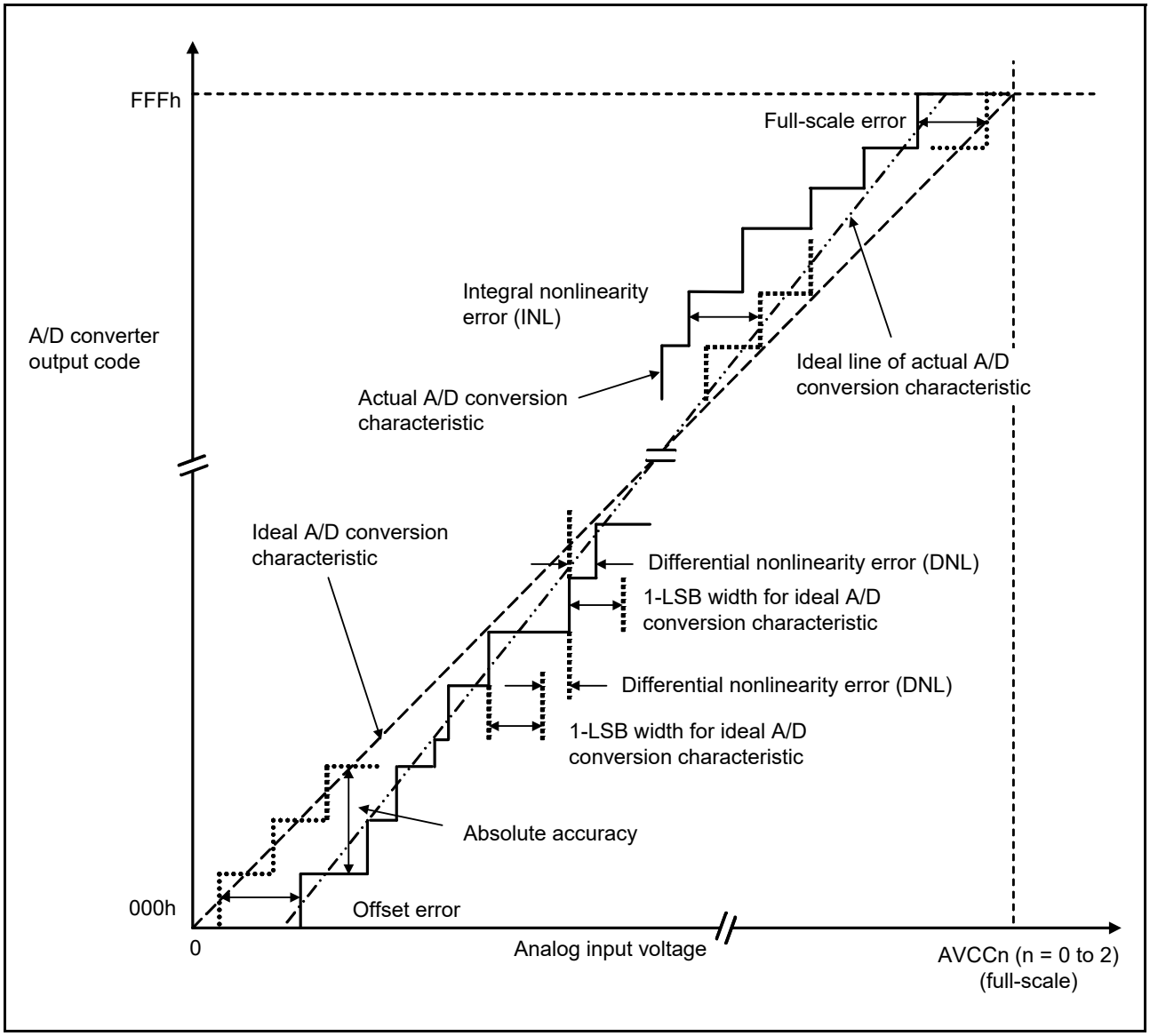


Figure 5.53 Illustration of A/D Converter Characteristic Terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and if reference voltage (AVCCn (n = 0 to 2)) is 3.072 V, then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, 1.5 mV, ... are used as analog input voltages.

If analog input voltage is 6 mV, absolute accuracy = ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh though an output code, 008h, can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

5.9 Oscillation Stop Detection Timing

Table 5.38 Oscillation Stop Detection Timing

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 =AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, Ta = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 5.60

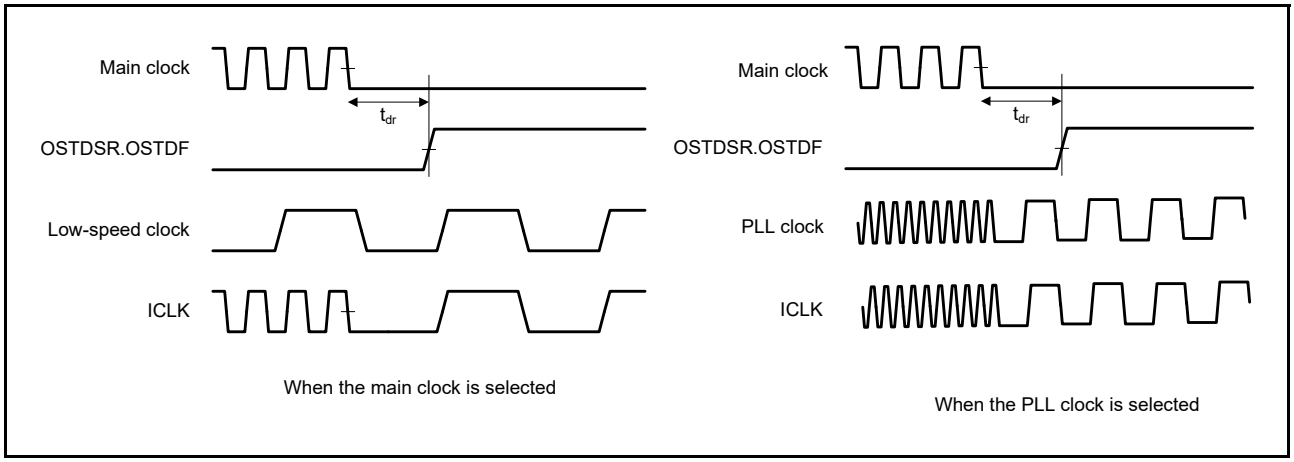


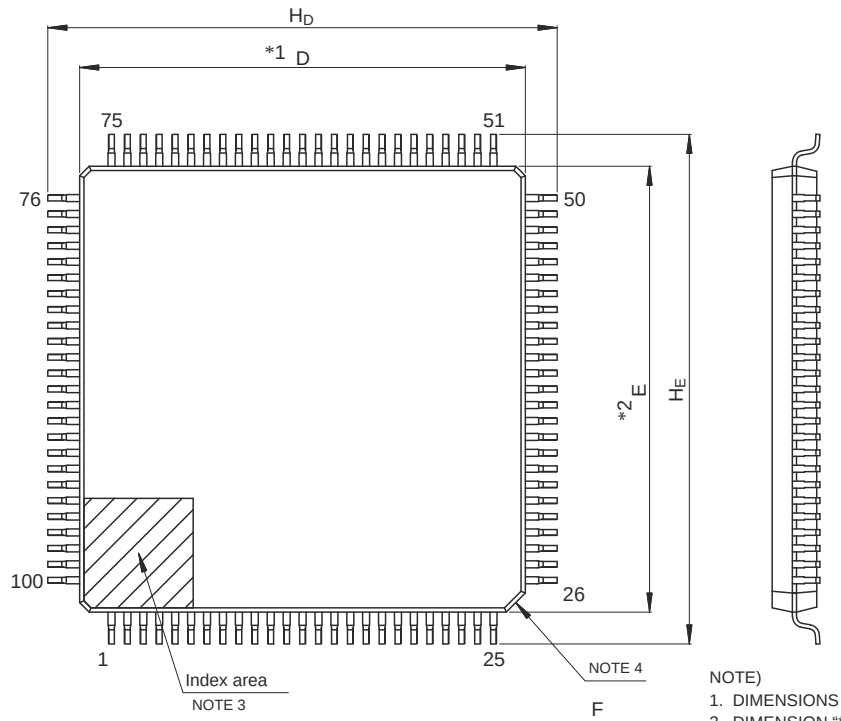
Figure 5.60 Oscillation Stop Detection Timing

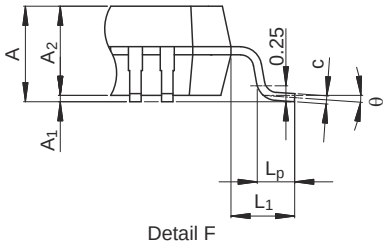
Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm



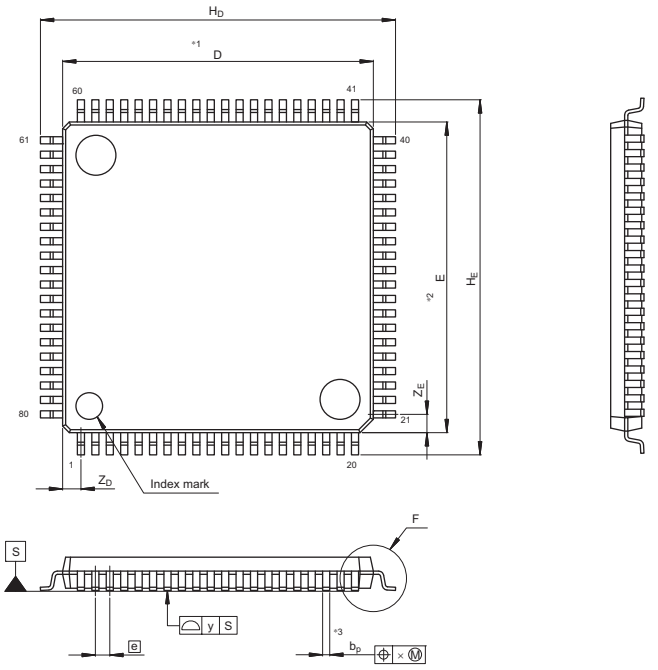


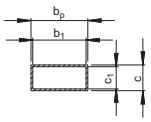
NOTE)
1. DIMENSIONS “*1” AND “*2” DO NOT INCLUDE MOLD FLASH.
2. DIMENSION “*3” DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

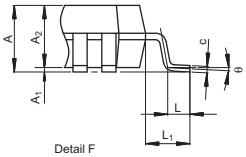
Figure A 100-Pin LFQFP (PLQP0100KB-B)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP80-14x14-0.65	PLQP0080JA-A	FP-80W / FP-80WV	0.6g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.27	0.32	0.37
b_1	—	0.30	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z_D	—	0.825	—
Z_E	—	0.825	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure B 80-Pin LQFP (PLQP0080JA-A)

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