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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RXv2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, SCI, SPI
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	80
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 22x12b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f524teadfp-31

Table 1.4 Pin Functions (4/4)

Classifications	Pin Name	I/O	Description
I/O ports	P00 to P02	I/O	3-bit input/output pins.
	P10, P11	I/O	2-bit input/output pins.
	P20 to P24	I/O	5-bit input/output pins.
	P30 to P33, P36, P37	I/O	6-bit input/output pins.
	P40 to P47	I/O	8-bit input/output pins.
	P50 to P55	I/O	6-bit input/output pins.
	P60 to P65	I/O	6-bit input/output pins.
	P70 to P76	I/O	7-bit input/output pins.
	P80 to P82	I/O	3-bit input/output pins.
	P90 to P96	I/O	7-bit input/output pins.
	PA0 to PA5	I/O	6-bit input/output pins.
	PB0 to PB7	I/O	8-bit input/output pins.
	PD0 to PD7	I/O	8-bit input/output pins.
	PE0 to PE5	I/O	6-bit input/output pins (PE2: input).

Note: When the A/D converter, D/A converter, and comparator C are not used, connect the AVCC0, AVCC1, AVCC2, and VREF pins to VCC, and connect the AVSS0, AVSS1 and AVSS2 pins to VSS, respectively.

Table 1.5 List of Pins and Pin Functions (100-Pin LFQFP, Chip Version B) (2/3)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (TMR, MTU, POE, CAC, GPT)	Communications (SCI, RSPI, RIIC, RSCAN)	Others
52		P75	MTIOC4C, MTIOC4C#, GTIOC1B, GTIOC1B#		
53		P74	MTIOC3D, MTIOC3D#, GTIOC0B, GTIOC0B#		
54		P73	MTIOC4B, MTIOC4B#, GTIOC2A, GTIOC2A#		
55		P72	MTIOC4A, MTIOC4A#, GTIOC1A, GTIOC1A#		
56		P71	MTIOC3B, MTIOC3B#, GTIOC0A, GTIOC0A#		
57		P70	POE0#		IRQ5
58		P33	MTIOC3A, MTIOC3A#, MTCLKA, MTCLKA#, TMO0	SSLA3	
59		P32	MTIOC3C, MTIOC3C#, MTCLKB, MTCLKB#, TMO6	SSLA2	
60	VCC				
61		P31	MTIOC0A, MTIOC0A#, MTCLKC, MTCLKC#, TMRI6	SSLA1	IRQ6
62	VSS				
63		P30	MTIOC0B, MTIOC0B#, MTCLKD, MTCLKD#, TMCI6	SSLA0	IRQ7, COMP3
64		P24	MTIC5U, MTIC5U#, TMCI2, TMO6	RSPCKA	COMP0, DA0
65		P23	MTIC5V, MTIC5V#, TMO2, CACREF	MOSIA	COMP1, DA1
66		P22	MTIC5W, MTIC5W#, TMRI2, TMO4	MISOA	ADTRG2#, COMP2
67		P21	MTCLKA, MTCLKA#, MTIOC9A, MTIOC9A#, TMCI4		IRQ6, ADTRG1#, AN116
68		P20	MTCLKB, MTCLKB#, MTIOC9C, MTIOC9C#, TMRI4		IRQ7, ADTRG0#, AN016
69		P65			AN205
70		P64			AN204
71	AVCC2				
72	VREF				
73	AVSS2				
74		P63			AN203, IRQ7
75		P62			AN202, IRQ6
76		P61			AN201, IRQ5
77		P60			AN200, IRQ4
78		P55			AN211, IRQ3
79		P54			AN210, IRQ2
80		P53			AN209, IRQ1
81		P52			AN208, IRQ0
82		P51			AN207
83		P50			AN206
84		P47			AN103
85		P46			AN102, CMPC12, CMPC13, CMPC30, CMPC31
86		P45			AN101, CMPC02, CMPC03, CMPC20, CMPC21
87		P44			AN100, CMPC10, CMPC11, CMPC32, CMPC33
88		P43			AN003
89		P42			AN002
90		P41			AN001
91		P40			AN000, CMPC00, CMPC01, CMPC22, CMPC23
92	AVCC1				
93	AVCC0				

Table 4.1 List of I/O Registers (Address Order) (10/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles
						ICLK ≥ PCLK
0008 73BDh	ICU	Interrupt Source Priority Register 189	IPR189	8	8	2 ICLK
0008 73C0h	ICU	Interrupt Source Priority Register 192	IPR192	8	8	2 ICLK
0008 73C3h	ICU	Interrupt Source Priority Register 195	IPR195	8	8	2 ICLK
0008 73CAh	ICU	Interrupt Source Priority Register 202*2	IPR202	8	8	2 ICLK
0008 73CBh	ICU	Interrupt Source Priority Register 203*2	IPR203	8	8	2 ICLK
0008 73CCh	ICU	Interrupt Source Priority Register 204*2	IPR204	8	8	2 ICLK
0008 73CDh	ICU	Interrupt Source Priority Register 205*2	IPR205	8	8	2 ICLK
0008 73CEh	ICU	Interrupt Source Priority Register 206*2	IPR206	8	8	2 ICLK
0008 73CFh	ICU	Interrupt Source Priority Register 207*2	IPR207	8	8	2 ICLK
0008 73D0h	ICU	Interrupt Source Priority Register 208*2	IPR208	8	8	2 ICLK
0008 73D1h	ICU	Interrupt Source Priority Register 209*2	IPR209	8	8	2 ICLK
0008 73D2h	ICU	Interrupt Source Priority Register 210*2	IPR210	8	8	2 ICLK
0008 73D3h	ICU	Interrupt Source Priority Register 211*2	IPR211	8	8	2 ICLK
0008 73D4h	ICU	Interrupt Source Priority Register 212*2	IPR212	8	8	2 ICLK
0008 73D5h	ICU	Interrupt Source Priority Register 213*2	IPR213	8	8	2 ICLK
0008 73D6h	ICU	Interrupt Source Priority Register 214*2	IPR214	8	8	2 ICLK
0008 73D7h	ICU	Interrupt Source Priority Register 215*2	IPR215	8	8	2 ICLK
0008 73D8h	ICU	Interrupt Source Priority Register 216*2	IPR216	8	8	2 ICLK
0008 73D9h	ICU	Interrupt Source Priority Register 217*2	IPR217	8	8	2 ICLK
0008 73DAh	ICU	Interrupt Source Priority Register 218	IPR218	8	8	2 ICLK
0008 73DEh	ICU	Interrupt Source Priority Register 222	IPR222	8	8	2 ICLK
0008 73E2h	ICU	Interrupt Source Priority Register 226	IPR226	8	8	2 ICLK
0008 73EEh	ICU	Interrupt Source Priority Register 238*2	IPR238	8	8	2 ICLK
0008 73EFh	ICU	Interrupt Source Priority Register 239*2	IPR239	8	8	2 ICLK
0008 73F0h	ICU	Interrupt Source Priority Register 240*2	IPR240	8	8	2 ICLK
0008 73F1h	ICU	Interrupt Source Priority Register 241*2	IPR241	8	8	2 ICLK
0008 73F2h	ICU	Interrupt Source Priority Register 242*2	IPR242	8	8	2 ICLK
0008 73F3h	ICU	Interrupt Source Priority Register 243*2	IPR243	8	8	2 ICLK
0008 73F4h	ICU	Interrupt Source Priority Register 244*2	IPR244	8	8	2 ICLK
0008 73F6h	ICU	Interrupt Source Priority Register 246	IPR246	8	8	2 ICLK
0008 73F7h	ICU	Interrupt Source Priority Register 247	IPR247	8	8	2 ICLK
0008 73F8h	ICU	Interrupt Source Priority Register 248	IPR248	8	8	2 ICLK
0008 73F9h	ICU	Interrupt Source Priority Register 249	IPR249	8	8	2 ICLK
0008 7500h	ICU	IRQ Control Register 0	IRQCR0	8	8	2 ICLK
0008 7501h	ICU	IRQ Control Register 1	IRQCR1	8	8	2 ICLK
0008 7502h	ICU	IRQ Control Register 2	IRQCR2	8	8	2 ICLK
0008 7503h	ICU	IRQ Control Register 3	IRQCR3	8	8	2 ICLK
0008 7504h	ICU	IRQ Control Register 4	IRQCR4	8	8	2 ICLK
0008 7505h	ICU	IRQ Control Register 5	IRQCR5	8	8	2 ICLK
0008 7506h	ICU	IRQ Control Register 6	IRQCR6	8	8	2 ICLK
0008 7507h	ICU	IRQ Control Register 7	IRQCR7	8	8	2 ICLK
0008 7510h	ICU	IRQ Pin Digital Filter Enable Register 0	IRQFLTE0	8	8	2 ICLK
0008 7514h	ICU	IRQ Pin Digital Filter Setting Register 0	IRQFLTC0	16	16	2 ICLK
0008 7580h	ICU	Non-Maskable Interrupt Status Register	NMISR	8	8	2 ICLK
0008 7581h	ICU	Non-Maskable Interrupt Enable Register	NMIER	8	8	2 ICLK
0008 7582h	ICU	Non-Maskable Interrupt Status Clear Register	NMICLR	8	8	2 ICLK
0008 7583h	ICU	NMI Pin Interrupt Control Register	NMICR	8	8	2 ICLK
0008 7590h	ICU	NMI Pin Digital Filter Enable Register	NMIFLTE	8	8	2 ICLK
0008 7594h	ICU	NMI Pin Digital Filter Setting Register	NMIFLTC	8	8	2 ICLK
0008 8000h	CMT	Compare Match Timer Start Register 0	CMSTR0	16	16	2 or 3 PCLKB
0008 8002h	CMT0	Compare Match Timer Control Register	CMCR	16	16	2 or 3 PCLKB
0008 8004h	CMT0	Compare Match Counter	CMCNT	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (16/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
0008 A0AFh	SCI5	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB
0008 A0B0h	SCI5	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB
0008 A0B0h	SCI5	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB
0008 A0B1h	SCI5	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB
0008 A0B2h	SCI5	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB
0008 A0C0h	SCI6	Serial Mode Register	SMR	8	8	2 or 3 PCLKB
0008 A0C1h	SCI6	Bit Rate Register	BRR	8	8	2 or 3 PCLKB
0008 A0C2h	SCI6	Serial Control Register	SCR	8	8	2 or 3 PCLKB
0008 A0C3h	SCI6	Transmit Data Register	TDR	8	8	2 or 3 PCLKB
0008 A0C4h	SCI6	Serial Status Register	SSR	8	8	2 or 3 PCLKB
0008 A0C5h	SCI6	Receive Data Register	RDR	8	8	2 or 3 PCLKB
0008 A0C6h	SMCI6	Smart Card Mode Register	SCMR	8	8	2 or 3 PCLKB
0008 A0C7h	SCI6	Serial Extended Mode Register	SEMR	8	8	2 or 3 PCLKB
0008 A0C8h	SCI6	Noise Filter Setting Register	SNFR	8	8	2 or 3 PCLKB
0008 A0C9h	SCI6	I^2C Mode Register 1	SIMR1	8	8	2 or 3 PCLKB
0008 A0CAh	SCI6	I^2C Mode Register 2	SIMR2	8	8	2 or 3 PCLKB
0008 A0CBh	SCI6	I^2C Mode Register 3	SIMR3	8	8	2 or 3 PCLKB
0008 A0CCh	SCI6	I^2C Status Register	SISR	8	8	2 or 3 PCLKB
0008 A0CDh	SCI6	SPI Mode Register	SPMR	8	8	2 or 3 PCLKB
0008 A0CEh	SCI6	Transmit Data Register HL	TDRHL	16	16	4 or 5 PCLKB
0008 A0CEh	SCI6	Transmit Data Register H	TDRH	8	8	2 or 3 PCLKB
0008 A0CFh	SCI6	Transmit Data Register L	TDRL	8	8	2 or 3 PCLKB
0008 A0D0h	SCI6	Receive Data Register HL	RDRHL	16	16	4 or 5 PCLKB
0008 A0D0h	SCI6	Receive Data Register H	RDRH	8	8	2 or 3 PCLKB
0008 A0D1h	SCI6	Receive Data Register L	RDRL	8	8	2 or 3 PCLKB
0008 A0D2h	SCI6	Modulation Duty Register	MDDR	8	8	2 or 3 PCLKB
0008 B000h	CAC	CAC Control Register 0	CACR0	8	8	2 or 3 PCLKB
0008 B001h	CAC	CAC Control Register 1	CACR1	8	8	2 or 3 PCLKB
0008 B002h	CAC	CAC Control Register 2	CACR2	8	8	2 or 3 PCLKB
0008 B003h	CAC	CAC Interrupt Request Enable Register	CAICR	8	8	2 or 3 PCLKB
0008 B004h	CAC	CAC Status Register	CASTR	8	8	2 or 3 PCLKB
0008 B006h	CAC	CAC Upper-Limit Value Setting Register	CAULVR	16	16	2 or 3 PCLKB
0008 B008h	CAC	CAC Lower-Limit Value Setting Register	CALLVR	16	16	2 or 3 PCLKB
0008 B00Ah	CAC	CAC Counter Buffer Register	CACNTBR	16	16	2 or 3 PCLKB
0008 B080h	DOC	DOC Control Register	DOCR	8	8	2 or 3 PCLKB
0008 B082h	DOC	DOC Data Input Register	DODIR	16	16	2 or 3 PCLKB
0008 B084h	DOC	DOC Data Setting Register	DODSR	16	16	2 or 3 PCLKB
0008 C000h	PORT0	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C001h	PORT1	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C002h	PORT2	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C003h	PORT3	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C004h	PORT4	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C005h	PORT5	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C006h	PORT6	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C007h	PORT7	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C008h	PORT8	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C009h	PORT9	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Ah	PORTA	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Bh	PORTB	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Dh	PORTD	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C00Eh	PORTE	Port Direction Register	PDR	8	8	2 or 3 PCLKB
0008 C020h	PORT0	Port Output Data Register	PODR	8	8	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (22/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
000A 836Dh	RSCAN0	Transmit Buffer Status Register 1*2	TMSTS1	8	8	1 or 2 PCLKB
000A 836Eh	RSCAN0	Transmit Buffer Status Register 2*2	TMSTS2	8	8	1 or 2 PCLKB
000A 836Fh	RSCAN0	Transmit Buffer Status Register 3*2	TMSTS3	8	8	1 or 2 PCLKB
000A 8374h	RSCAN0	Transmit Buffer Transmit Request Status Register*2	TMTRSTS	16	16	2 or 3 PCLKB
000A 8376h	RSCAN0	Transmit Buffer Transmit Complete Status Register*2	TMTCSTS	16	16	2 or 3 PCLKB
000A 8378h	RSCAN0	Transmit Buffer Transmit Abort Status Register*2	TMTASTS	16	16	2 or 3 PCLKB
000A 837Ah	RSCAN0	Transmit Buffer Interrupt Enable Register*2	TMIEC	16	16	2 or 3 PCLKB
000A 837Ch	RSCAN0	Transmit History Buffer Control Register*2	THLCC0	16	16	2 or 3 PCLKB
000A 8380h	RSCAN0	Transmit History Buffer Status Register*2	THLSTS0	16	16	2 or 3 PCLKB
000A 8384h	RSCAN0	Transmit History Buffer Pointer Control Register*2	THLPCTR0	16	16	2 or 3 PCLKB
000A 8388h	RSCAN	Global Transmit Interrupt Status Register*2	GTINTSTS	16	16	2 or 3 PCLKB
000A 838Ah	RSCAN	Global RAM Window Control Register*2	GRWCR	16	16	2 or 3 PCLKB
000A 838Ch	RSCAN	Global Test Configuration Register*2	GTSTCFG	16	16	2 or 3 PCLKB
000A 838Eh	RSCAN	Global Test Control Register*2	GTSTCTRL	8	8	1 or 2 PCLKB
000A 8394h	RSCAN	Global Test Protection Unlock Register*2	GLOCKK	16	16	2 or 3 PCLKB
000A 83A0h	RSCAN	Receive Rule Entry Register 0AL*2	GAFLIDL0	16	16	2 or 3 PCLKB
000A 83A0h	RSCAN	Receive Buffer Register 0AL*2	RMIDL0	16	16	2 or 3 PCLKB
000A 83A2h	RSCAN	Receive Rule Entry Register 0AH*2	GAFLIDH0	16	16	2 or 3 PCLKB
000A 83A2h	RSCAN	Receive Buffer Register 0AH*2	RMIDH0	16	16	2 or 3 PCLKB
000A 83A4h	RSCAN	Receive Rule Entry Register 0BL*2	GAFLML0	16	16	2 or 3 PCLKB
000A 83A4h	RSCAN	Receive Buffer Register 0BL*2	RMTS0	16	16	2 or 3 PCLKB
000A 83A6h	RSCAN	Receive Rule Entry Register 0BH*2	GAFLMH0	16	16	2 or 3 PCLKB
000A 83A6h	RSCAN	Receive Buffer Register 0BH*2	RMPTR0	16	16	2 or 3 PCLKB
000A 83A8h	RSCAN	Receive Rule Entry Register 0CL*2	GAFLPL0	16	16	2 or 3 PCLKB
000A 83A8h	RSCAN	Receive Buffer Register 0CL*2	RMDF00	16	16	2 or 3 PCLKB
000A 83AAh	RSCAN	Receive Rule Entry Register 0CH*2	GAFLPH0	16	16	2 or 3 PCLKB
000A 83AAh	RSCAN	Receive Buffer Register 0CH*2	RMDF10	16	16	2 or 3 PCLKB
000A 83ACh	RSCAN	Receive Rule Entry Register 1AL*2	GAFLIDL1	16	16	2 or 3 PCLKB
000A 83ACh	RSCAN	Receive Buffer Register 0DL*2	RMDF20	16	16	2 or 3 PCLKB
000A 83AEh	RSCAN	Receive Rule Entry Register 1AH*2	GAFLIDH1	16	16	2 or 3 PCLKB
000A 83AEh	RSCAN	Receive Buffer Register 0DH*2	RMDF30	16	16	2 or 3 PCLKB
000A 83B0h	RSCAN	Receive Rule Entry Register 1BL*2	GAFLML1	16	16	2 or 3 PCLKB
000A 83B0h	RSCAN	Receive Buffer Register 1AL*2	RMIDL1	16	16	2 or 3 PCLKB
000A 83B2h	RSCAN	Receive Rule Entry Register 1BH*2	GAFLMH1	16	16	2 or 3 PCLKB
000A 83B2h	RSCAN	Receive Buffer Register 1AH*2	RMIDH1	16	16	2 or 3 PCLKB
000A 83B4h	RSCAN	Receive Rule Entry Register 1CL*2	GAFLPL1	16	16	2 or 3 PCLKB
000A 83B4h	RSCAN	Receive Buffer Register 1BL*2	RMTS1	16	16	2 or 3 PCLKB
000A 83B6h	RSCAN	Receive Rule Entry Register 1CH*2	GAFLPH1	16	16	2 or 3 PCLKB
000A 83B6h	RSCAN	Receive Buffer Register 1BH*2	RMPTR1	16	16	2 or 3 PCLKB
000A 83B8h	RSCAN	Receive Rule Entry Register 2AL*2	GAFLIDL2	16	16	2 or 3 PCLKB
000A 83B8h	RSCAN	Receive Buffer Register 1CL*2	RMDF01	16	16	2 or 3 PCLKB
000A 83BAh	RSCAN	Receive Rule Entry Register 2AH*2	GAFLIDH2	16	16	2 or 3 PCLKB
000A 83BAh	RSCAN	Receive Buffer Register 1CH*2	RMDF11	16	16	2 or 3 PCLKB
000A 83BCh	RSCAN	Receive Rule Entry Register 2BL*2	GAFLML2	16	16	2 or 3 PCLKB
000A 83BCh	RSCAN	Receive Buffer Register 1DL*2	RMDF21	16	16	2 or 3 PCLKB
000A 83BEh	RSCAN	Receive Rule Entry Register 2BH*2	GAFLMH2	16	16	2 or 3 PCLKB
000A 83BEh	RSCAN	Receive Buffer Register 1DH*2	RMDF31	16	16	2 or 3 PCLKB
000A 83C0h	RSCAN	Receive Rule Entry Register 2CL*2	GAFLPL2	16	16	2 or 3 PCLKB
000A 83C0h	RSCAN	Receive Buffer Register 2AL*2	RMIDL2	16	16	2 or 3 PCLKB
000A 83C2h	RSCAN	Receive Rule Entry Register 2CH*2	GAFLPH2	16	16	2 or 3 PCLKB
000A 83C2h	RSCAN	Receive Buffer Register 2AH*2	RMIDH2	16	16	2 or 3 PCLKB
000A 83C4h	RSCAN	Receive Rule Entry Register 3AL*2	GAFLIDL3	16	16	2 or 3 PCLKB

Table 4.1 List of I/O Registers (Address Order) (34/37)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access Cycles ICLK ≥ PCLK
000C 21A0h	GPT1	General PWM Timer Period Setting Double Buffer Register*2	GTPDBR	16	16, 32	4 or 5 PCLKA
000C 21A4h	GPT1	A/D Converter Start Request Timing Register A*2	GTADTRA	16	16, 32	4 or 5 PCLKA
000C 21A6h	GPT1	A/D Converter Start Request Timing Buffer Register A*2	GTADTBRA	16	16, 32	4 or 5 PCLKA
000C 21A8h	GPT1	A/D Converter Start Request Timing Double Buffer Register A*2	GTADTDBRA	16	16, 32	4 or 5 PCLKA
000C 21ACh	GPT1	A/D Converter Start Request Timing Register B*2	GTADTRB	16	16, 32	4 or 5 PCLKA
000C 21AEh	GPT1	A/D Converter Start Request Timing Buffer Register B*2	GTADTBRB	16	16, 32	4 or 5 PCLKA
000C 21B0h	GPT1	A/D Converter Start Request Timing Double Buffer Register B*2	GTADTDBRB	16	16, 32	4 or 5 PCLKA
000C 21B4h	GPT1	General PWM Timer Output Negate Control Register*2	GTONCR	16	16, 32	4 or 5 PCLKA
000C 21B6h	GPT1	General PWM Timer Dead Time Control Register*2	GTDTCR	16	16, 32	4 or 5 PCLKA
000C 21B8h	GPT1	General PWM Timer Dead Time Value Register U*2	GTDVU	16	16, 32	4 or 5 PCLKA
000C 21BAh	GPT1	General PWM Timer Dead Time Value Register D*2	GTDVD	16	16, 32	4 or 5 PCLKA
000C 21BCh	GPT1	General PWM Timer Dead Time Buffer Register U*2	GTDBU	16	16, 32	4 or 5 PCLKA
000C 21BEh	GPT1	General PWM Timer Dead Time Buffer Register D*2	GTDBD	16	16, 32	4 or 5 PCLKA
000C 21C0h	GPT1	General PWM Timer Output Protection Function Status Register*2	GTSOS	16	16, 32	4 or 5 PCLKA
000C 21C2h	GPT1	General PWM Timer Output Protection Function Temporary Release Register*2	GTSOTR	16	16, 32	4 or 5 PCLKA
000C 2200h	GPT2	General PWM Timer I/O Control Register*2	GTIOR	16	8, 16, 32	4 or 5 PCLKA
000C 2202h	GPT2	General PWM Timer Interrupt Output Setting Register*2	GTINTAD	16	8, 16, 32	4 or 5 PCLKA
000C 2204h	GPT2	General PWM Timer Control Register*2	GTCR	16	8, 16, 32	4 or 5 PCLKA
000C 2206h	GPT2	General PWM Timer Buffer Enable Register*2	GTBER	16	8, 16, 32	4 or 5 PCLKA
000C 2208h	GPT2	General PWM Timer Count Direction Register*2	GTUDC	16	8, 16, 32	4 or 5 PCLKA
000C 220Ah	GPT2	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register*2	GTITC	16	8, 16, 32	4 or 5 PCLKA
000C 220Ch	GPT2	General PWM Timer Status Register*2	GTST	16	8, 16, 32	4 or 5 PCLKA
000C 220Eh	GPT2	General PWM Timer Counter*2	GTCNT	16	16	4 or 5 PCLKA
000C 2210h	GPT2	General PWM Timer Compare Capture Register A*2	GTCCRA	16	16, 32	4 or 5 PCLKA
000C 2212h	GPT2	General PWM Timer Compare Capture Register B*2	GTCCRB	16	16, 32	4 or 5 PCLKA
000C 2214h	GPT2	General PWM Timer Compare Capture Register C*2	GTCCRC	16	16, 32	4 or 5 PCLKA
000C 2216h	GPT2	General PWM Timer Compare Capture Register D*2	GTCCRD	16	16, 32	4 or 5 PCLKA
000C 2218h	GPT2	General PWM Timer Compare Capture Register E*2	GTCCRE	16	16, 32	4 or 5 PCLKA
000C 221Ah	GPT2	General PWM Timer Compare Capture Register F*2	GTCCRF	16	16, 32	4 or 5 PCLKA
000C 221Ch	GPT2	General PWM Timer Period Setting Register*2	GTPR	16	16, 32	4 or 5 PCLKA
000C 221Eh	GPT2	General PWM Timer Period Setting Buffer Register*2	GTPBR	16	16, 32	4 or 5 PCLKA
000C 2220h	GPT2	General PWM Timer Period Setting Double Buffer Register*2	GTPDBR	16	16, 32	4 or 5 PCLKA
000C 2224h	GPT2	A/D Converter Start Request Timing Register A*2	GTADTRA	16	16, 32	4 or 5 PCLKA
000C 2226h	GPT2	A/D Converter Start Request Timing Buffer Register A*2	GTADTBRA	16	16, 32	4 or 5 PCLKA
000C 2228h	GPT2	A/D Converter Start Request Timing Double Buffer Register A*2	GTADTDBRA	16	16, 32	4 or 5 PCLKA
000C 222Ch	GPT2	A/D Converter Start Request Timing Register B*2	GTADTRB	16	16, 32	4 or 5 PCLKA
000C 222Eh	GPT2	A/D Converter Start Request Timing Buffer Register B*2	GTADTBRB	16	16, 32	4 or 5 PCLKA
000C 2230h	GPT2	A/D Converter Start Request Timing Double Buffer Register B*2	GTADTDBRB	16	16, 32	4 or 5 PCLKA
000C 2234h	GPT2	General PWM Timer Output Negate Control Register*2	GTONCR	16	16, 32	4 or 5 PCLKA
000C 2236h	GPT2	General PWM Timer Dead Time Control Register*2	GTDTCR	16	16, 32	4 or 5 PCLKA
000C 2238h	GPT2	General PWM Timer Dead Time Value Register U*2	GTDVU	16	16, 32	4 or 5 PCLKA
000C 223Ah	GPT2	General PWM Timer Dead Time Value Register D*2	GTDVD	16	16, 32	4 or 5 PCLKA
000C 223Ch	GPT2	General PWM Timer Dead Time Buffer Register U*2	GTDBU	16	16, 32	4 or 5 PCLKA
000C 223Eh	GPT2	General PWM Timer Dead Time Buffer Register D*2	GTDBD	16	16, 32	4 or 5 PCLKA
000C 2240h	GPT2	General PWM Timer Output Protection Function Status Register*2	GTSOS	16	16, 32	4 or 5 PCLKA
000C 2242h	GPT2	General PWM Timer Output Protection Function Temporary Release Register*2	GTSOTR	16	16, 32	4 or 5 PCLKA

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = AVSS1 = AVSS2 = 0 V

Item		Symbol	Value	Unit
Power supply voltage		VCC	–0.3 to +6.5	V
Input voltage	Port 4, port 5, port 6	V_{in}	–0.3 to VREF + 0.3	V
	Except for port 4, port 5, port 6 and ports for 5 V tolerant*1		–0.3 to VCC + 0.3	V
	Ports for 5 V tolerant*1		–0.3 to +6.5	V
Analog power supply voltage		AVCC0, AVCC1, AVCC2, VREF	–0.3 to +6.5	V
Analog input voltage	When AN000 to AN003, AN100 to AN103, AN200 to AN211 used	V_{AN}	–0.3 to VREF + 0.3	V
	When AN016, AN116, CVREFC0, CVREFC1 used		–0.3 to VCC + 0.3	
Operating temperature		T_{opr}	–40 to +85	°C
Storage temperature		T_{stg}	–55 to +125	°C

Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.
To preclude any malfunctions due to noise interference, insert capacitors of high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, between the AVCC1 and AVSS1 pins, between the AVCC2 and AVSS2 pins, between the VREF and AVSS2 pins. Place capacitors of about 0.1 µF as close as possible to every power supply pin and use the shortest and heaviest possible traces.
Connect the VCL pin to a VSS pin via a 4.7 µF capacitor. The capacitor must be placed close to the pin.
Do not input signals or an I/O pull-up power supply to ports other than 5-V tolerant ports while the device is not powered.
The current injection that results from input of such a signal or I/O pull-up may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.
Even if –0.3 to +6.5 V is input to 5-V tolerant ports, it will not cause problems such as damage to the MCU.
Note 1. Ports B1 and B2 are 5 V tolerant.

Table 5.2 Recommended Operating Voltage Conditions

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltages	VCC*1, *2		2.7	—	5.5	V
	VSS		—	0	—	
Analog power supply voltages	AVCC0, AVCC1, AVCC2, VREF*1, *2		VCC	—	5.5	V
	AVSS0, AVSS1, AVSS2		—	0	—	

Note 1. AVCC0/AVCC1/AVCC2/VREF and VCC can be set individually within the operating range.
Note 2. When powering on the VCC and AVCC0/AVCC1/AVCC2/VREF pins, power them on at the same time or the VCC pin first and then the AVCC0/AVCC1/AVCC2/VREF pin.

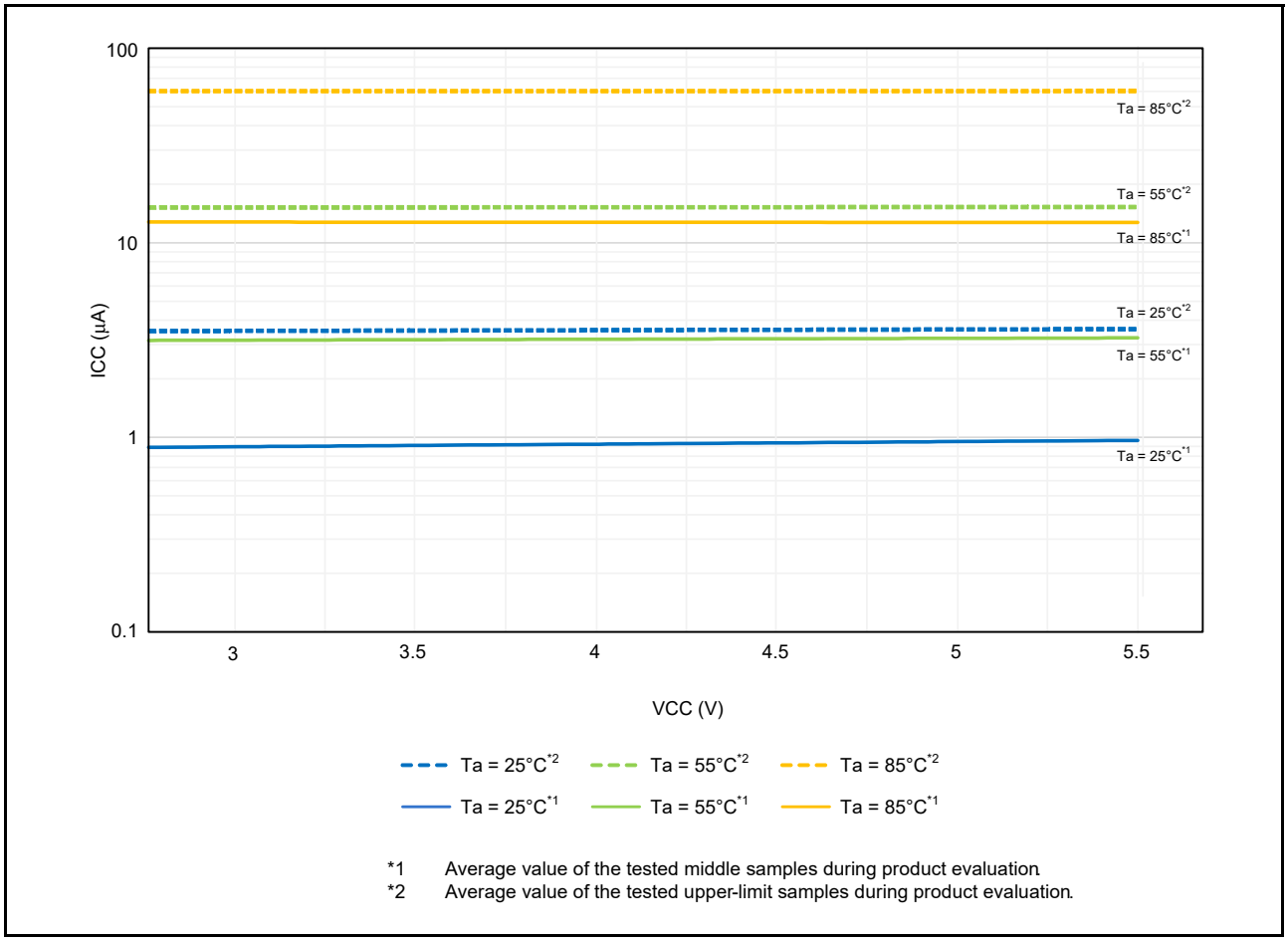


Figure 5.2 Voltage Dependency in Software Standby Mode (Chip Version B) (Reference Data)

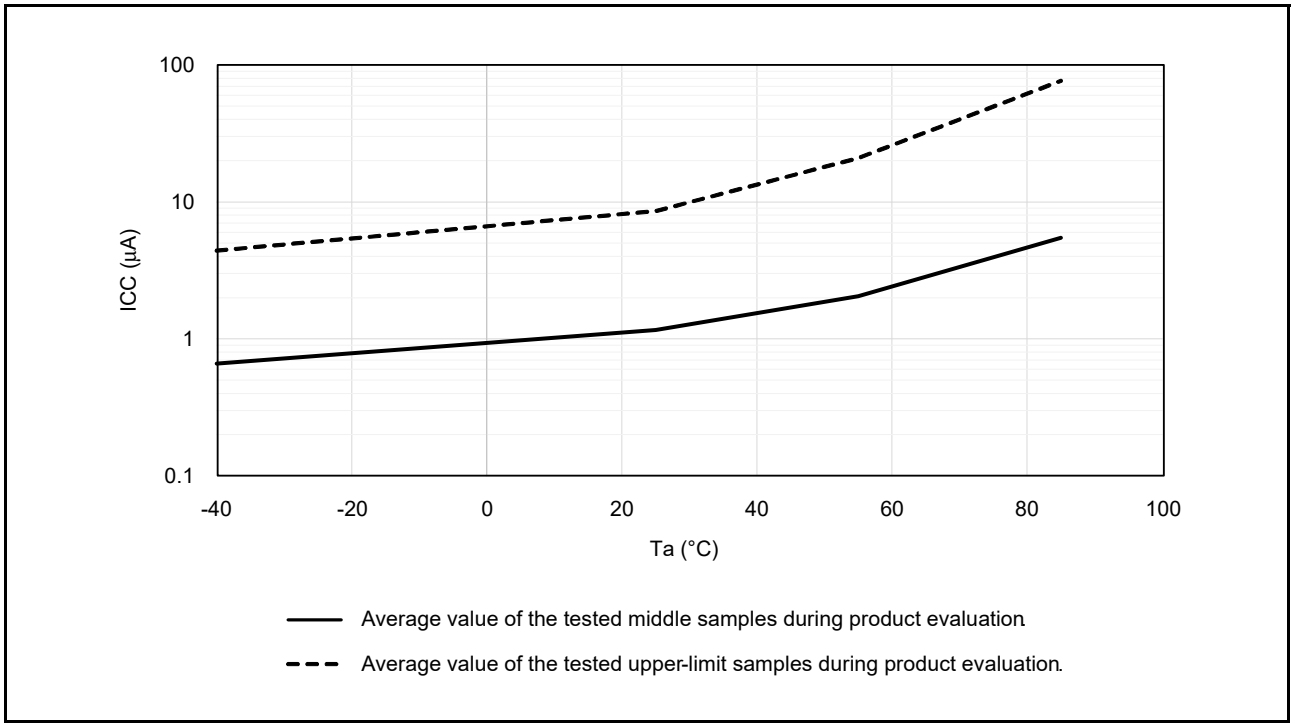


Figure 5.3 Temperature Dependency in Software Standby Mode (Chip Version A) (Reference Data)

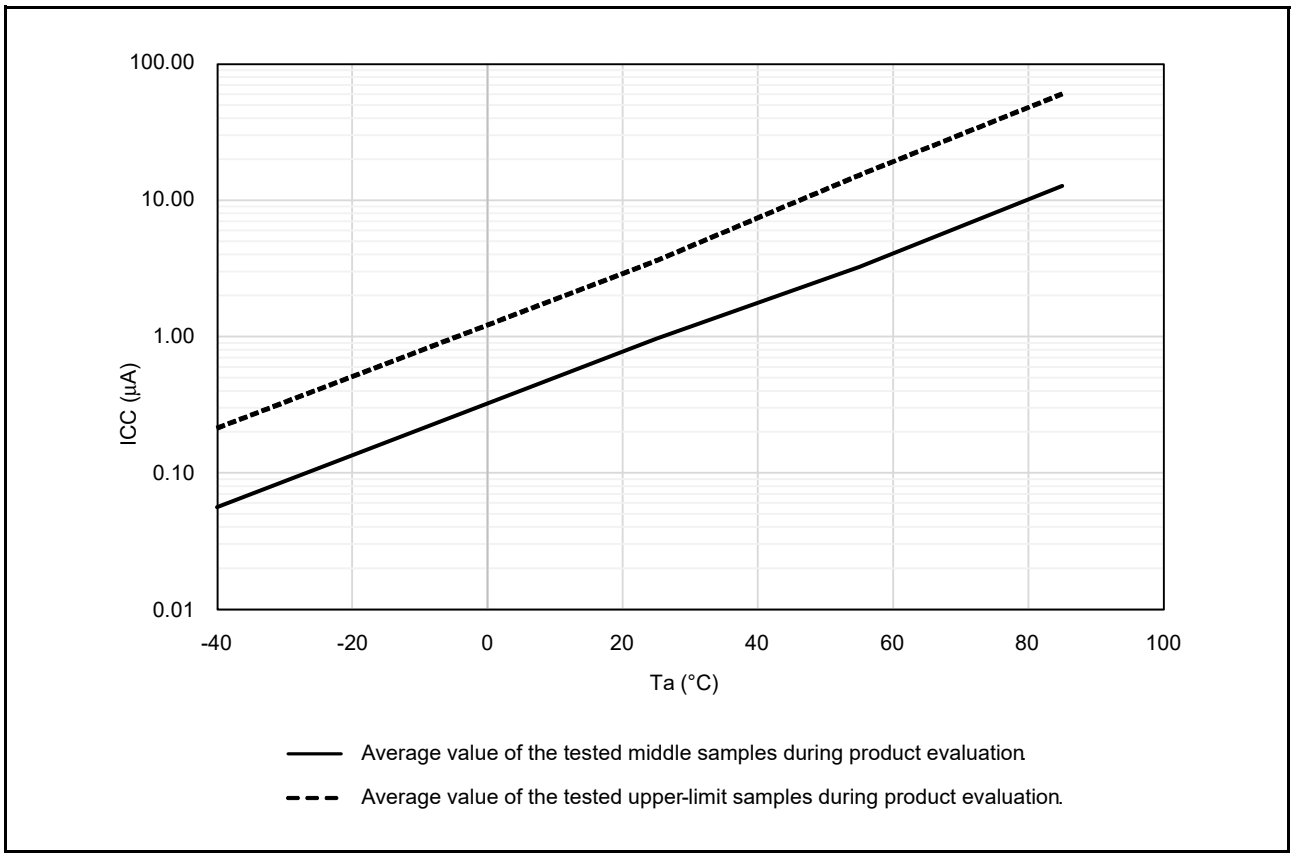


Figure 5.4 Temperature Dependency in Software Standby Mode (Chip Version B) (Reference Data)

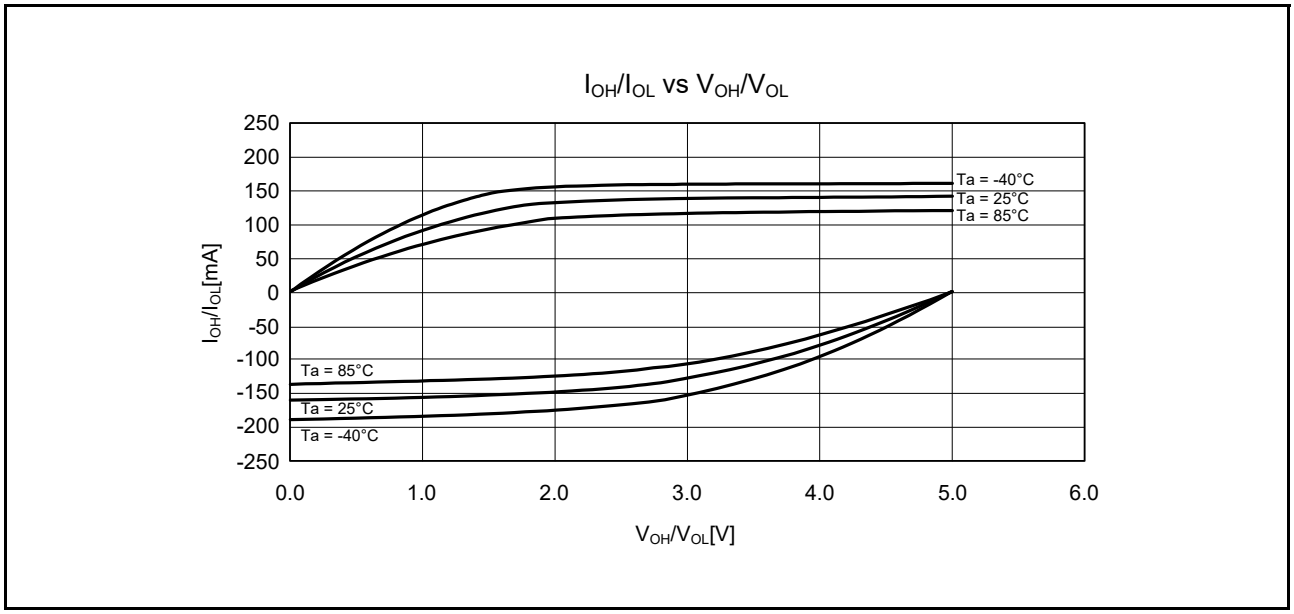


Figure 5.16 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics of Large Current Ports at VCC = 5.0 V (Reference Data)

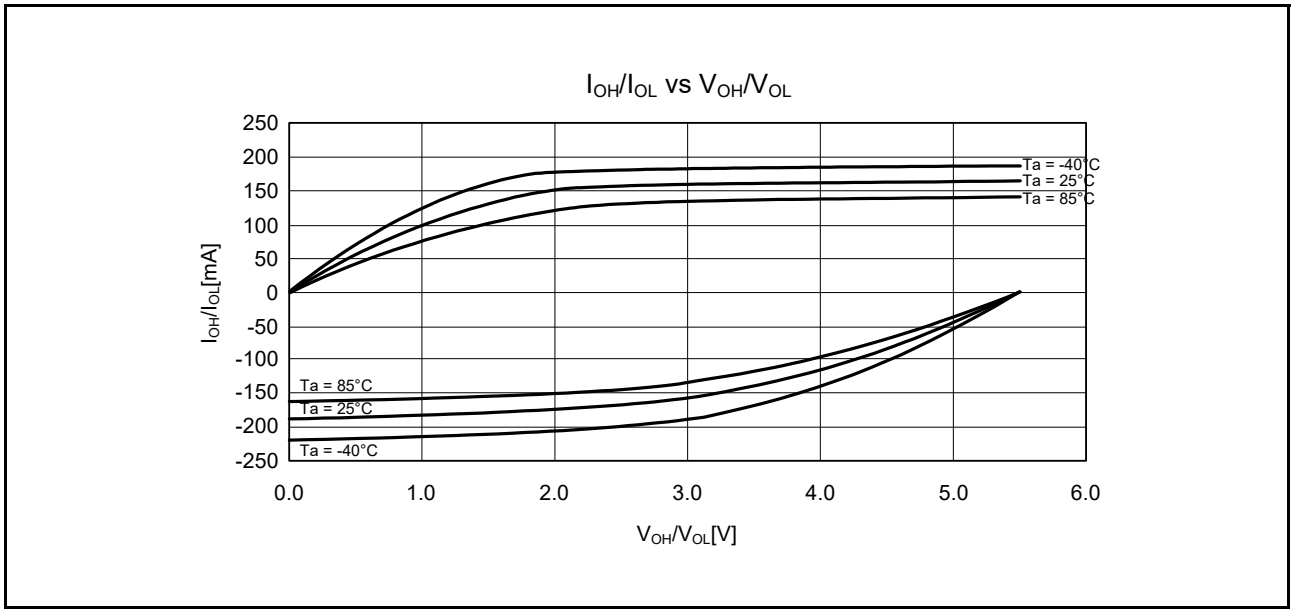


Figure 5.17 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics of Large Current Ports at VCC = 5.5 V (Reference Data)

5.3 AC Characteristics

5.3.1 Clock Timing

Table 5.14 Operating Frequency Value (High-Speed Operating Mode)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item		Symbol	min.	typ.	max.	Unit
Operating frequency	System clock (ICLK)	f_{max}	—	—	80	MHz
	FlashIF clock (FCLK)*1, *2		—	—	32	
	Peripheral module clock (PCLKA)		—	—	80	
	Peripheral module clock (PCLKB)		—	—	40	
	Peripheral module clock (PCLKD)		—	—	40	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK should be ±3.5%.

Table 5.15 Operating Frequency Value (Middle-Speed Operating Mode)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item		Symbol	min.	typ.	max.	Unit
Operating frequency	System clock (ICLK)	f_{max}	—	—	12	MHz
	FlashIF clock (FCLK)*1, *2		—	—	12	
	Peripheral module clock (PCLKA)		—	—	12	
	Peripheral module clock (PCLKB)		—	—	12	
	Peripheral module clock (PCLKD)		—	—	12	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK should be ±3.5%.

Table 5.16 Clock Timing

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time	t_{Xcyc}	50	—	—	ns	Figure 5.22
EXTAL external clock input high pulse width	t_{XH}	20	—	—	ns	
EXTAL external clock input low pulse width	t_{XL}	20	—	—	ns	
EXTAL external clock rise time	t_{Xr}	—	—	5	ns	
EXTAL external clock fall time	t_{Xf}	—	—	5	ns	
EXTAL external clock input wait time*1	t_{XWT}	0.5	—	—	μs	
Main clock oscillator oscillation frequency	f_{MAIN}	1	—	20	MHz	
Main clock oscillation stabilization time (crystal)*2	$t_{MAINOSC}$	—	3	—	ms	Figure 5.23
Main clock oscillation stabilization time (ceramic resonator)*2	$t_{MAINOSC}$	—	50	—	μs	
LOCO clock oscillation frequency	f_{LOCO}	3.44	4.0	4.56	MHz	
LOCO clock oscillation stabilization time	t_{LOCO}	—	—	0.5	μs	Figure 5.24
HOCO clock oscillation frequency	f_{HOCO} (32MHz)	31.52	32	32.48	MHz	T_a = –40 to –20°C
		31.68	32	32.32	MHz	T_a = –20 to +75°C
		31.52	32	32.48	MHz	T_a = +75 to +85°C
	f_{HOCO} (64MHz)	63.04	64	64.96	MHz	T_a = –40 to –20°C
		63.36	64	64.64	MHz	T_a = –20 to +75°C
		63.04	64	64.96	MHz	T_a = +75 to +85°C
HOCO clock oscillation stabilization time	t_{HOCO} (32MHz)	—	—	37.1	μs	Figure 5.26
	t_{HOCO} (64MHz)	—	—	80.6	μs	Figure 5.26
IWDT-dedicated clock oscillation frequency	f_{ILOCO}	12.75	15	17.25	kHz	
IWDT-dedicated clock oscillation stabilization time	t_{ILOCO}	—	—	50	μs	Figure 5.27
PLL circuit oscillation frequency	f_{PLL}	40	—	80	MHz	
PLL clock oscillation stabilization time	t_{PLL}	—	—	50	μs	Figure 5.28
PLL free-running oscillation frequency	f_{PLLFR}	—	8	—	MHz	

Note 1. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating) when the external clock is stable.

Note 2. Reference values when an 8-MHz resonator is used.
When specifying the main clock oscillator stabilization time, set the MOSCWTCR register with a stabilization time value that is equal to or greater than the resonator-manufacturer-recommended value.
After changing the setting of the MOSCCR.MOSTP bit so that the main clock oscillator operates, read the OSCOVFSR.MOOVF flag to confirm that is has become 1, and then start using the main clock.

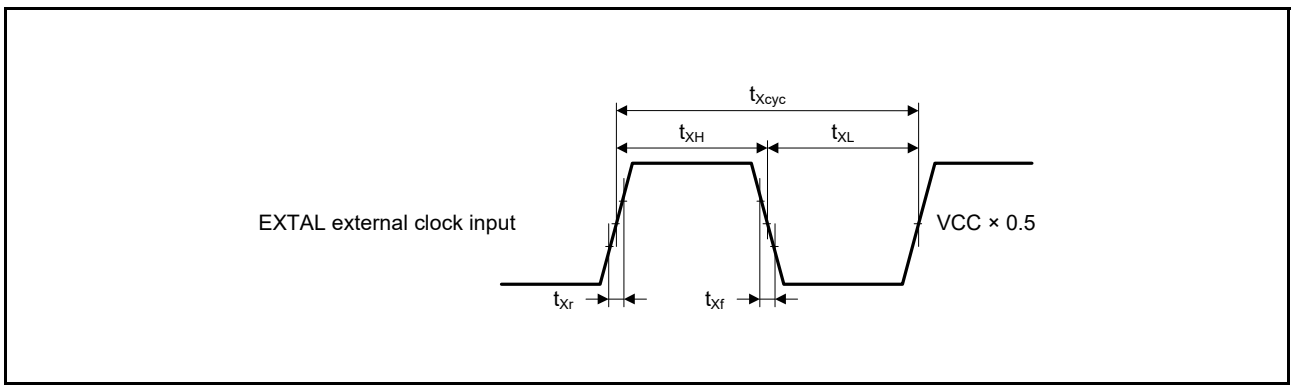


Figure 5.22 EXTAL External Clock Input Timing

Table 5.19 Timing of Recovery from Low Power Consumption Modes (2)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	Middle-speed mode	Crystal connected to main clock oscillator	Main clock oscillator operating*2	t_{SBYMC}	—	2	3	ms	Figure 5.32
			Main clock oscillator and PLL circuit operating*3	t_{SBYPC}	—	2	3	ms	
		External clock input to main clock oscillator	Main clock oscillator operating*4	t_{SBYEX}	—	3	4	µs	
			Main clock oscillator and PLL circuit operating*5	t_{SBYPE}	—	65	85	µs	
		HOCO clock oscillator operating	HOCO clock oscillator operating 1 *6	t_{SBYHO}	—	40	50	µs	
			HOCO clock oscillator operating 2 *7		—	75	85	µs	
			HOCO clock oscillator and PLL circuit operating*8	t_{SBYPH}	—	110	125	µs	
		LOCO clock oscillator operating*9		t_{SBYLO}	—	5	7	µs	

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. The recovery time when multiple oscillators are operating varies depending on the operating state of the oscillators that are not selected as the system clock source. The above table applies when only the corresponding clock is operating.

Note 2. When the frequency of the crystal is 12 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are not divided.

Note 3. When the frequency of PLL is 48 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are set to 12 MHz.

Note 4. When the frequency of the external clock is 12 MHz.
When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are not divided.

Note 5. When the frequency of PLL is 48 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.
When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are set to 12 MHz.

Note 6. When the frequency of the high-speed on-chip oscillator is 32 MHz. When the high-speed on-chip oscillator wait control register (HOCOWTCR) is set to 05h. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are set to 8 MHz.

Note 7. When the frequency of the high-speed on-chip oscillator is 64 MHz. Set the high-speed on-chip oscillator wait control register (HOCOWTCR) is set to 06h. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are set to 8 MHz.

Note 8. When the frequency of the high-speed on-chip oscillator is 32 MHz, and the frequency of PLL is 80 MHz. When the high-speed on-chip oscillator wait control register (HOCOWTCR) is set to 05h. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are set to 10 MHz.

Note 9. When the frequencies of ICLK, FCLK, PCLKA, PCLKB, and PCLKD are not divided.

5.3.5 Timing of On-Chip Peripheral Modules

Table 5.23 Timing of On-Chip Peripheral Modules (1)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C

Item				Symbol	Min.	Max.	Unit *1	Test Conditions
I/O ports	Input data pulse width			t_{PRW}	1.5	—	t_{Pcyc}	Figure 5.36
MTU3	Input capture input pulse width		Single-edge setting	t_{TICW}	3	—	t_{PAcyc}	Figure 5.37
			Both-edge setting		5	—		
	Timer clock pulse width		Single-edge setting	t_{TCKWH}, t_{TCKWL}	3	—	t_{PAcyc}	Figure 5.38
			Both-edge setting		5	—		
			Phase counting mode		5	—		
POE3	POE# input pulse width			t_{POEW}	1.5	—	t_{Pcyc}	Figure 5.39
GPT	Input capture input pulse width		Single-edge setting	t_{GTICW}	1.5	—	t_{PAcyc}	Figure 5.40
			Both-edge setting		2.5	—		
	External trigger input pulse width		Single-edge setting	t_{GTETW}	1.5	—	t_{PAcyc}	Figure 5.41
			Both-edge setting		2.5	—		
	Timer clock pulse width			t_{GTCKWH}	1.5	—	t_{PAcyc}	Figure 5.42
				t_{GTCKWL}				
TMR	Timer clock pulse width		Single-edge setting	t_{TMCWH}, t_{TMCWL}	1.5	—	t_{Pcyc}	Figure 5.43
			Both-edge setting		2.5	—		
SCI	Input clock cycle		Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	Figure 5.44
			Clock synchronous		6	—		
	Input clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time			t_{SCKr}	—	20	ns	
	Input clock fall time			t_{SCKf}	—	20	ns	
	Output clock cycle		Asynchronous	t_{Scyc}	16	—	t_{Pcyc}	Figure 5.45
			Clock synchronous		4	—		
	Output clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time			t_{SCKr}	—	20	ns	
	Output clock fall time			t_{SCKf}	—	20	ns	
	Transmit data delay time (master)	Clock synchronous		t_{TXD}	—	40	ns	
	Transmit data delay time (slave)	Clock synchronous	VCC = 4.0 V or above		—	40	ns	
			VCC = 2.7 V or above		—	65	ns	
	Receive data setup time (master)	Clock synchronous	VCC = 4.0 V or above	t_{RXS}	40	—	ns	
			VCC = 2.7 V or above		65	—	ns	
	Receive data setup time (slave)	Clock synchronous			40	—	ns	
	Receive data hold time	Clock synchronous		t_{RXH}	40	—	ns	
A/D converter	Trigger input pulse width			t_{TRGW}	1.5	—	t_{Pcyc}	Figure 5.46
CAC	CACREF input pulse width		$t_{Pcyc} \le t_{cac}$ *2	t_{CACREF}	4.5 t_{cac} + 3 t_{Pcyc}	—	ns	
			$t_{Pcyc} > t_{cac}$ *2		5 t_{cac} + 6.5 t_{Pcyc}			

Note 1. t_{Pcyc}: PCLK cycle, t_{PAcyc}: PCLKA cycle
Note 2. t_{cac}: CAC count clock source cycle

Table 5.24 Timing of On-Chip Peripheral Modules (2)

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 =AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = –40 to +85°C, C = 30pF

Item				Symbol	Min.	Max.	Unit*1	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc}	Figure 5.47
		Slave			6	—		
	RSPCK clock high pulse width	Master	VCC = 4.0 V or above	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 5$	—	ns	
			VCC = 2.7 V or above		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 8$	—		
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width	Master	VCC = 4.0 V or above	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 5$	—	ns	
			VCC = 2.7 V or above		$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 8$	—		
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/fall time	Output	VCC = 4.0 V or above	t_{SPCKr}, t_{SPCKf}	—	6	ns	
			VCC = 2.7 V or above		—	10		
		Input			—	0.1	μs/V	
	Data input setup time	Master	VCC = 4.0 V or above	t_{SU}	10	—	ns	Figure 5.48 to Figure 5.51
			VCC = 2.7 V or above		26	—		
		Slave			20	—		
	Data input hold time	Master	RSPCK set to a division ratio other than PCLKB divided by 2	t_H	t_{Pcyc}	—	ns	
			RSPCK set to PCLKB divided by 2	t_{HF}	0	—		
		Slave		t_H	0	—		
	SSL setup time	Master		t_{LEAD}	–30 + N*2 × t_{SPcyc}	—	ns	
		Slave			6	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	–30 + N*3 × t_{SPcyc}	—	ns	
		Slave			6	—	t_{Pcyc}	
	Data output delay time	Master	VCC = 4.0 V or above	t_{OD}	—	10	ns	
			VCC = 2.7 V or above		—	14		
		Slave			—	65		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$6 \times t_{Pcyc}$	—		
	MOSI and MISO rise/fall time	Output		t_{Dr}, t_{Df}	—	10	ns	
		Input			—	1	μs	
	SSL rise/fall time	Output		t_{SSLr}, t_{SSLf}	—	10	ns	
		Input			—	1	μs	
	Slave access time			t_{SA}	—	6	t_{Pcyc}	Figure 5.50, Figure 5.51
	Slave output release time			t_{REL}	—	5	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle
Note 2. N: An integer from 1 to 8 that can be set by the RSPI clock delay register (SPCKD)
Note 3. N: An integer from 1 to 8 that can be set by the RSPI slave select negation delay register (SSLND)

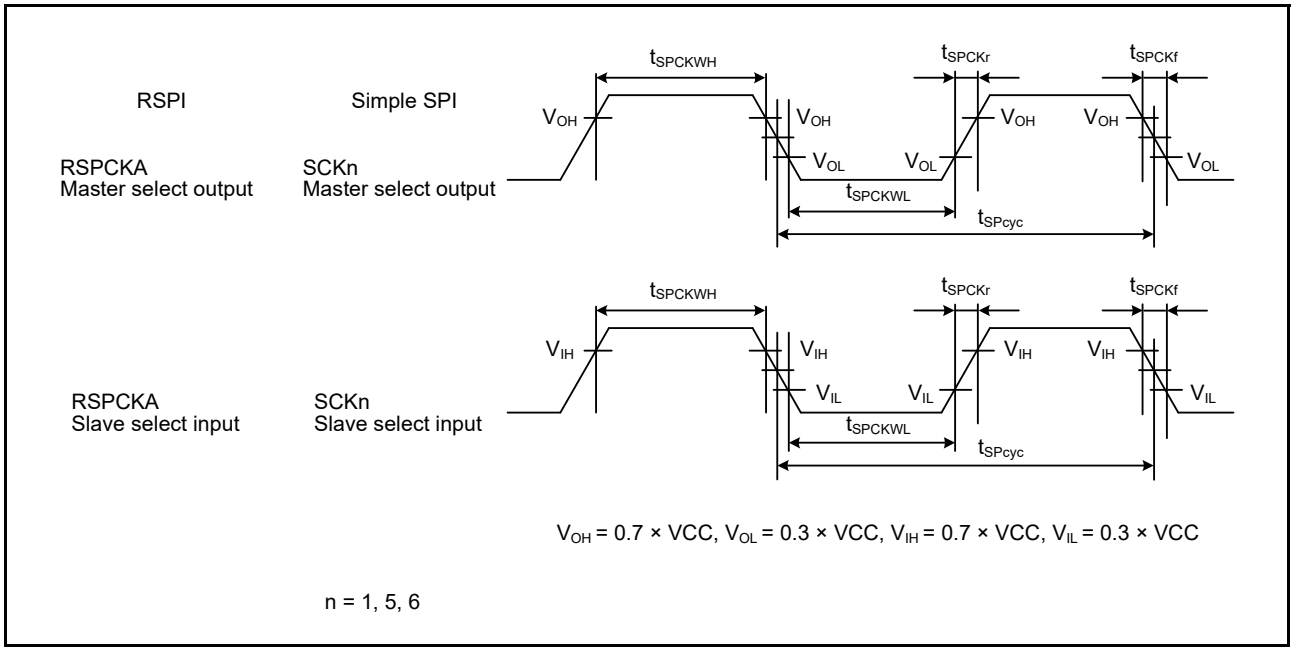


Figure 5.47 RSPI Clock Timing and Simple SPI Clock Timing

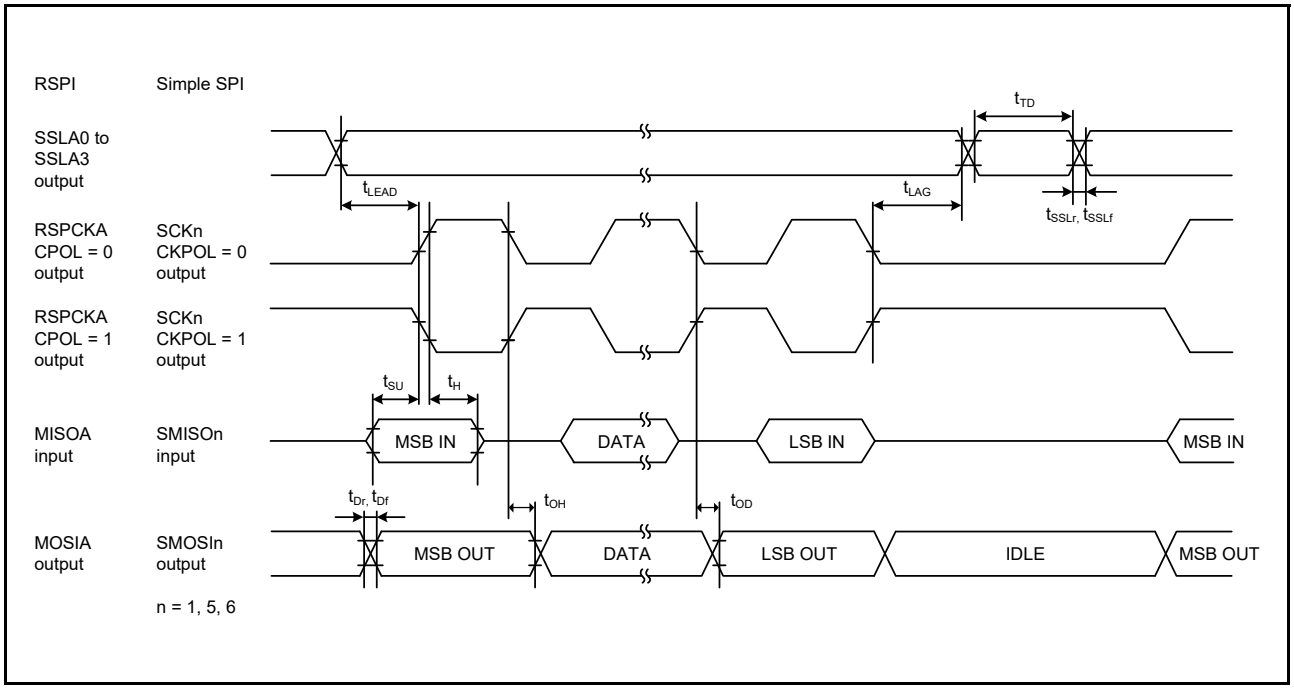


Figure 5.48 RSPI Timing (Master, CPHA = 0) and Simple SPI Clock Timing (Master, CKPH = 1)

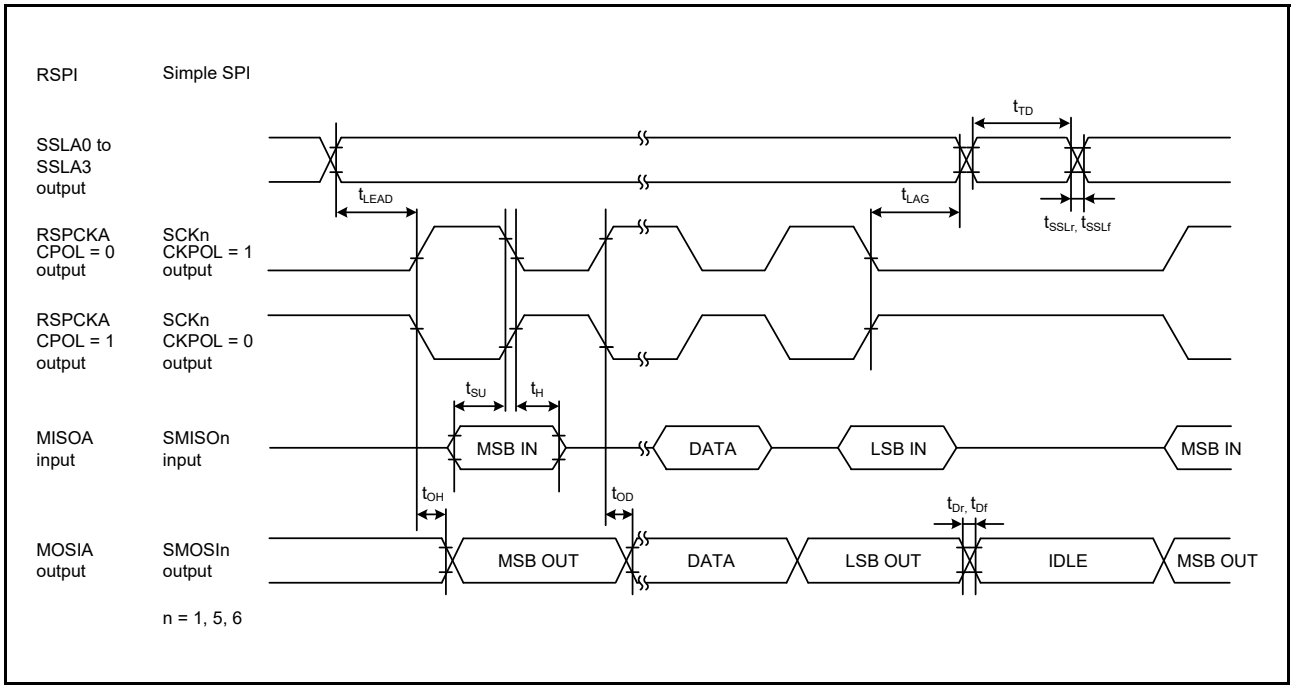


Figure 5.49 RSPI Timing (Master, CPHA = 1) and Simple SPI Clock Timing (Master, CKPH = 0)

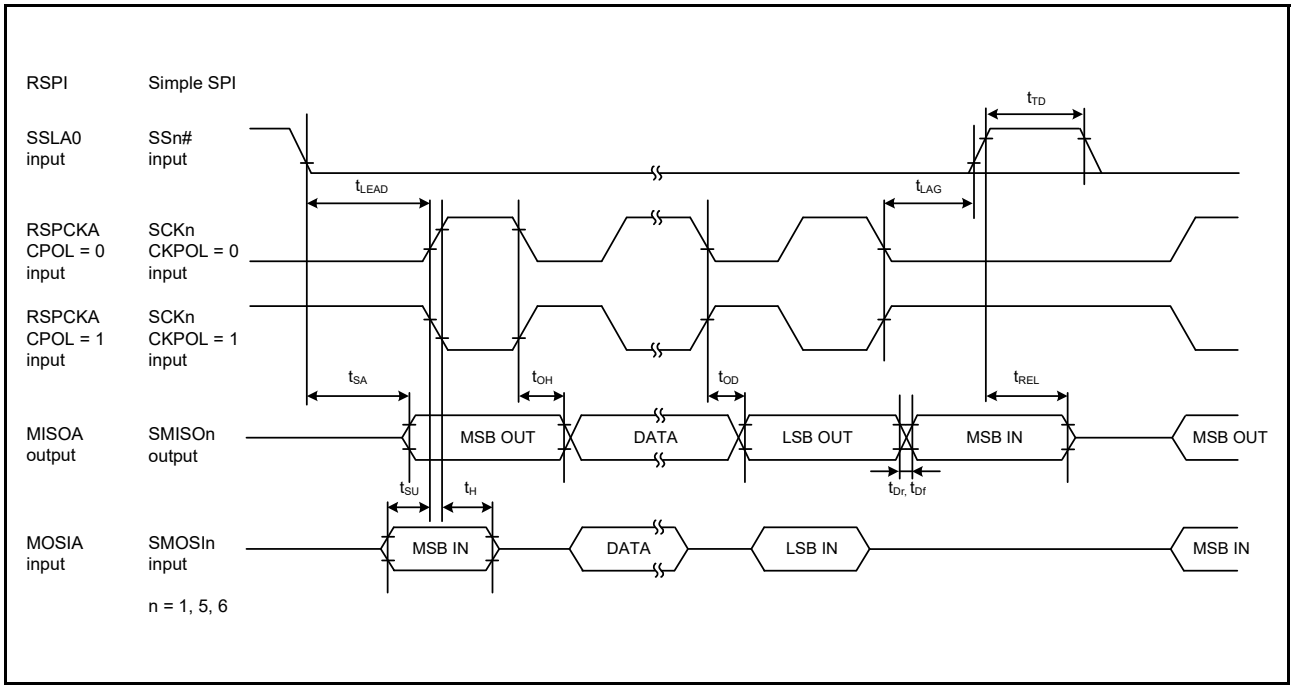


Figure 5.50 RSPI Timing (Slave, CPHA = 0) and Simple SPI Clock Timing (Slave, CKPH = 1)

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

Offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

Table 5.41 ROM (Flash Memory for Code Storage) Characteristics (3): Middle-Speed Operating Mode

Conditions: VCC = 2.7 V to 5.5 V, AVCC0 = AVCC1 = AVCC2 = VREF = VCC to 5.5 V, VSS = AVSS0 = AVSS1 = AVSS2 = 0 V

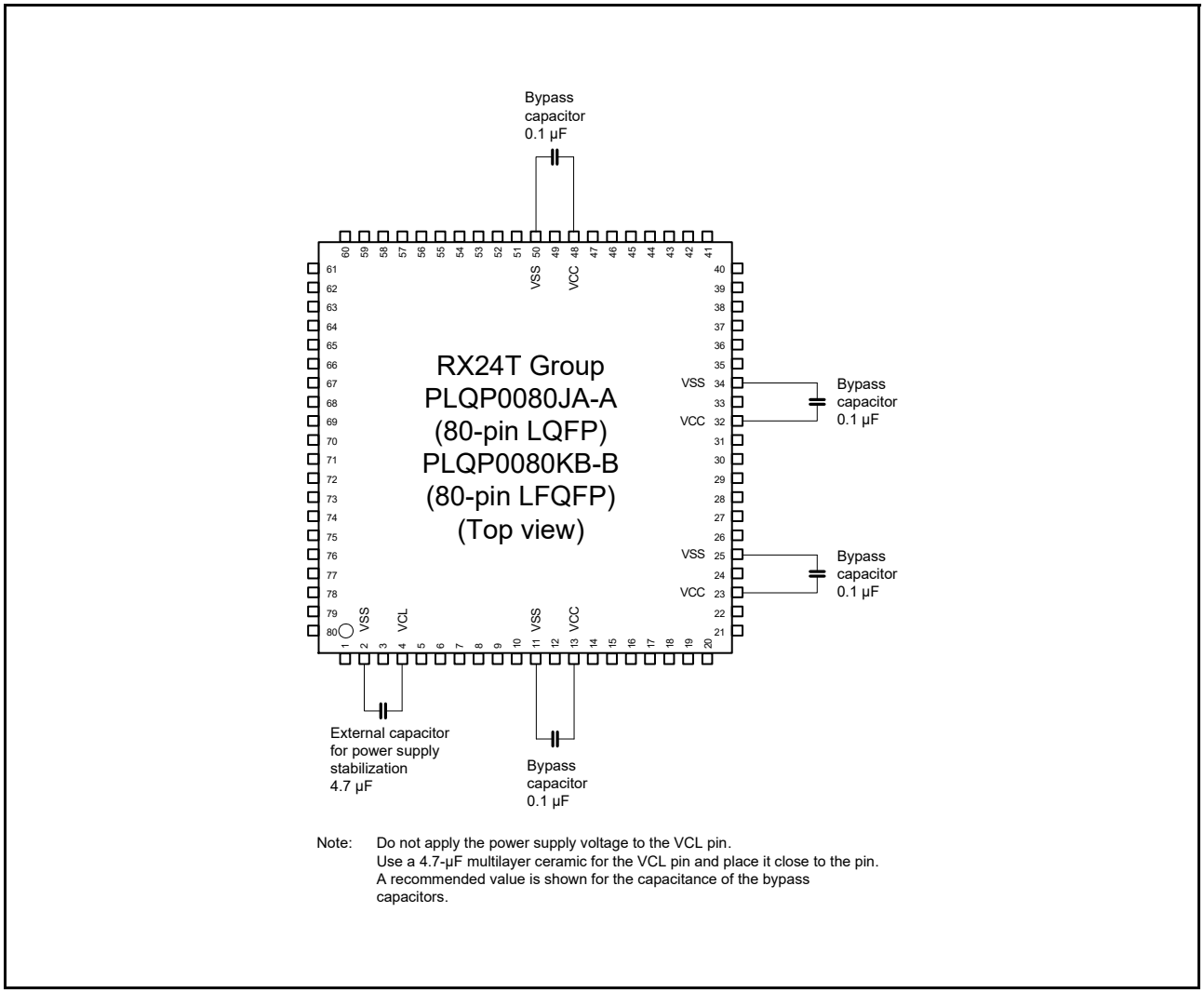
Temperature range for the programming/erasure operation: T_a = –40 to +85°C

Item		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	8-byte	t_{P8}	—	152.0	1367.0	—	97.9	936.0	µs
Erasure time	2-Kbyte	t_{E2K}	—	8.8	279.7	—	5.9	220.8	ms
	256-Kbyte (when block erase command used)	t_{E256K}	—	469.2	9816.9	—	100.5	2260.1	ms
	256-Kbyte (when all-block erase command used)	t_{EA256K}	—	464.0	9610.7	—	95.3	2053.7	ms
	512-Kbyte (when block erase command used)	t_{E512K}	—	928.0	19221.2	—	190.6	4107.3	ms
	512-Kbyte (when all-block erase command used)	t_{EA512K}	—	922.7	19015.0	—	185.4	3901.0	ms
Blank check time	8-byte	t_{BC8}	—	—	85.0	—	—	50.9	µs
	2-Kbyte	t_{BC2K}	—	—	1870.0	—	—	401.5	µs
Erase operation forcible stop time		t_{SED}	—	—	28.0	—	—	21.3	µs
Start-up area switching setting time		t_{SAS}	—	13.0	573.3	—	7.7	450.1	ms
Access window time		t_{AWS}	—	13.0	573.3	—	7.7	450.1	ms
ROM mode transition wait time 1		t_{DIS}	2.0	—	—	2.0	—	—	µs
ROM mode transition wait time 2		t_{MS}	3.0	—	—	3.0	—	—	µs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK should be ±3.5%.



Note: Do not apply the power supply voltage to the VCL pin.
Use a 4.7-µF multilayer ceramic for the VCL pin and place it close to the pin.
A recommended value is shown for the capacitance of the bypass capacitors.

Figure 5.62 Connecting Capacitors (80 Pins)