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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	18
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP Module
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w79e8213akg

2. FEATURES

- Fully static design 8-bit 4T-8051 CMOS microcontroller:
  - VDD = 4.5V to 5.5V @20MHz
  - VDD = 2.7V to 5.5V @12MHz
  - VDD = 2.4V to 5.5V @4MHz
- Instruction-set compatible with MSC-51.
- Flexible CPU clock source configurable by config bit and software:
  - High speed external oscillator: upto 20MHz Crystal and resonator (enabled by config bit).
  - Internal RC oscillator: 20/10MHz selectable by config bit, only W79E8213R supports ±2% accuracy internal RC oscillator at fixed voltage and temperature condition.
- 4K bytes of AP Flash EPROM, with ICP and external writer programmable mode.
- 128 bytes of on-chip RAM.
- W79E8213 series supports 128 bytes NVM Data Flash EPROM for customer data storage used and 10K writer cycles.
  - 8 pages. Page size is 16 bytes.
- Two 16-bit timer/counters.
- Ten interrupts source with four levels of priority.
- Three-edge detect interrupt inputs.
- Programmable Watchdog Timer.
- Four-channel 10-bit PWM (Pulse Width Modulator).
- Internal square wave generator for buzzer.
- Up to 18 I/O pins.
- The 4 outputs mode and TTL/Schmitt trigger selectable Port.
- LED drive capability on all port pins. Sink 20mA; Drive: -15~-20mA @push-pull mode.
- Eight high sink capability (40mA) port pins.
- Eight-channel multiplexed with 10-bits A/D convert.
- Low Voltage Detect interrupt and reset.
- Development Tools:
  - ICP(In Circuit Programming) writer
- Packages:

  - Lead Free (RoHS) DIP 20: W79E8213AKG
  - Lead Free (RoHS) SOP 20: W79E8213ASG
  - Lead Free (RoHS) DIP 20: W79E8213RAKG
  - Lead Free (RoHS) SOP 20: W79E8213RASG

7. MEMORY ORGANIZATION

The W79E8213 series separate the memory into two separate sections, the Program Memory and the Data Memory. The Program Memory is used to store the instruction op-codes, while the Data Memory is used to store data or for memory mapped devices.

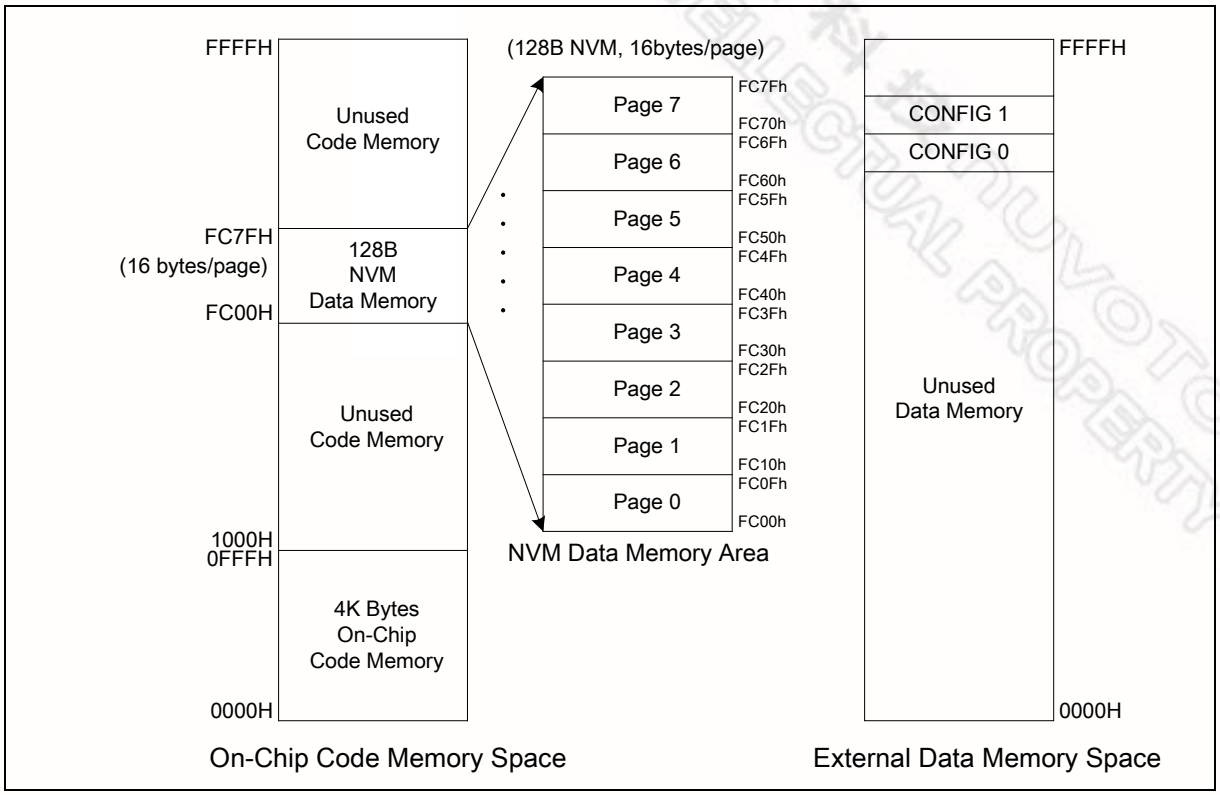


Figure 7-1: W79E8213 series memory map

7.1 Program Memory (on-chip Flash)

The Program Memory on the W79E8213 series can be up to 4K bytes long. All instructions are fetched for execution from this memory area. The MOVC instruction can also access this memory region.

7.2 Data Flash Memory

The NVM Data Memory of Flash EPROM on the W79E8213 series is 128 bytes long, with page size of 16 bytes, respectively. The W79E8213 series' NVM size is controllable through CONFIG1 register. The W79E8213 series read the content of data memory by using "MOVC A, @A+DPTR". To write data is by NVMADDRL, NVMDATA and NVMCON SFR's registers.

7.3 Data Memory (accessed by MOVX)

Not available in this product series.

7.4 Scratch-pad RAM and Register Map

As mentioned before the W79E8213 series have separate Program and Data Memory areas. The on-chip 128 bytes scratch pad RAM is in addition to the external memory. There are also several Special Function Registers (SFRs) which can be accessed by software. The SFRs can be accessed only by direct addressing, while the on-chip RAM can be accessed by either direct or indirect addressing.

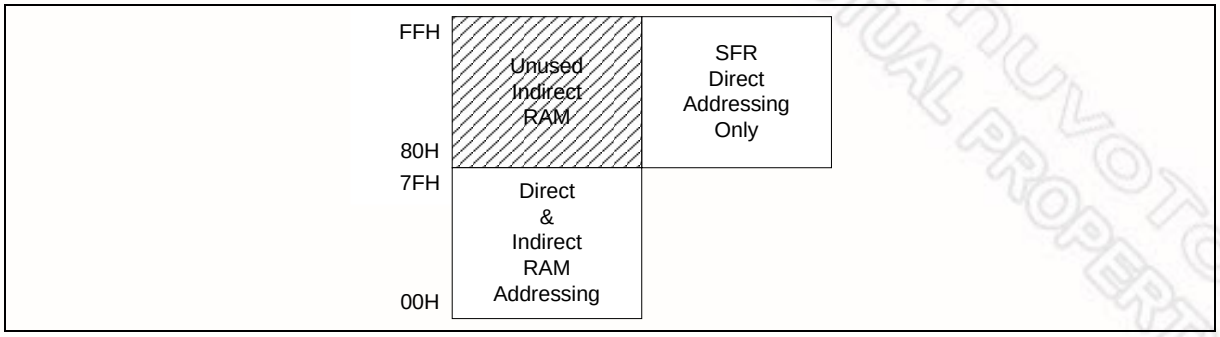


Figure 7-2: W79E8213 RAM and SFR memory map

Since the scratch-pad RAM is only 128 bytes it can be used only when data contents are small. There are several other special purpose areas within the scratch-pad RAM. These are described as following.

8. SPECIAL FUNCTION REGISTERS

The W79E8213 series uses Special Function Registers (SFRs) to control and monitor peripherals and their Modes. The SFRs reside in the register locations 80-FFh and are accessed by direct addressing only. Some of the SFRs are bit addressable. This is very useful in cases where users wish to modify a particular bit without changing the others. The SFRs that are bit addressable are those whose addresses end in 0 or 8. The W79E8213 series contain all the SFRs present in the standard 8052. However some additional SFRs are added. In some cases the unused bits in the original 8052, have been given new functions. The list of the SFRs is as following.

F8	IP1	BUZCON						
F0	B						PADIDS	IP1H
E8	EIE							
E0	ACC	ADCCON	ADCH	ADCCON1				
D8	WDCON	PWMPL	PWM0L	PWM1L	PWMCON1	PWM2L	PWM3L	PWMCON2
D0	PSW	PWMPH	PWM0H	PWM1H		PWM2H	PWM3H	PWMCON3
C8							NVMCON	NVMDATA
C0							NVMADDRL	TA
B8	IP0							
B0		P0M1	P0M2	P1M1	P1M2	P2M1	P2M2	IP0H
A8	IE							
A0	P2		AUXR1	EDIC				
98								
90	P1							
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	
80	P0	SP	DPL	DPH				PCON

Table 8-1: Special Function Register Location Table

Note: 1. The SFRs in the column with dark borders are bit-addressable

2. The table is condensed with eight locations per row. Empty locations indicate that these are no registers at these addresses. When a bit or register is not implemented, it will read high.

SYMBOL	DEFINITION	ADDRESS	MSB LSB BIT_ADDRESS, SYMBOL								RESET
BUZCON	Square wave control register	F9H	-	-	BUZDIV.5	BUZDIV.4	BUZDIV.3	BUZDIV.2	BUZDIV.1	BUZDIV.0	xx00 0000B
IP1	Interrupt priority 1	F8H	(FF) PED	(FE) PPWM	(FD) PBK	(FC) PWDI	(FB) -	(FA) -	(F9) -	(F8) -	0000xxxxB
IP1H	Interrupt high priority 1	F7H	PEDH	PPWMH	PBKH	PWDIH	-	-	-	-	0000xxxxB
PADIDS	Port ADC digital input disable	F6H									00000000B
B	B register	F0H	(F7)	(F6)	(F5)	(F4)	(F3)	(F2)	(F1)	(F0)	00000000B
EIE	Interrupt enable 1	E8H	(EF) EED	(EE) EPWMUF	(ED) EPWM	(EC) EWDI	(EB) -	(EA) -	(E9) -	(E8) -	0000xxxxB
ADCCON1	ADC control register 1	E3H	ADCLK.1	ADCLK.0	-	-	-	AADR2	-	-	10xxx0xxB
ADCH	ADC converter result high register	E2H	ADC.9	ADC.8	ADC.7	ADC.6	ADC.5	ADC.4	ADC.3	ADC.2	00000000B
ADCCON	ADC control register	E1H	ADC.1	ADC.0	ADCEX	ADCI	ADCS	RCCLK	AADR1	AADR0	00000000B
ACC	Accumulator	E0H	(E7)	(E6)	(E5)	(E4)	(E3)	(E2)	(E1)	(E0)	00000000B
PWMCON2	PWM control register 2	DFH	BKCH	BKPS	BPEN	BKEN	PWM3B	PWM2B	PWM1B	PWM0B	00000000B
PWM3L	PWM 3 low bits register	DEH	PWM3.7	PWM3.6	PWM3.5	PWM3.4	PWM3.3	PWM3.2	PWM3.1	PWM3.0	00000000B
PWM2L	PWM 2 low bits register	DDH	PWM2.7	PWM2.6	PWM2.5	PWM2.4	PWM2.3	PWM2.2	PWM2.1	PWM2.0	00000000B
PWMCON1	PWM control register 1	DCH	PWMRUN	load	PWMF	CLRPWM	PWM3I	PWM2I	PWM1I	PWM0I	00000000B
PWM1L	PWM 1 low bits register	DBH	PWM1.7	PWM1.6	PWM1.5	PWM1.4	PWM1.3	PWM1.2	PWM1.1	PWM1.0	00000000B
PWM0L	PWM 0 low bits register	DAH	PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0	00000000B
PWMPL	PWM counter low register	D9H	PWMP0.7	PWMP0.6	PWMP0.5	PWMP0.4	PWMP0.3	PWMP0.2	PWMP0.1	PWMP0.0	00000000B
WDCON	Watch-Dog control	D8H	(DF) WDRUN	(DE) -	(DD) WD1	(DC) WD0	(DB) WDIF	(DA) WTRF	(D9) EWRST	(D8) WDCLR	External reset: 0x00 0000B Watchdog reset: 0x00 0100B Power on reset 0x000000B
PWMCON3	PWM control register 3	D7H	-	-	-	-	FP1	FP0	-	BKF	xxxx00x0B
PWM3H	PWM 3 high bits register	D6H	-	-	-	-	-	-	PWM3.9	PWM3.8	xxxxxx00B
PWM2H	PWM 2 high bits register	D5H	-	-	-	-	-	-	PWM2.9	PWM2.8	xxxxxx00B
PWM1H	PWM 1 high bits register	D3H	-	-	-	-	-	-	PWM1.9	PWM1.8	xxxxxx00B
PWM0H	PWM 0 high bits register	D2H	-	-	-	-	-	-	PWM0.9	PWM0.8	xxxxxx00B
PWMPH	PWM counter high register	D1H	-	-	-	-	-	-	PWMP0.9	PWMP0.8	00000000B
PSW	Program status word	D0H	(D7) CY	(D6) AC	(D5) F0	(D4) RS1	(D3) RS0	(D2) OV	(D1) F1	(D0) P	00000000B
NVMDATA	NVM Data	CFH									00000000B
NVMCON	NVM Control	CEH	EER	EWR	-	-	-	-	-	-	00xxxxxxB
TA	Timed Access Protection	C7H	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0	11111111B
NVMADDRL	NVM low byte address	C6H	-	NVMADDR.6	NVMADDR.5	NVMADDR.4	NVMADDR.3	NVMADDR.2	NVMADDR.1	NVMADDR.0	00000000B
IP0	Interrupt priority	B8H	(BF) -	(BE) PADC	(BD) PBO	(BC) -	(BB) PT1	(BA) PX1	(B9) PT0	(B8) PX0	x00x0000B

BIT	NAME	FUNCTION
7	TF1	Timer 1 Overflow Flag. This bit is set when Timer 1 overflows. It is cleared automatically when the program does a timer 1 interrupt service routine. Software can also set or clear this bit.
6	TR1	Timer 1 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
5	TF0	Timer 0 Overflow Flag. This bit is set when Timer 0 overflows. It is cleared automatically when the program does a timer 0 interrupt service routine. Software can also set or clear this bit.
4	TR0	Timer 0 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
3	IE1	Interrupt 1 Edge Detect Flag: Set by hardware when an edge/level is detected on $\overline{INT1}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
2	IT1	Interrupt 1 Type Control. Set/cleared by software to specify falling edge/ low level triggered external inputs.
1	IE0	Interrupt 0 Edge Detect Flag. Set by hardware when an edge/level is detected on $\overline{INT0}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
0	IT0	Interrupt 0 Type Control: Set/cleared by software to specify falling edge/ low level triggered external inputs.

TIMER MODE CONTROL

Bit:	7	6	5	4	3	2	1	0
	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
	TIMER1				TIMER0			

Mnemonic: TMOD Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer/counter 1 is enabled only while the $\overline{INT1}$ pin is high and the TR1 control bit is set. When cleared, the $\overline{INT1}$ pin has no effect, and Timer 1 is enabled whenever TR1 control bit is set.
6	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 1 is incremented by the internal clock. When set, the timer counts falling edges on the T1 pin.
5	M1	Timer 1 mode select bit 1. See table below.
4	M0	Timer 1 mode select bit 0. See table below.
3	GATE	Gating control: When this bit is set, Timer/counter 0 is enabled only while the $\overline{INT0}$ pin is high and the TR0 control bit is set. When cleared, the $\overline{INT0}$ pin has no effect, and Timer 0 is enabled whenever TR0 control bit is set.
2	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 0 is incremented by the internal clock. When set, the timer counts falling edges on the T0 pin.
1	M1	Timer 0 mode select bit 1. See table below.
0	M0	Timer 0 mode select bit 0. See table below.

M1, M0: Mode Select bits:

M1	M0	MODE
0	0	Mode 0: 13-bits timer/counter; THx 8 bits and TLx 5 bits which serve as pre-scalar.

1	P2.1	XTAL1 clock input pin.
0	P2.0	XTAL2 or CLKOUT pin by alternative.

Note: During power-on-reset, the port pins are tri-stated. After power-on-reset, the value of the port is set by CONFIG0.PRHI bit. The default setting for CONFIG0.PRHI =1 which the alternative function output is turned on upon reset. If CONFIG0.PRHI is set to 0, the user has to write a 1 to port SFR to turn on the alternative function output.

AUX FUNCTION REGISTER 1

Bit:	7	6	5	4	3	2	1	0
	EDF	BOD	BOI	LPBOV	SRST	ADCEN	BUZE	-

Mnemonic: AUXR1 Address: A2h

BIT	NAME	FUNCTION
7	EDF	Edge detect Interrupt Flag: 1: When any pin of port 1.0-1.2 that is enabled for the Edge Detect Interrupt function trigger (falling/rising edge trigger configurable). Must be cleared by software.
6	BOD	Brown Out Disable: 0: Enable Brownout Detect function. 1: Disable Brownout Detect function and save power.
5	BOI	Brown Out Interrupt: 0: Disable Brownout Detect Interrupt function and it will cause chip reset when BOF is set. 1: This prevents Brownout Detection from causing a chip reset and allows the Brownout Detect function to be used as an interrupt.
4	LPBOV	Low Power Brown Out Detect control: 0: When BOD is enable, the Brown Out detect is always turned on by normal run or Power-down mode. 1: When BOD is enable, the Brown Out detect circuit is turned on by Power-down mode. This control can help save 15/16 of the Brownout circuit power. When uC is in Power-down mode, the BOD will enable internal RC OSC (600KHz+/- 50%)
3	SRST	Software reset: 1: reset the chip as if a hardware reset occurred.
2	ADCEN	0: Disable ADC circuit. 1: Enable ADC circuit.
1	BUZE	Square-wave enable bit: 0: Disable square wave output. 1: The square wave is output to the BUZ (P1.0) pin.
0	-	Reserved.

EDGE DETECT CONTROL REGISTER

Bit:	7	6	5	4	3	2	1	0
	EDFILT.1	EDFILT.0	ED2TRG	ED2EN	ED1TRG	ED1EN	ED0TRG	ED0EN

Mnemonic: EDIC Address: A3h

BIT	NAME	FUNCTION
7	EA	Global enable. Enable/Disable all interrupts.
6	EADC	Enable ADC interrupt.
5	EBO	Enable Brown Out interrupt.
4	-	Reserved.
3	ET1	Enable Timer 1 interrupt.
2	EX1	Enable external interrupt 1.
1	ET0	Enable Timer 0 interrupt.
0	EX0	Enable external interrupt 0.

PORT 0 OUTPUT MODE 1

Bit:	7	6	5	4	3	2	1	0
	P0M1.7	P0M1.6	P0M1.5	P0M1.4	P0M1.3	P0M1.2	P0M1.1	P0M1.0

Mnemonic: P0M1 Address: B1h

BIT	NAME	FUNCTION
7-0	P0M1.[7:0]	To control the output configuration of P0 bits [7:0]

PORT 0 OUTPUT MODE 2

Bit:	7	6	5	4	3	2	1	0
	P0M2.7	P0M2.6	P0M2.5	P0M2.4	P0M2.3	P0M2.2	P0M2.1	P0M2.0

Mnemonic: P0M2 Address: B2h

BIT	NAME	FUNCTION
7-0	P0M2.[7:0]	To control the output configuration of P0 bits [7:0]

PORT 1 OUTPUT MODE 1

Bit:	7	6	5	4	3	2	1	0
	P1M1.7	P1M1.6	-	P1M1.4	P1M1.3	P1M1.2	P1M1.1	P1M1.0

Mnemonic: P1M1 Address: B3h

BIT	NAME	FUNCTION
7-0	P1M1.[7:0]	To control the output configuration of P1 bits [7:0]

PORT 1 OUTPUT MODE 2

Bit:	7	6	5	4	3	2	1	0
	P1M2.7	P1M2.6	-	P1M2.4	P1M2.3	P1M2.2	P1M2.1	P1M2.0

Mnemonic: P1M2 Address: B4h

BIT	NAME	FUNCTION
7-0	P1M2.[7:0]	To control the output configuration of P1 bits [7:0]

PORT 2 OUTPUT MODE 1

Bit:	7	6	5	4	3	2	1	0

7~0	PWM1.[7:0]	PWM 1 Low Bits Register.

PWM CONTROL REGISTER 1

Bit:	7	6	5	4	3	2	1	0
	PWMRUN	Load	PWMF	CLRPWM	-	-	PWM1I	PWM0I

Mnemonic: PWMCON1 Address: DCh

BIT	NAME	FUNCTION
7	PWMRUN	0: The PWM is not running. 1: The PWM counter is running.
6	Load	0: The registers value of PWMP and PWMn are never loaded to counter and Comparator registers. 1: The PWMP and PWMn registers load value to counter and compare registers at the counter underflow. This bit is auto cleared by hardware at next clock cycle.
5	PWMF	PWM underflow flag: 0: The 10-bit counter down count is not underflow. 1: The 10-bit counter down count is underflow. (PWM interrupt is requested if PWM interrupt is enabled). This bit is Software clear.
4	CLRPWM	1: Clear 10-bit PWM counter to 000H. This bit is auto cleared by hardware.
3	PWM3I	0: PWM3 out is non-inverted. 1: PWM3 output is inverted.
2	PWM2I	0: PWM2 out is non-inverted. 1: PWM2 output is inverted.
1	PWM1I	0: PWM1 out is non-inverted. 1: PWM1 output is inverted.
0	PWM0I	0: PWM0 out is non-inverted. 1: PWM0 output is inverted.

PWM2 LOW BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	PWM2.7	PWM2.6	PWM2.5	PWM2.4	PWM2.3	PWM2.2	PWM2.1	PWM2.0

Mnemonic: PWM2L Address: DDh

BIT	NAME	FUNCTION
7~0	PWM2.[7:0]	PWM 2 Low Bits Register.

Brake Condition Table:

BPEN	BKCH	BRAKE CONDITION
0	0	Brake On (software brake and keeping brake). Software brake condition. When active (BPEN=BKCH=0, and BKEN=1), PWM output follows PWMnB setting. This brake has no effect on PWMRUN bit, therefore, internal PWM generator continues to run. When the brake is released, the state of PWM output depends on the current state of PWM generator output during the release.
0	1	Brake On; This condition is when BKEN set (BKEN=1) and PWM is not running (PWMRUN=0), the PWMn output follows PWMnB setting. When the brake is released (by disabling BKEN = 0), the PWMn output resumes to the state when PWM generator stop running prior to enabling the brake. Brake Off; This condition is when PWM is running (PWMRUN=1).
1	0	Brake On, when Brake Pin asserted. External pin brake condition. When active (by external pin), PWM output follows PWMnB setting, PWMRUN will be cleared by hardware, and BKF flag will be set. When the brake is released (by de-asserting the external pin and disabling BKEN = 0), the PWM output resumes to the state of the PWM generator output prior to the brake.
1	1	This is another brake condition (by Brake Pin) which causes BKF to be set, but PWM generator continues to run. The PWM output does not follow PWMnB, instead it output continuously as per normal.

ACCUMULATOR

Bit:	7	6	5	4	3	2	1	0
	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0

Mnemonic: ACC Address: E0h

BIT	NAME	FUNCTION
7-0	ACC.[7:0]	The A or ACC register is the standard 8052 accumulator

ADC CONTROL REGISTER

Bit:	7	6	5	4	3	2	1	0
	ADC.1	ADC.0	ADCEX	ADCI	ADCS	RCCLK	AADR1	AADR0

Mnemonic: ADCCON Address: E1h

BIT	NAME	FUNCTION
7	PED	1: To set interrupt priority of Edge Detect is higher priority level.
6	PPWM	1: To set interrupt priority of PWM underflow is higher priority level.
5	PBK	1: To set interrupt priority of PWM's external brake is higher priority level.
4	PWDI	1: To set interrupt priority of Watchdog is higher priority level.
3-0	-	Reserved.

BUZZER CONTROL REGISTER

Bit:	7	6	5	4	3	2	1	0
	-	-	BUZDIV.5	BUZDIV.4	BUZDIV.3	BUZDIV.2	BUZDIV.1	BUZDIV.0

Mnemonic: BUZCON Address: F9h

BIT	NAME	FUNCTION
7-6	-	Reserved.
5-0	BUZDIV	Buzzer division select bits: These bits are division selector. User may configure these bits to further divide the cpu clock in order to generate the desired buzzer output frequency. The following shows the equation for the buzzer output rate; Fbuz = Fcpu x 1/[(256)x(BUZDIV + 1)]

9. INSTRUCTION SET

The W79E8213 series execute all the instructions of the standard 8052 family. The operations of these instructions, as well as their effects on flag and status bits, are exactly the same. However, the timing of these instructions is different in two ways. Firstly, the machine cycle is four clock periods, while the standard-8051/52 machine cycle is twelve clock periods. Secondly, it can fetch only once per machine cycle (i.e., four clocks per fetch), while the standard 8051/52 can fetch twice per machine cycle (i.e., six clocks per fetch).

The timing differences create an advantage for the W79E8213 series. There is only one fetch per machine cycle, so the number of machine cycles is usually equal to the number of operands in the instruction. (Jumps and calls do require an additional cycle to calculate the new address.) As a result, the W79E8213 series reduces the number of dummy fetches and wasted cycles, and therefore improves overall efficiency, compared to the standard 8051/52.

Op-code	HEX Code	Bytes	W79E8213 series Machine Cycle	W79E8213 series Clock cycles	8032 Clock cycles	W79E8213 series v.s. 8032 Speed Ratio
NOP	00	1	1	4	12	3
ADD A, R0	28	1	1	4	12	3
ADD A, R1	29	1	1	4	12	3
ADD A, R2	2A	1	1	4	12	3
ADD A, R3	2B	1	1	4	12	3
ADD A, R4	2C	1	1	4	12	3
ADD A, R5	2D	1	1	4	12	3
ADD A, R6	2E	1	1	4	12	3
ADD A, R7	2F	1	1	4	12	3
ADD A, @R0	26	1	1	4	12	3
ADD A, @R1	27	1	1	4	12	3
ADD A, direct	25	2	2	8	12	1.5
ADD A, #data	24	2	2	8	12	1.5
ADDC A, R0	38	1	1	4	12	3
ADDC A, R1	39	1	1	4	12	3
ADDC A, R2	3A	1	1	4	12	3
ADDC A, R3	3B	1	1	4	12	3
ADDC A, R4	3C	1	1	4	12	3
ADDC A, R5	3D	1	1	4	12	3
ADDC A, R6	3E	1	1	4	12	3
ADDC A, R7	3F	1	1	4	12	3
ADDC A, @R0	36	1	1	4	12	3
ADDC A, @R1	37	1	1	4	12	3
ADDC A, direct	35	2	2	8	12	1.5

INSTRUCTION SET, continued

Op-code	HEX Code	Bytes	W79E8213 series Machine Cycle	W79E8213 series Clock cycles	8032 Clock cycles	W79E8213 series v.s. 8032 Speed Ratio
ADDC A, #data	34	2	2	8	12	1.5
SUBB A, R0	98	1	1	4	12	3
SUBB A, R1	99	1	1	4	12	3
SUBB A, R2	9A	1	1	4	12	3
SUBB A, R3	9B	1	1	4	12	3
SUBB A, R4	9C	1	1	4	12	3
SUBB A, R5	9D	1	1	4	12	3
SUBB A, R6	9E	1	1	4	12	3
SUBB A, R7	9F	1	1	4	12	3
SUBB A, @R0	96	1	1	4	12	3
SUBB A, @R1	97	1	1	4	12	3
SUBB A, direct	95	2	2	8	12	1.5
SUBB A, #data	94	2	2	8	12	1.5
INC A	04	1	1	4	12	3
INC R0	08	1	1	4	12	3
INC R1	09	1	1	4	12	3
INC R2	0A	1	1	4	12	3
INC R3	0B	1	1	4	12	3
INC R4	0C	1	1	4	12	3
INC R5	0D	1	1	4	12	3
INC R6	0E	1	1	4	12	3
INC R7	0F	1	1	4	12	3
INC @R0	06	1	1	4	12	3
INC @R1	07	1	1	4	12	3
INC direct	05	2	2	8	12	1.5
INC DPTR	A3	1	2	8	24	3
DEC A	14	1	1	4	12	3
DEC R0	18	1	1	4	12	3
DEC R1	19	1	1	4	12	3
DEC R2	1A	1	1	4	12	3
DEC R3	1B	1	1	4	12	3
DEC R4	1C	1	1	4	12	3
DEC R5	1D	1	1	4	12	3
DEC R6	1E	1	1	4	12	3

10. POWER MANAGEMENT

The W79E8213 series has several features that help the user to control the power consumption of the device. These modes are discussed in the next two sections.

10.1 Idle Mode

The user can put the device into idle mode by writing 1 to the bit PCON.0. The instruction that sets the idle bit is the last instruction that will be executed before the device goes into Idle Mode. In the Idle mode, the clock to the CPU is halted, but not to the Interrupt, Timer, PWM and Watchdog timer blocks. This forces the CPU state to be frozen; the Program counter, the Stack Pointer, the Program Status Word, the Accumulator and the other registers hold their contents. The port pins hold the logical states they had at the time Idle was activated. The Idle mode can be terminated in two ways. Since the interrupt controller is still active, the activation of any enabled interrupt can wake up the processor. This will automatically clear the Idle bit, terminate the Idle mode, and the Interrupt Service Routine (ISR) will be executed. After the ISR, execution of the program will continue from the instruction which put the device into Idle Mode.

The Idle mode can also be exited by activating the reset. The device can put into reset either by applying a low on the external /RST pin, a Power on reset condition or a Watchdog timer reset. The external reset pin has to be held low for at least two machine cycles i.e. 8 clock periods to be recognized as a valid reset. In the reset condition the program counter is reset to 0000h and all the SFRs are set to the reset condition. Since the clock is already running there is no delay and execution starts immediately. In the Idle mode, the Watchdog timer continues to run, and if enabled, a time-out will cause a watchdog timer interrupt which will wake up the device. The software must reset the Watchdog timer in order to preempt the reset which will occur after 512 clock periods of the time-out. When the W79E8213 series are exiting from an Idle Mode with a reset, the instruction following the one which put the device into Idle Mode is not executed. So there is no danger of unexpected writes.

10.2 Power-down Mode

The device can be put into Power-down mode by writing 1 to bit PCON.1. The instruction that does this will be the last instruction to be executed before the device goes into Power-down mode. In the Power-down mode, all the clocks are stopped and the device comes to a halt. All activity is completely stopped and the power consumption is reduced to the lowest possible value. The port pins output the values held by their respective SFRs.

The W79E8213 series will exit the Power-down mode with a reset or by an external interrupt pin enabled as level detected. An external reset can be used to exit the Power down state. The low on /RST pin terminates the Power-down mode, and restarts the clock. The program execution will restart from 0000h. In the Power-down mode, the clock is stopped, so the Watchdog timer cannot be used to provide the reset to exit Power-down mode when its clock source is external OSC or crystal.

The sources that can wake up from the power-down mode are external interrupts, brownout reset (BOR) and ADC. Note that for ADC waking up from powerdown, the device need to run on internal rc and software perform start ADC prior to powerdown.

The W79E8213 series can be waken up from the Power-down mode by forcing an external interrupt pin activation, provided the corresponding interrupt is enabled, while the global enable (EA) bit is set. If these conditions are met, then either a low-level or a falling-edge at external interrupt pin will re-start the oscillator. The device will then execute the interrupt service routine for the corresponding external interrupt. After the interrupt service routine is completed, the program execution returns to the instruction after one which put the device into Power-down mode and continues from there. During Power-down mode, if AUXR1.LPBOV = 1 and AUXR1.BOD = 0, the internal RC clock will be enabled and hence save power.

12. INTERRUPTS

The W79E8213 series have four priority level interrupts structure with 10 interrupt sources. Each of the interrupt sources has an individual priority bit, flag, interrupt vector and enable bit. In addition, the interrupts can be globally enabled or disabled.

12.1 Interrupt Sources

The External Interrupts $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ can be either edge triggered or level triggered, programmable through bits IT0 and IT1. The bits IE0 and IE1 in the TCON register are the flags which are checked to generate the interrupt. In the edge triggered mode, the INTx inputs are sampled in every machine cycle. If the sample is high in one cycle and low in the next, then a high to low transition is detected and the interrupts request flag IEx in TCON is set. The flag bit requests the interrupt. Since the external interrupts are sampled every machine cycle, they have to be held high or low for at least one complete machine cycle. The IEx flag is automatically cleared when the service routine is called. If the level triggered mode is selected, then the requesting source has to hold the pin low till the interrupt is serviced. The IEx flag will not be cleared by the hardware on entering the service routine. If the interrupt continues to be held low even after the service routine is completed, then the processor may acknowledge another interrupt request from the same source.

The Timer 0 and 1 Interrupts are generated by the TF0 and TF1 flags. These flags are set by the overflow in the Timer 0 and Timer 1. The TF0 and TF1 flags are automatically cleared by the hardware when the timer interrupt is serviced.

The Watchdog timer can be used as a system monitor or a simple timer. In either case, when the time-out count is reached, the Watchdog Timer interrupt flag WDIF (WDCON.3) is set. If the interrupt is enabled by the enable bit EIE.4, then an interrupt will occur.

PWM interrupt is generated when its' 10-bit down counter underflows. PWMF flag is set and PWM interrupt is generated if enabled. PWMF is set by hardware and can only be cleared by software. Alternatively, PWM function can also generate interrupt by BKF flag, after external brake pin has brake occurred. This bit will be cleared by software.

The ADC can generate interrupt after finished ADC converter. There is one interrupt source, which is obtained by the ADCI bit in the ADCCON SFR. This bit is not automatically cleared by the hardware, and the user will have to clear this bit using software.

Edge detect interrupt is generated when any of the keypad connected to P1.0-P1.2 pins is pressed. Each edge detect interrupt can be individually enabled/disabled. User will have to software clear the flag bit. The ED pins have edge type and filter type control, configurable through EDIC SFR.

Brownout detect can cause brownout flag, BOF, to be asserted if power voltage drop below brownout voltage level. Interrupt will occur if BOI (AUXR1.5), EBO (IE.5) and global interrupt enable are set.

All the bits that generate interrupts can be set or reset by software, and thereby software initiated interrupts can be generated. Each of the individual interrupts can be enabled or disabled by setting or clearing a bit in the IE SFR. IE also has a global enable/disable bit EA, which can be cleared to disable all interrupts.

The interrupt flags are sampled every machine cycle. In the same machine cycle, the sampled interrupts are polled and their priority is resolved. If certain conditions are met then the hardware will execute an internally generated LCALL instruction which will vector the process to the appropriate interrupt vector address. The conditions for generating the LCALL are;

1. An interrupt of equal or higher priority is not currently being serviced.

2. The current polling cycle is the last machine cycle of the instruction currently being execute.

3. The current instruction does not involve a write to IE, EIE, IP0, IP0H, IP1 or IPH1 registers and is not a RETI.

If any of these conditions are not met, then the LCALL will not be generated. The polling cycle is repeated every machine cycle, with the interrupts sampled in the same machine cycle. If an interrupt

flag is active in one cycle but not responded to, and is not active when the above conditions are met, the denied interrupt will not be serviced. This means that active interrupts are not remembered; every polling cycle is new.

The processor responds to a valid interrupt by executing an LCALL instruction to the appropriate service routine. This may or may not clear the flag which caused the interrupt. In case of Timer interrupts, the TF0 or TF1 flags are cleared by hardware whenever the processor vectors to the appropriate timer service routine. In case of external interrupt, INT0 and INT1, the flags are cleared only if they are edge triggered. In case of Serial interrupts, the flags are not cleared by hardware. The Watchdog timer interrupt flag WDIF has to be cleared by software. The hardware LCALL behaves exactly like the software LCALL instruction. This instruction saves the Program Counter contents onto the Stack, but does not save the Program Status Word PSW. The PC is reloaded with the vector address of that interrupt which caused the LCALL. These address of vector for the different sources are as following:

VECTOR LOCATIONS FOR INTERRUPT SOURCES

SOURCE	VECTOR ADDRESS	SOURCE	VECTOR ADDRESS
External Interrupt 0	0003h	Timer 0 Overflow	000Bh
External Interrupt 1	0013h	Timer 1 Overflow	001Bh
-	0023h	Brownout Interrupt	002Bh
-	0033h	Edge Detect Interrupt	003Bh
-	0043h	-	004Bh
Watchdog Timer	0053h	ADC Interrupt	005Bh
-	0063h	PWM Brake Interrupt	0073h
PWM Underflow Interrupt	006Bh	-	007Bh

Table 12-1: Vector locations for interrupt sources

Execution continues from the vectored address till an RETI instruction is executed. On execution of the RETI instruction the processor pops the Stack and loads the PC with the contents at the top of the stack. The user must take care that the status of the stack is restored to what it was after the hardware LCALL, if the execution is return to the interrupted program. The processor does not notice anything if the stack contents are modified and will proceed with execution from the address put back into PC. Note that a RET instruction would perform exactly the same process as a RETI instruction, but it would not inform the Interrupt Controller that the interrupt service routine is completed, and would leave the controller still thinking that the service routine is underway.

Example 5: Invalid Access

```
MOV     TA, #0AAh       ; 3 M/C
NOP                     ; 1 M/C
MOV     TA, #055h       ; 3 M/C
SETB    EWT             ; 2 M/C
```

In the first three examples, the writing to the protected bits is done before the 3 machine cycles window closes. In Example 4, however, the writing to the protected bit occurs after the window has closed, and so there is effectively no change in the status of the protected bit. In Example 5, the second write to TA occurs 4 machine cycles after the first write, therefore the timed access window is not opened at all, and the write to the protected bit fails.

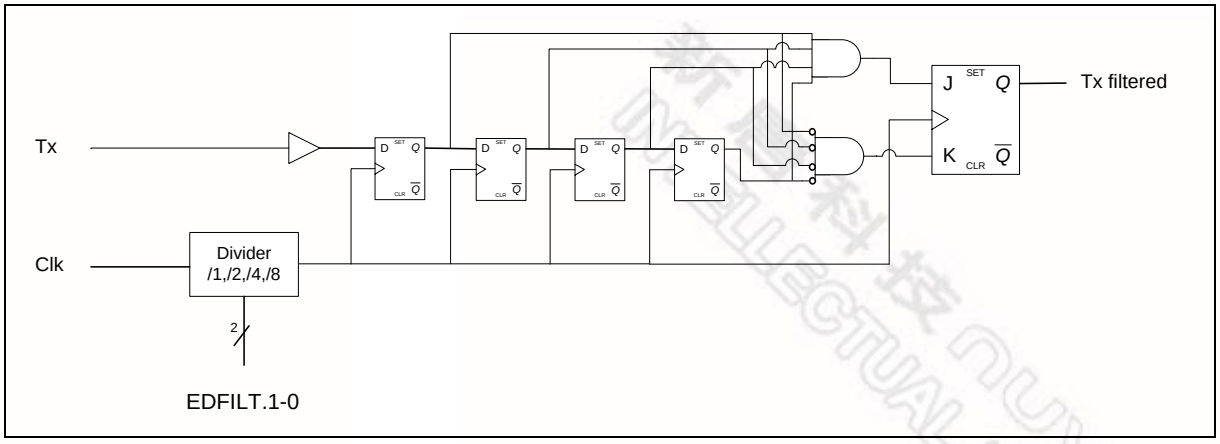
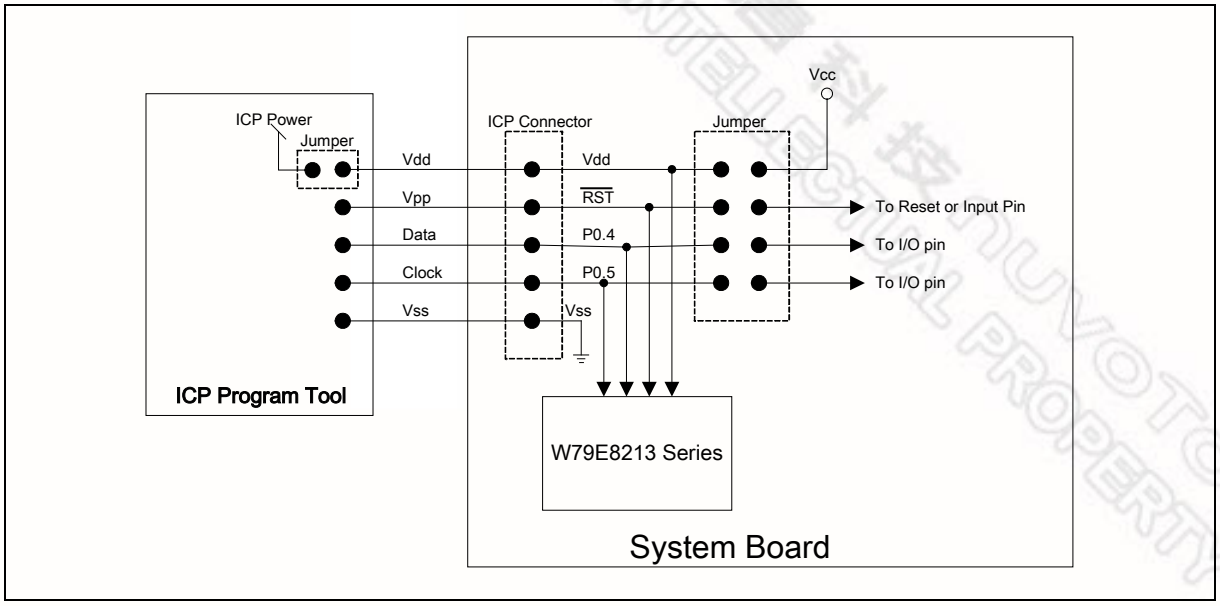


Figure 17-2: Edge Detect Noise Filter

24. ICP (IN-CIRCUIT PROGRAM) FLASH PROGRAM

The contexts of flash in W79E8213 series are empty by default. At the first use, you must program the flash EPROM by external Writer device or by ICP (In-Circuit Program) tool.



Note:

1. When using ICP to upgrade code, the P1.5, P0.4 and P0.5 must be taken within design system board.
2. After program finished by ICP, to suggest system power must power off and remove ICP connector then power on.
3. It is recommended that user performs erase function and programming configure bits continuously without any interruption.
4. During ICP mode, all PWM pins will be tri-stated.

DC ELECTRICAL CHARACTERISTICS, continued

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Brownout voltage with BOV=1	$V_{BO2.5}$	2.4	-	2.7	V	TA = -0 to 70°C
Brownout voltage with BOV=0	$V_{BO3.8}$	3.5	-	4	V	TA = -0 to 70°C
ADC current consumption	I_{ADC}	-	0.4	0.8	mA	V_{DD} = 5.0V, ADCCLK = 4MHz
		-	0.25	0.5		V_{DD} = 3.0V, ADCCLK = 4MHz
Brownout voltage detect current	I_{BOD}	-	1.2	1.8	mA	V_{DD} = 5.0V
		-	0.8	1.2		V_{DD} = 3.0V

*1. /RST pin is a Schmitt trigger input.

*2. XTAL1 is a CMOS input.

*3. Pins of P0, P1 and P2 can source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when Vin approximates to 2V.

*4. Only one of the 8 pins sinks high current at a time.

26.3 The ADC Converter DC ELECTRICAL CHARACTERISTICS

(V_{DD}–V_{SS} = 3.0~5V, TA = -40~85°C, Fosc = 4MHz, unless otherwise specified.)

PARAMETER	SYMBOL	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Analog input	AVin	V_{SS}-0.2		V_{DD}+0.2	V	
ADC clock	ADCCLK	200KHz	-	5MHz	Hz	ADC block circuit input clock
Conversion time	t_C		$52t_{ADC}$ [1]		us	
Differential non-linearity	DNL	-1	-	+1	LSB	
Integral non-linearity	INL	-2	-	+2	LSB	
Offset error	Ofe	-1	-	+1	LSB	
Gain error	Ge	-1	-	+1	%	
Absolute voltage error	Ae	-3	-	+3	LSB	

Notes:

1. tADC: The period time of ADC input clock.