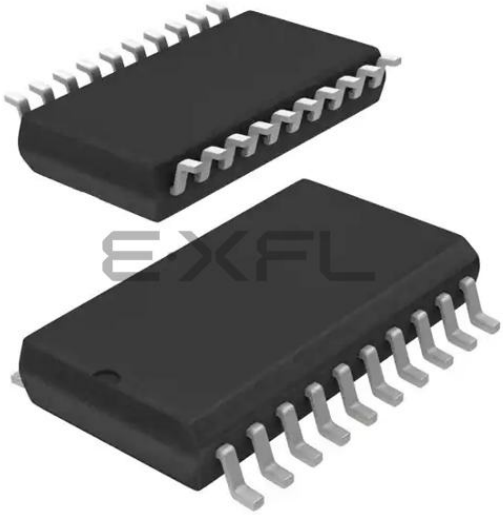

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	18
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w79e8213asg

3. PARTS INFORMATION LIST

3.1 Lead Free (RoHS) Parts information list

PART NO.	EPROM FLASH SIZE	RAM	NVM FLASH EPROM	INTERNAL RC [1] OSCILLATOR ACCURACY	PACKAGE
W79E8213AKG	4KB	128B	128B	±30%	DIP-20 Pin
W79E8213ASG	4KB	128B	128B	±30%	SOP-20 Pin
W79E8213RAKG	4KB	128B	128B	±2%	DIP-20 Pin
W79E8213RASG	4KB	128B	128B	±2%	SOP-20 Pin

Note: 1. Test conditions are V_{DD} = 3.3V, TA = 25°C

Table 3-1: Lead Free (RoHS) Parts information list

4. PIN CONFIGURATION

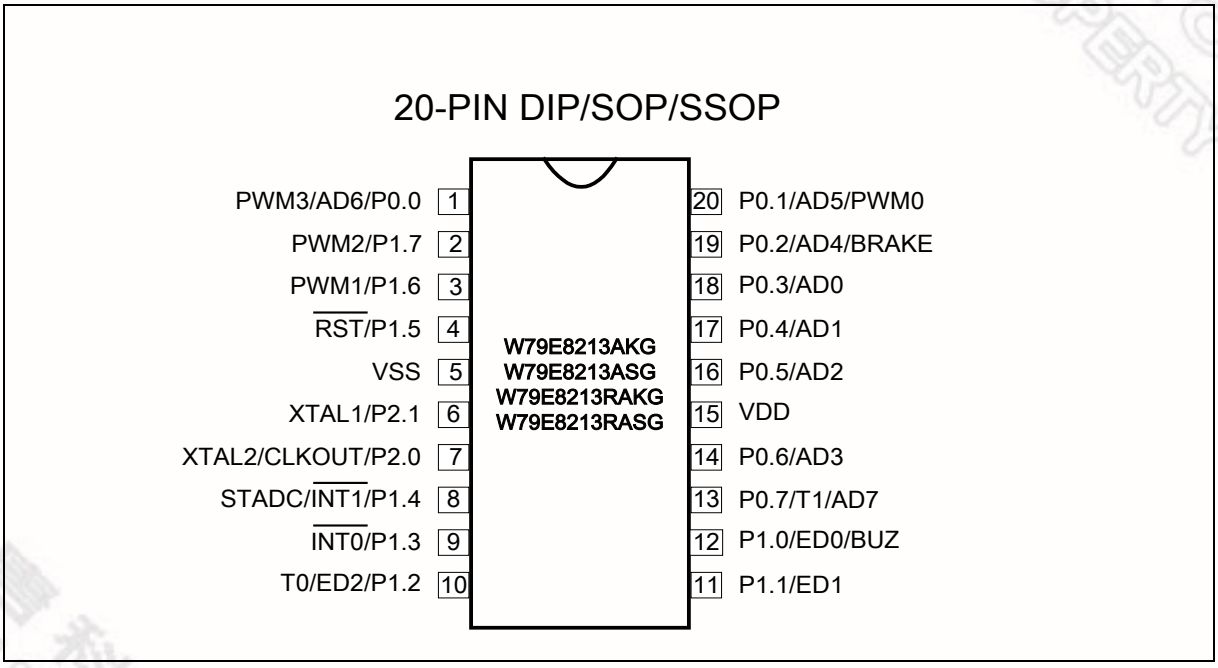


Figure 4-1: Pin Configuration

PWM3 LOW BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	PWM3.7	PWM3.6	PWM3.5	PWM3.4	PWM3.3	PWM3.2	PWM3.1	PWM3.0

Mnemonic: PWM3L Address: DEh

BIT	NAME	FUNCTION
7~0	PWM3.[7:0]	PWM 3 Low Bits Register.

PWM CONTROL REGISTER 2

Bit:	7	6	5	4	3	2	1	0
	BKCH	BKPS	BPEN	BKEN	PWM3B	PWM2B	PWM1B	PWM0B

Mnemonic: PWMCON2 Address: DFh

BIT	NAME	FUNCTION
7	BKCH	See the below table, when BKEN is set.
6	BKPS	0: Brake is asserted if P0.2 is low. 1: Brake is asserted if P0.2 is high
5	BPEN	See the below table, when BKEN is set.
4	BKEN	0: The Brake is never asserted. 1: The Brake is enabled, and see the below table.
3	PWM3B	0: The PWM3 output is low, when Brake is asserted. 1: The PWM3 output is high, when Brake is asserted.
2	PWM2B	0: The PWM2 output is low, when Brake is asserted. 1: The PWM2 output is high, when Brake is asserted.
1	PWM1B	0: The PWM1 output is low, when Brake is asserted. 1: The PWM1 output is high, when Brake is asserted.
0	PWM0B	0: The PWM0 output is low, when Brake is asserted. 1: The PWM0 output is high, when Brake is asserted.

Brake Condition Table:

BPEN	BKCH	BRAKE CONDITION
0	0	Brake On (software brake and keeping brake). Software brake condition. When active (BPEN=BKCH=0, and BKEN=1), PWM output follows PWMnB setting. This brake has no effect on PWMRUN bit, therefore, internal PWM generator continues to run. When the brake is released, the state of PWM output depends on the current state of PWM generator output during the release.
0	1	Brake On; This condition is when BKEN set (BKEN=1) and PWM is not running (PWMRUN=0), the PWMn output follows PWMnB setting. When the brake is released (by disabling BKEN = 0), the PWMn output resumes to the state when PWM generator stop running prior to enabling the brake. Brake Off; This condition is when PWM is running (PWMRUN=1).
1	0	Brake On, when Brake Pin asserted. External pin brake condition. When active (by external pin), PWM output follows PWMnB setting, PWMRUN will be cleared by hardware, and BKF flag will be set. When the brake is released (by de-asserting the external pin and disabling BKEN = 0), the PWM output resumes to the state of the PWM generator output prior to the brake.
1	1	This is another brake condition (by Brake Pin) which causes BKF to be set, but PWM generator continues to run. The PWM output does not follow PWMnB, instead it output continuously as per normal.

ACCUMULATOR

Bit:	7	6	5	4	3	2	1	0
	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0

Mnemonic: ACC Address: E0h

BIT	NAME	FUNCTION
7-0	ACC.[7:0]	The A or ACC register is the standard 8052 accumulator

ADC CONTROL REGISTER

Bit:	7	6	5	4	3	2	1	0
	ADC.1	ADC.0	ADCEX	ADCI	ADCS	RCCLK	AADR1	AADR0

Mnemonic: ADCCON Address: E1h

BIT	NAME	FUNCTION
7-6	ADC.1-0	2 LSB of 10-bit A/D conversion result.
5	ADCEX	Enable STADC-triggered conversion 0: Conversion can only be started by software (i.e., by setting ADCS). 1: Conversion can be started by software or by a rising edge on STADC (pin P1.4).
4	ADCI	ADC Interrupt flag: This flag is set when the result of an A/D conversion is ready. This generates an ADC interrupt, if it is enabled. The flag may be cleared by the ISR. While this flag is 1, the ADC cannot start a new conversion. ADCI can not be set by software.
3	ADCS	ADC Start and Status: Set this bit to start an A/D conversion. It may also be set by STADC if ADCEX is 1. This signal remains high while the ADC is busy and is reset right after ADCI is set. ***Note:*** ***1. It is recommended to clear ADCI before ADCS is set. However, if ADCI is cleared and ADCS is set at the same time, a new A/D conversion may start on the same channel.*** ***2. Software clearing of ADCS will abort conversion in progress.*** ***3. ADC cannot start a new conversion while ADCS is high.***
2	RCCLK	0: The CPU clock is used as ADC clock source. 1: The internal RC 10MHz/20MHz (selectable by CONFIG1.FS1 bit) clock is used as ADC clock source. ***Note:*** ***1. This bit can only be set/cleared when ADCEN=0.*** ***2. The ADC clock source will goes through pre-scalar of /1, /2, /4 or /8, selectable by ADCLK bits (SFR ADCCON1.6-7).***
1	AADR1	The ADC input select. See table below.
0	AADR0	The ADC input select. See table below.

The ADCI and ADCS control the ADC conversion as below:

ADCI	ADCS	ADC STATUS
0	0	ADC not busy; A conversion can be started.
0	1	ADC busy; Start of a new conversion is blocked.
1	0	Conversion completed; Start of a new conversion requires ADCI = 0.
1	1	This is an internal temporary state that user can ignore it.

BIT	NAME	FUNCTION
7	PED	1: To set interrupt priority of Edge Detect is higher priority level.
6	PPWM	1: To set interrupt priority of PWM underflow is higher priority level.
5	PBK	1: To set interrupt priority of PWM's external brake is higher priority level.
4	PWDI	1: To set interrupt priority of Watchdog is higher priority level.
3-0	-	Reserved.

BUZZER CONTROL REGISTER

Bit:	7	6	5	4	3	2	1	0
	-	-	BUZDIV.5	BUZDIV.4	BUZDIV.3	BUZDIV.2	BUZDIV.1	BUZDIV.0

Mnemonic: BUZCON Address: F9h

BIT	NAME	FUNCTION
7-6	-	Reserved.
5-0	BUZDIV	Buzzer division select bits: These bits are division selector. User may configure these bits to further divide the cpu clock in order to generate the desired buzzer output frequency. The following shows the equation for the buzzer output rate; Fbuz = Fcpu x 1/[(256)x(BUZDIV + 1)]

INSTRUCTION SET, continued

Op-code	HEX Code	Bytes	W79E8213 series Machine Cycle	W79E8213 series Clock cycles	8032 Clock cycles	W79E8213 series v.s. 8032 Speed Ratio
ADDC A, #data	34	2	2	8	12	1.5
SUBB A, R0	98	1	1	4	12	3
SUBB A, R1	99	1	1	4	12	3
SUBB A, R2	9A	1	1	4	12	3
SUBB A, R3	9B	1	1	4	12	3
SUBB A, R4	9C	1	1	4	12	3
SUBB A, R5	9D	1	1	4	12	3
SUBB A, R6	9E	1	1	4	12	3
SUBB A, R7	9F	1	1	4	12	3
SUBB A, @R0	96	1	1	4	12	3
SUBB A, @R1	97	1	1	4	12	3
SUBB A, direct	95	2	2	8	12	1.5
SUBB A, #data	94	2	2	8	12	1.5
INC A	04	1	1	4	12	3
INC R0	08	1	1	4	12	3
INC R1	09	1	1	4	12	3
INC R2	0A	1	1	4	12	3
INC R3	0B	1	1	4	12	3
INC R4	0C	1	1	4	12	3
INC R5	0D	1	1	4	12	3
INC R6	0E	1	1	4	12	3
INC R7	0F	1	1	4	12	3
INC @R0	06	1	1	4	12	3
INC @R1	07	1	1	4	12	3
INC direct	05	2	2	8	12	1.5
INC DPTR	A3	1	2	8	24	3
DEC A	14	1	1	4	12	3
DEC R0	18	1	1	4	12	3
DEC R1	19	1	1	4	12	3
DEC R2	1A	1	1	4	12	3
DEC R3	1B	1	1	4	12	3
DEC R4	1C	1	1	4	12	3
DEC R5	1D	1	1	4	12	3
DEC R6	1E	1	1	4	12	3

INSTRUCTION SET, continued

Op-code	HEX Code	Bytes	W79E8213 series Machine Cycle	W79E8213 series Clock cycles	8032 Clock cycles	W79E8213 series v.s 8032 Speed Ratio
MOV direct, R2	8A	2	2	8	12	1.5
MOV direct, R3	8B	2	2	8	12	1.5
MOV direct, R4	8C	2	2	8	12	1.5
MOV direct, R5	8D	2	2	8	12	1.5
MOV direct, R6	8E	2	2	8	12	1.5
MOV direct, R7	8F	2	2	8	12	1.5
MOV direct, @R0	86	2	2	8	12	1.5
MOV direct, @R1	87	2	2	8	12	1.5
MOV direct, direct	85	3	3	12	24	2
MOV direct, #data	75	3	3	12	24	2
MOV DPTR, #data 16	90	3	3	12	24	2
MOVC A, @A+DPTR	93	1	2	8	24	3
MOVC A, @A+PC	83	1	2	8	24	3
MOVX A, @R0	E2	1	2 - 9	8 - 36	24	3 - 0.66
MOVX A, @R1	E3	1	2 - 9	8 - 36	24	3 - 0.66
MOVX A, @DPTR	E0	1	2 - 9	8 - 36	24	3 - 0.66
MOVX @R0, A	F2	1	2 - 9	8 - 36	24	3 - 0.66
MOVX @R1, A	F3	1	2 - 9	8 - 36	24	3 - 0.66
MOVX @DPTR, A	F0	1	2 - 9	8 - 36	24	3 - 0.66
PUSH direct	C0	2	2	8	24	3
POP direct	D0	2	2	8	24	3
XCH A, R0	C8	1	1	4	12	3
XCH A, R1	C9	1	1	4	12	3
XCH A, R2	CA	1	1	4	12	3
XCH A, R3	CB	1	1	4	12	3
XCH A, R4	CC	1	1	4	12	3
XCH A, R5	CD	1	1	4	12	3
XCH A, R6	CE	1	1	4	12	3
XCH A, R7	CF	1	1	4	12	3
XCH A, @R0	C6	1	1	4	12	3
XCH A, @R1	C7	1	1	4	12	3
XCHD A, @R0	D6	1	1	4	12	3
XCHD A, @R1	D7	1	1	4	12	3
XCH A, direct	C5	2	2	8	12	1.5

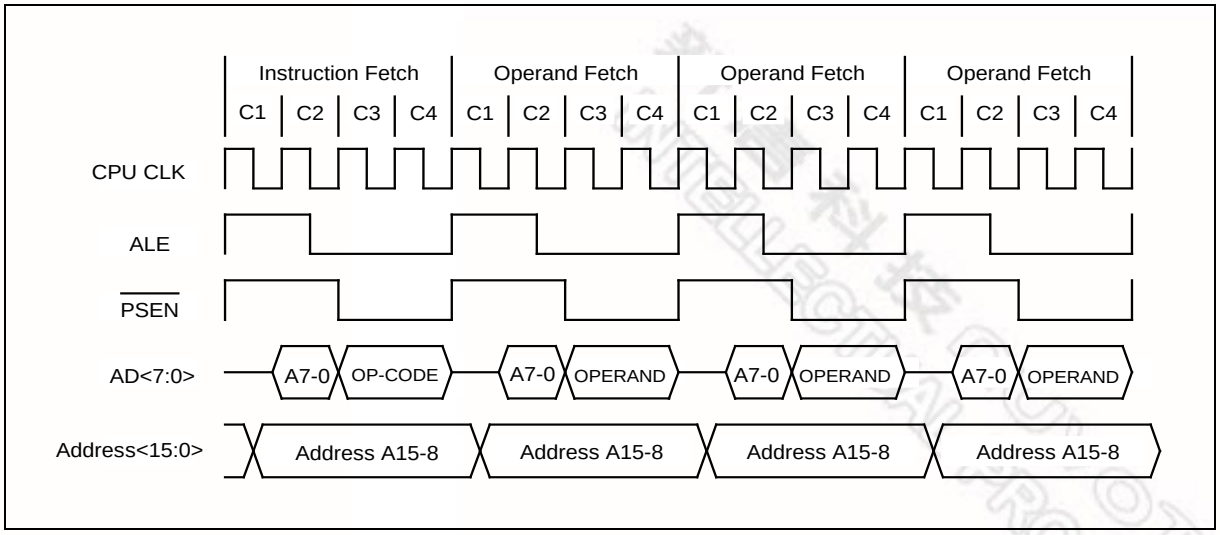


Figure 9-4: Four Cycles Instruction Timing

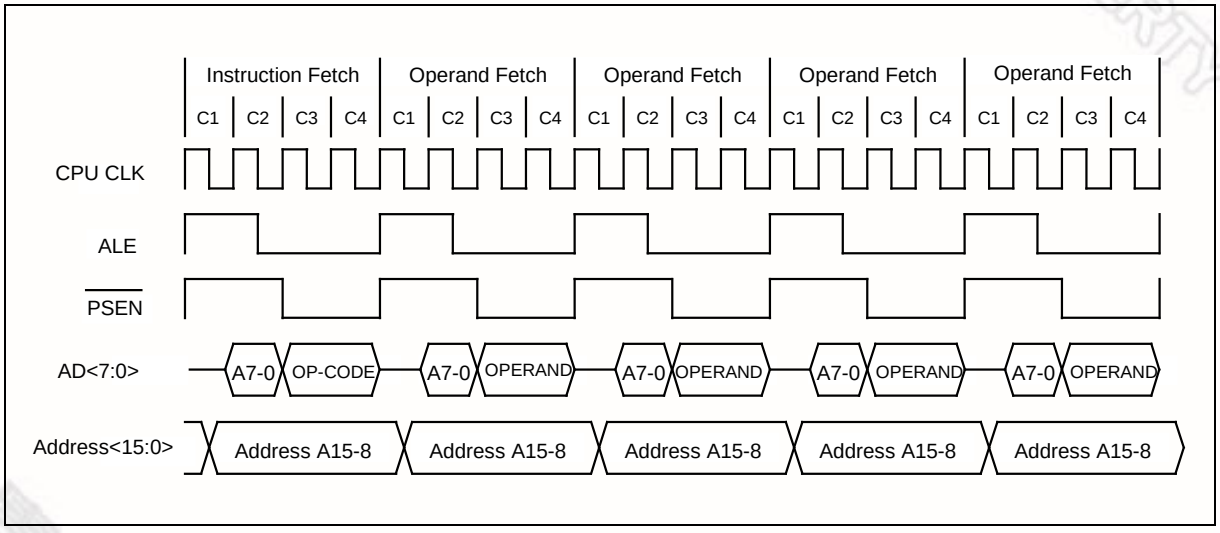


Figure 9-5: Five Cycles Instruction Timing

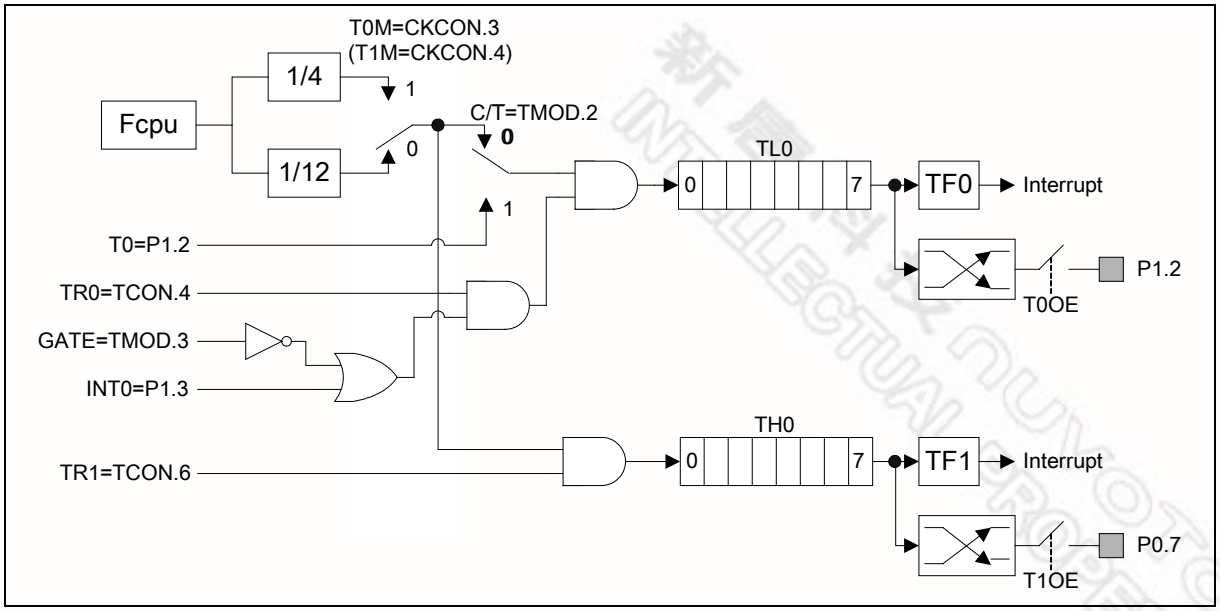


Figure 13-4: Timer/Counter Mode 3

14. NVM MEMORY

The W79E8213 series have NVM data memory of 128 bytes for customer's data store used. The NVM data memory has 8 pages area and each page of 16 bytes.

The NVM memory can be read/write by customer program to access. Read NVM data is by MOVC A,@A+DPTR instruction, and write data is by SFR of NVMADDRL, NVMDATA and NVMCON. Before write data to NVM memory, the page must be erased by providing page address on NVMADDRL, which address of On-Chip Code Memory space will decode, then set EER of NVMCON.7. This will automatically hold fetch program code and PC Counter, and execute page erase. After finished, this bit will be cleared by hardware. The erase time is ~ 5ms.

For writing data to NVM memory, user must set address and data to NVMADDRL and NVMDATA, then set EWR of NVMCON.6 to initiate nvm data write. The uC will hold program code and PC Counter, and then write data to mapping address. Upon write completion, the EWR bit will be cleared by hardware, the uC will continue execute next instruction. The program time is ~50us.

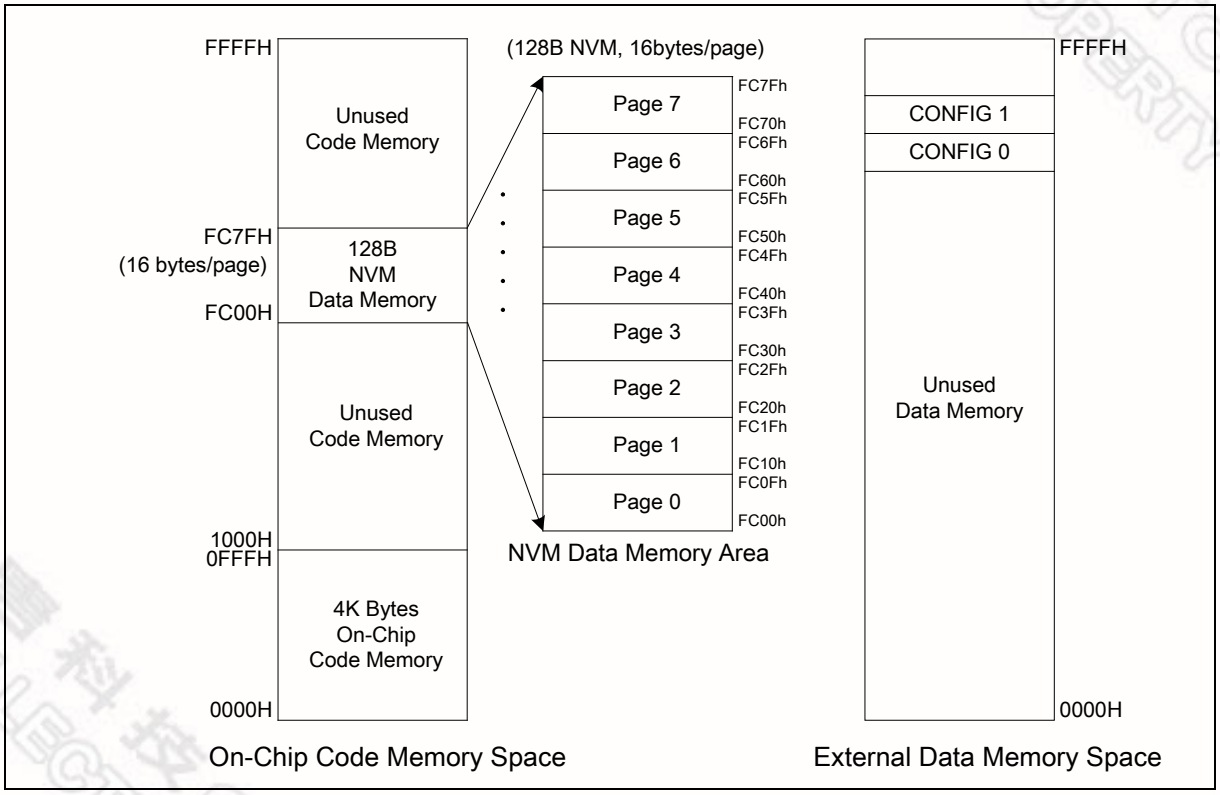


Figure 14-1: W79E8213 Memory Map

15. WATCHDOG TIMER

The Watchdog Timer is a free-running Timer which can be programmed by the user to serve as a system monitor, a time-base generator or an event timer. It is basically a set of dividers that divide the system clock. The divider output is selectable and determines the time-out interval. When the time-out occurs a flag is set, which can cause an interrupt if enabled, and a system reset can also be caused if it is enabled. The interrupt will occur if the individual interrupt enable and the global enable are set. The interrupt and reset functions are independent of each other and may be used separately or together depending on the user's software.

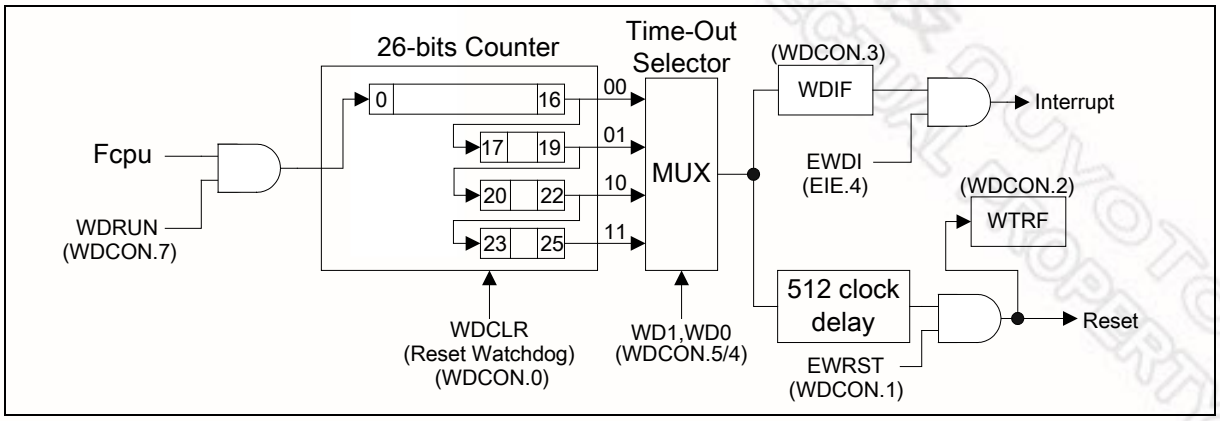


Figure 15-1: Watchdog Timer

The Watchdog Timer should first be restarted by using WDCLR. This ensures that the timer starts from a known state. The WDCLR bit is used to restart the Watchdog Timer. This bit is self clearing, i.e. after writing a 1 to this bit the software will automatically clear it. The Watchdog Timer will now count clock cycles. The time-out interval is selected by the two bits WD1 and WD0 (WDCON.5 and WDCON.4). When the selected time-out occurs, the Watchdog interrupt flag WDIF (WDCON.3) is set. After the time-out has occurred, the Watchdog Timer waits for an additional 512 clock cycles. If the Watchdog Reset EWRST (WDCON.1) is enabled, then 512 clocks after the time-out, if there is no WDCLR, a system reset due to Watchdog Timer will occur. This will last for two machine cycles, and the Watchdog Timer reset flag WTRF (WDCON.2) will be set. This indicates to the software that the Watchdog was the cause of the reset.

When used as a simple timer, the reset and interrupt functions are disabled. The timer will set the WDIF flag each time the timer completes the selected time interval. The WDIF flag is polled to detect a time-out and the WDCLR allows software to restart the timer. The Watchdog Timer can also be used as a very long timer. The interrupt feature is enabled in this case. Every time the time-out occurs an interrupt will occur if the global interrupt enable EA is set.

The main use of the Watchdog Timer is as a system monitor. This is important in real-time control applications. In case of some power glitches or electro-magnetic interference, the processor may begin to execute errant code. If this is left unchecked the entire system may crash. Using the watchdog timer interrupt during software development will allow the user to select ideal watchdog reset locations. The code is first written without the watchdog interrupt or reset. Then the Watchdog interrupt is enabled to identify code locations where interrupt occurs. The user can now insert instructions to reset the Watchdog Timer, which will allow the code to run without any Watchdog Timer interrupts. Now the Watchdog Timer reset is enabled and the Watchdog interrupt may be disabled. If any errant code is executed now, then the reset Watchdog Timer instructions will not be executed at the required instants and Watchdog reset will occur.

The Watchdog Timer time-out selection will result in different time-out values depending on the clock

19. OSCILLATOR

The W79E8213 series provides three oscillator input option. These are configured at CONFIG register (CONFIG0) that include Internal RC Oscillator Option, External Clock Input Option and Crystal Oscillator Input Option. The Crystal Oscillator Input frequency may be supported from 4MHz to 20MHz, and without capacitor or resister.

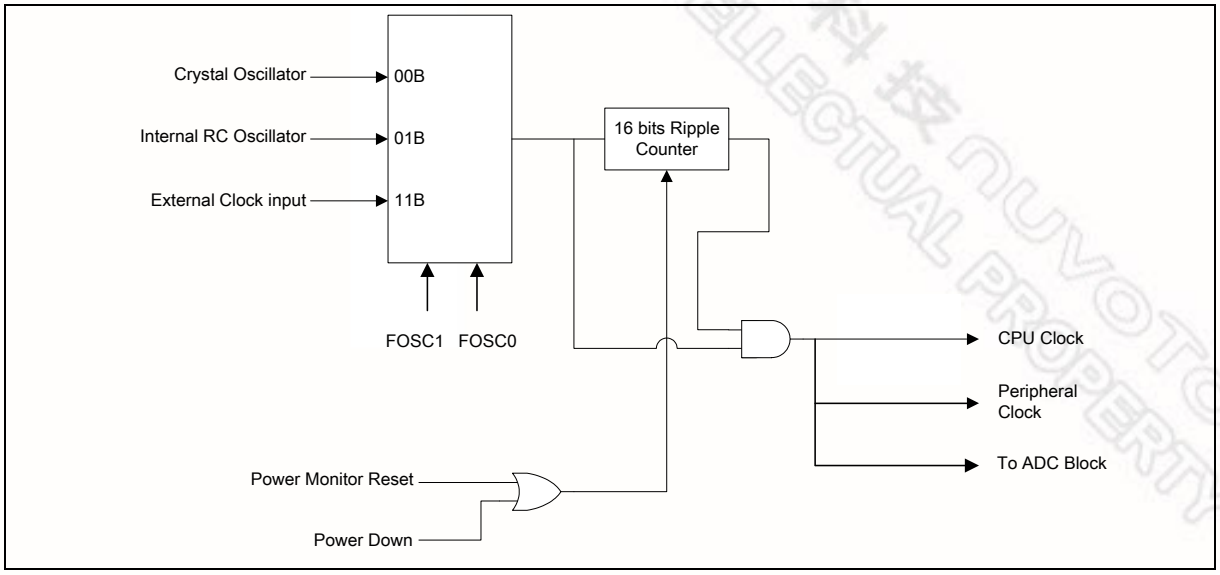


Figure 19-1: Oscillator

19.1 Internal RC Oscillator Option

The internal RC Oscillator is configurable to 10MHz/20MHz (through CONFIG1.FS1 bit) frequency to support clock source. When FOSC1, FOSC0 = 01b, the internal RC oscillator is enabled. A clock output on P2.0 (XTAL2) may be enabled when internal RC oscillator is used.

19.2 External Clock Input Option

The clock source pin (XTAL1) is from External Clock Input by FOSC1, FOSC0 = 11b, and frequency range is form 4MHz up to 20MHz. A clock output on P2.0 (XTAL2) may be enabled when External Clock Input is used.

The W79E8213 series supports a clock output function when either the internal RC oscillator or the external clock input options is selected. This allows external devices to synchronize to the W79E8213 serial. When enabled, via the ENCLK bit in the P2M1 register, the clock output appears on the XTAL2/CLKOUT pin whenever the internal RC oscillator is running, including in Idle Mode. The frequency of the clock output is 1/4 of the CPU clock rate. If the clock output is not needed in Idle Mode, it may be turned off prior to entering Idle mode, saving additional power. The clock output may also be enabled when the external clock input option is selected.

For supporting active low buzzer, this buzzer output is implemented with an off-state of high. The following pseudo code shows the operating procedure when working with active high and low buzzer;

(Assume PRHI=1):

1) During power on, P1.0/BUZ will be high;

```
<For active high buzzer>
Clear SFR P1.0          ; user has to take care to output this pin low
                        ; at the top of s/w code to avoid initial beep sound.
<For active low buzzer>
No action needed.
```

2) To turn-on buzzer;

```
<For active high buzzer>
Set BUZE bit
Set SFR P1.0 bit        ; to push out the buzout.
<For active low buzzer>
Set BUZE bit
```

3) To turn-off buzzer;

```
<For active high buzzer>
Clear SFR P1.0          ; user has to take care to output this pin low.
Clear BUZE bit
<For active low buzzer>
Set BUZE bit
```

21. POWER MONITORING FUNCTION

Power-On Detect and Brownout are two additional power monitoring functions implemented in W79E8213 series to prevent incorrect operation during power up and power drop or loss.

21.1 Power On Detect

The Power–On Detect function is a designed to detect power up after power voltage reaches to a level where Brownout Detect can work. After power on detect, the POR (PCON.4) will be set to “1” to indicate an initial power up condition. The POR flag will be cleared by software.

21.2 Brownout Detect

The Brownout Detect function is detect power voltage is drops to brownout voltage level, and allows preventing some process work or indicate power warming. The W79E8213 series have two brownout voltage levels to select by BOV (CONFIG0.4). If BOV =0 that brownout voltage level is 3.8V, If BOV = 1 that brownout voltage level is 2.5V. When the Brownout voltage is drop to select level, the brownout detector will detect and keeps this active until VDD is returns to above brownout Detect voltage. The Brownout Detect block is as follow.

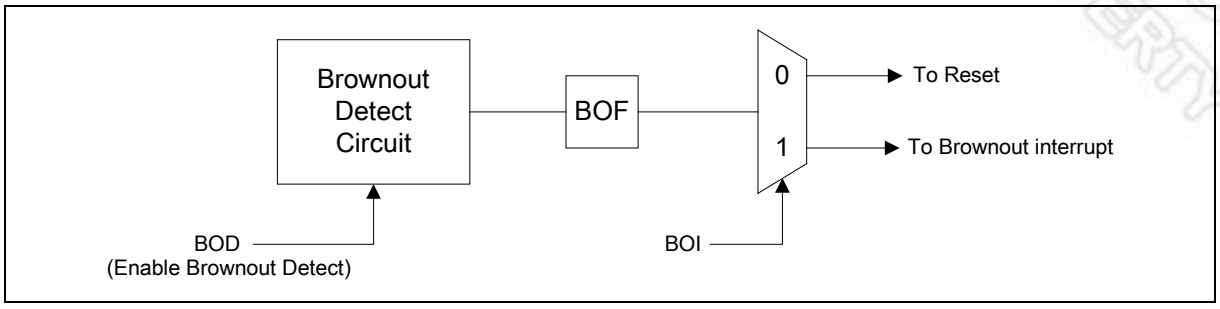


Figure 21-1: Brownout Detect Block

When Brownout Detect is enabled by BOD (AUXR1.6), the BOF (PCON.5) flag will be set and brownout reset will occur. If BOI (AUXR1.5) is set to “1”, the brownout detect will cause interrupt via the EA (IE.7) and EBO (IE.5) bits is set. BOF is cleared by software.

In order to guarantee a correct detection of Brownout, The VDD fail time must be slower than 50mV/us, and rise time is slower than 2mV/us to ensure a proper reset.

22. PULSE-WIDTH-MODULATED (PWM) OUTPUTS

The W79E8213 series have 4 Pulse Width Modulated (PWM) channels, and the PWM outputs are PWM0(P0.1), PWM1(P1.6), PWM2(P1.7), PWM3(P0.0). The initial PWM outputs level correspondingly depend on the PRHI level set prior to the chip reset. When PRHI set to high, PWM output will initialize to high after chip reset; if PRHI set to low, PWM output will be initialize to low after chip reset.

The W79E8213 series support 10-bits down counter with cpu clock as its input. The PWM counter clock, has the frequency as $F_{CPWM} = F_{OSC}$/Prescaler. The two pre-scaler selectable bits FP[1:0] are located at PWMCON3[3:2].

When the counter reaches underflow it will automatic reloaded from counter register. The PWM frequency is given by: $f_{PWM} = F_{CPWM} / (PWMP+1)$, where PWMP is 10-bits register of PWMPH.1, PWMPH.0 and PWMPL.7~PWMPL.0.

The counter register will be loaded with the PWMP register value when PWMRUN, load and PWMF are equal to 1; the load bit will be automatically cleared to zero on the next clock cycle, and at the same time the counter register value will be loaded to the 10 bits down counter. PWMF flag is set when 10-bits down counter underflow, the PWMF flag can only be cleared by software.

The pulse width of each PWM output is determined by the Compare registers of PWM0L through PWM3L and PWM0H through PWM3H. When PWM compare register is greater than 10-bits counter register, the PWM output is low. Load bit has to be set to 1 for alteration of PWMn width. After the new values are written to the PWMn registers, and if load bit is set to 1, the new PWMn values will be loaded to the PWMn registers upon the next underflow. The PWM output high pulses width is given by:

t_{HI} = (PWMP – PWMn+1).

The following equations show the formula for period and duty:

Period = (pwmp +1) * ioclock period * 1/prescaler

Duty = duty * ioclock period

Note:

1. *If compare register is set to 000H, the PWMn output will stay at high, and if compare register is set to 3FFH, the PWMn output will stuck at low until there is a change in the compare register.* [n = 0-3].
2. During ICP mode, PWM pins will be tri-stated. PWM operation will be stop. When exit from ICP mode, the PWM pins will follow the last SFR port values.

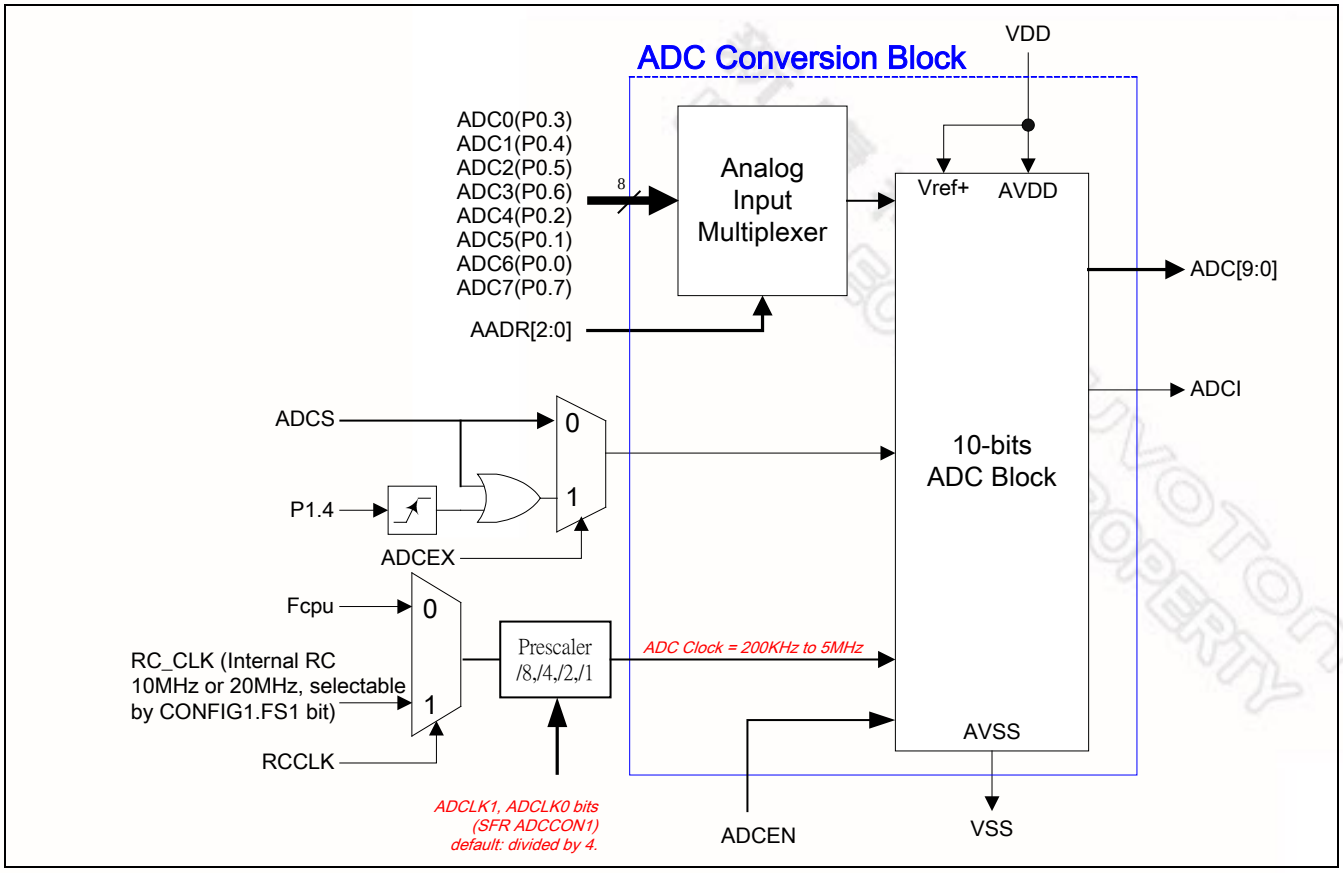


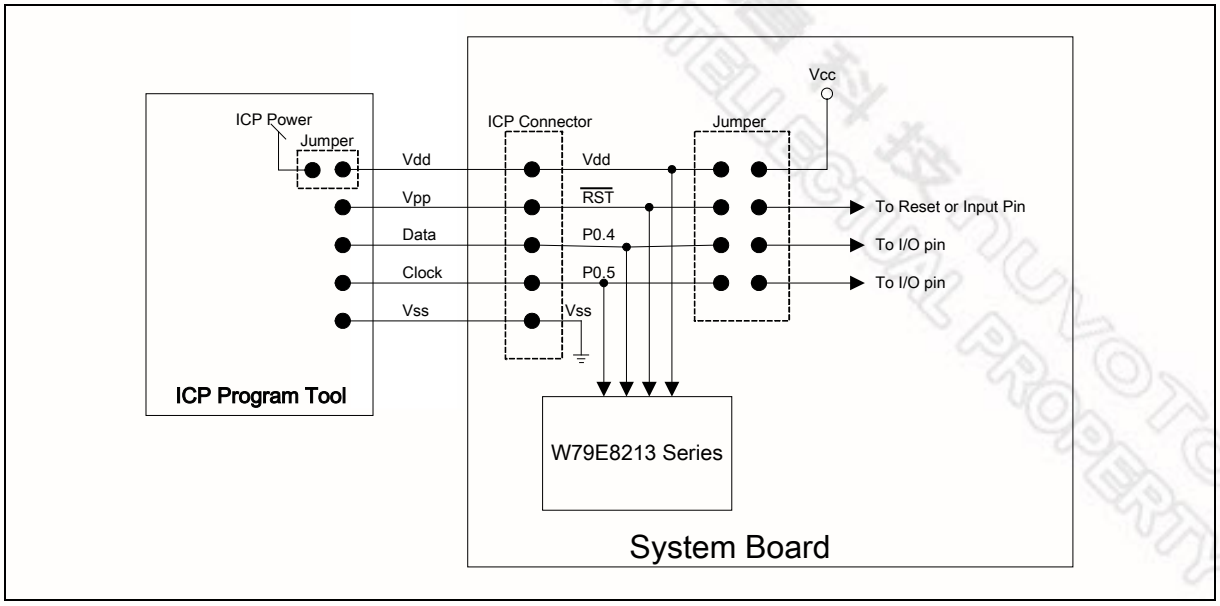
Figure 23-2: ADC block diagram

Note:

As Port 0 is multi-function port, when configuring Port0 for ADC application, user should configure Input Only (High Impedance) and Disable Digital Input on port 0. This is done using P1Mx and PADIDS SFRs.

24. ICP (IN-CIRCUIT PROGRAM) FLASH PROGRAM

The contexts of flash in W79E8213 series are empty by default. At the first use, you must program the flash EPROM by external Writer device or by ICP (In-Circuit Program) tool.



Note:

1. When using ICP to upgrade code, the P1.5, P0.4 and P0.5 must be taken within design system board.
2. After program finished by ICP, to suggest system power must power off and remove ICP connector then power on.
3. It is recommended that user performs erase function and programming configure bits continuously without any interruption.
4. During ICP mode, all PWM pins will be tri-stated.

26. ELECTRICAL CHARACTERISTICS

26.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNIT
DC Power Supply	VDD–VSS	-0.3	+7.0	V
Input Voltage	VIN	VSS-0.3	VDD+0.3	V
Operating Temperature	TA	-40	+85	°C
Storage Temperature	Tst	-55	+150	°C
P1 Sink current	ISK	-	90	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

26.2 DC ELECTRICAL CHARACTERISTICS

(TA = -40~85°C, unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating Voltage	V_{DD1}	2.4	-	5.5	V	V_{DD}=4.5V ~ 5.5V @ 20MHz V_{DD}=2.7V ~ 5.5V @ 12MHz V_{DD}=2.4V ~ 5.5V @ 4MHz
	V_{DD2}	3.0	-	5.5		NVM program and erase operation.
Operating Current (20MHz)	I_{DD1}	-	8.30	12	mA	No load, /RST = VSS, V_{DD}= 5.0V @ 20MHz
	I_{DD2}	-	4.20	6		No load, /RST = VSS, V_{DD}= 3.0V @ 20MHz
	I_{DD3}	-	14.50	20		No load, /RST = V_{DD}, V_{DD}= 5.0V @ 20MHz, RUN NOP
	I_{DD4}	-	5.20	7		No load, /RST = V_{DD}, V_{DD}= 3.0V @ 20MHz, RUN NOP
Operating Current (4MHz)	I_{DD5}	-	3.60	5	mA	No load, /RST = VSS, V_{DD}= 5.0V @ 4MHz
	I_{DD6}	-	1.86	3		No load, /RST = VSS, V_{DD}= 3.0V @ 4MHz
	I_{DD7}	-	8.60	12		No load, /RST = V_{DD}, V_{DD}= 5.0V @ 4MHz, RUN NOP
	I_{DD8}	-	2.20	3.5		No load, /RST = V_{DD}, V_{DD}= 3.0V @ 4MHz, RUN NOP
Idle Current	I_{IDLE1}	-	5.70	8	mA	No load, V_{DD} = 5.0V @ 20MHz
	I_{IDLE2}	-	2.48	3.5		No load, V_{DD} = 3.0V @ 20MHz

DC ELECTRICAL CHARACTERISTICS, continued

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Brownout voltage with BOV=1	$V_{BO2.5}$	2.4	-	2.7	V	TA = -0 to 70°C
Brownout voltage with BOV=0	$V_{BO3.8}$	3.5	-	4	V	TA = -0 to 70°C
ADC current consumption	I_{ADC}	-	0.4	0.8	mA	V_{DD} = 5.0V, ADCCLK = 4MHz
		-	0.25	0.5		V_{DD} = 3.0V, ADCCLK = 4MHz
Brownout voltage detect current	I_{BOD}	-	1.2	1.8	mA	V_{DD} = 5.0V
		-	0.8	1.2		V_{DD} = 3.0V

*1. /RST pin is a Schmitt trigger input.

*2. XTAL1 is a CMOS input.

*3. Pins of P0, P1 and P2 can source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when Vin approximates to 2V.

*4. Only one of the 8 pins sinks high current at a time.

26.3 The ADC Converter DC ELECTRICAL CHARACTERISTICS

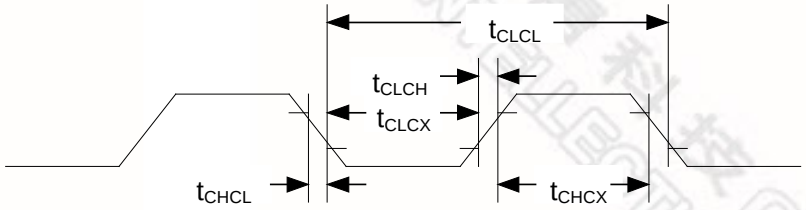
(V_{DD}–V_{SS} = 3.0~5V, TA = -40~85°C, Fosc = 4MHz, unless otherwise specified.)

PARAMETER	SYMBOL	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Analog input	AVin	V_{SS}-0.2		V_{DD}+0.2	V	
ADC clock	ADCCLK	200KHz	-	5MHz	Hz	ADC block circuit input clock
Conversion time	t_C		$52t_{ADC}$ [1]		us	
Differential non-linearity	DNL	-1	-	+1	LSB	
Integral non-linearity	INL	-2	-	+2	LSB	
Offset error	Ofe	-1	-	+1	LSB	
Gain error	Ge	-1	-	+1	%	
Absolute voltage error	Ae	-3	-	+3	LSB	

Notes:

1. tADC: The period time of ADC input clock.

26.5 AC ELECTRICAL CHARACTERISTICS



Note: Duty cycle is 50%.

26.6 EXTERNAL CLOCK CHARACTERISTICS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Clock High Time	t_{CHCX}	12.5	-	-	nS	
Clock Low Time	t_{CLCX}	12.5	-	-	nS	
Clock Rise Time	t_{CLCH}	-	-	10	nS	
Clock Fall Time	t_{CHCL}	-	-	10	nS	

26.7 AC SPECIFICATION

PARAMETER	SYMBOL	VARIABLE CLOCK MIN.	VARIABLE CLOCK MAX.	UNITS
Oscillator Frequency	$1/t_{CLCL}$	0	20	MHz

26.8 TYPICAL APPLICATION CIRCUITS

CRYSTAL	C1	C2	R
4MHz ~ 20 MHz	without	without	without

The above table shows the reference values for crystal applications.