Nuvoton Technology Corporation - W79E8213RAKG Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	18
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP Module
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w79e8213rakg

2. FEATURES

- Fully static design 8-bit 4T-8051 CMOS microcontroller:
  - VDD = 4.5V to 5.5V @20MHz
  - VDD = 2.7V to 5.5V @12MHz
  - VDD = 2.4V to 5.5V @4MHz
- Instruction-set compatible with MSC-51.
- Flexible CPU clock source configurable by config bit and software:
  - High speed external oscillator: upto 20MHz Crystal and resonator (enabled by config bit).
  - Internal RC oscillator: 20/10MHz selectable by config bit, only W79E8213R supports ±2% accuracy internal RC oscillator at fixed voltage and temperature condition.
- 4K bytes of AP Flash EPROM, with ICP and external writer programmable mode.
- 128 bytes of on-chip RAM.
- W79E8213 series supports 128 bytes NVM Data Flash EPROM for customer data storage used and 10K writer cycles.
  - 8 pages. Page size is 16 bytes.
- Two 16-bit timer/counters.
- Ten interrupts source with four levels of priority.
- Three-edge detect interrupt inputs.
- Programmable Watchdog Timer.
- Four-channel 10-bit PWM (Pulse Width Modulator).
- Internal square wave generator for buzzer.
- Up to 18 I/O pins.
- The 4 outputs mode and TTL/Schmitt trigger selectable Port.
- LED drive capability on all port pins. Sink 20mA; Drive: -15~-20mA @push-pull mode.
- Eight high sink capability (40mA) port pins.
- Eight-channel multiplexed with 10-bits A/D convert.
- Low Voltage Detect interrupt and reset.
- Development Tools:
  - ICP(In Circuit Programming) writer
- Packages:

  - Lead Free (RoHS) DIP 20: W79E8213AKG
  - Lead Free (RoHS) SOP 20: W79E8213ASG
  - Lead Free (RoHS) DIP 20: W79E8213RAKG
  - Lead Free (RoHS) SOP 20: W79E8213RASG

7. MEMORY ORGANIZATION

The W79E8213 series separate the memory into two separate sections, the Program Memory and the Data Memory. The Program Memory is used to store the instruction op-codes, while the Data Memory is used to store data or for memory mapped devices.

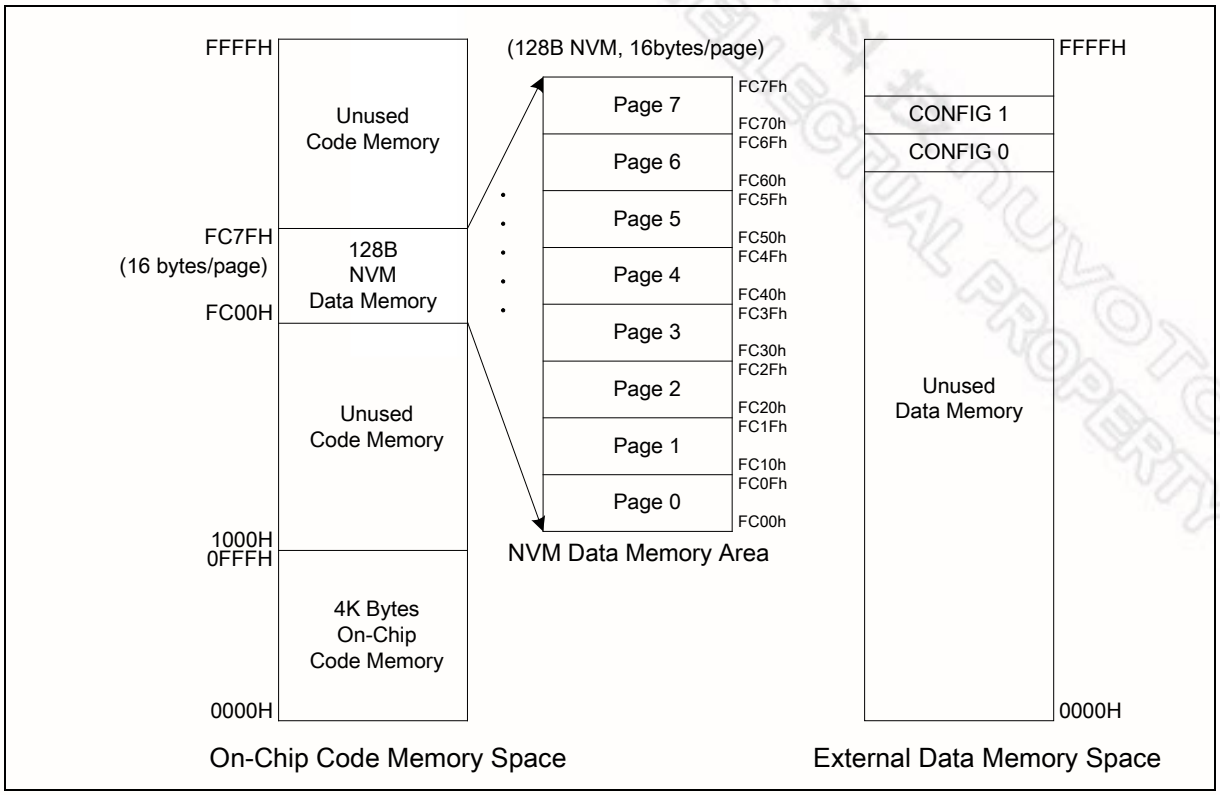


Figure 7-1: W79E8213 series memory map

7.1 Program Memory (on-chip Flash)

The Program Memory on the W79E8213 series can be up to 4K bytes long. All instructions are fetched for execution from this memory area. The MOVC instruction can also access this memory region.

7.2 Data Flash Memory

The NVM Data Memory of Flash EPROM on the W79E8213 series is 128 bytes long, with page size of 16 bytes, respectively. The W79E8213 series' NVM size is controllable through CONFIG1 register. The W79E8213 series read the content of data memory by using "MOVC A, @A+DPTR". To write data is by NVMADDRL, NVMDATA and NVMCON SFR's registers.

SYMBOL	DEFINITION	ADDRESS	MSB LSB BIT_ADDRESS, SYMBOL								RESET
BUZCON	Square wave control register	F9H	-	-	BUZDIV.5	BUZDIV.4	BUZDIV.3	BUZDIV.2	BUZDIV.1	BUZDIV.0	xx00 0000B
IP1	Interrupt priority 1	F8H	(FF) PED	(FE) PPWM	(FD) PBK	(FC) PWDI	(FB) -	(FA) -	(F9) -	(F8) -	0000xxxxB
IP1H	Interrupt high priority 1	F7H	PEDH	PPWMH	PBKH	PWDIH	-	-	-	-	0000xxxxB
PADIDS	Port ADC digital input disable	F6H									00000000B
B	B register	F0H	(F7)	(F6)	(F5)	(F4)	(F3)	(F2)	(F1)	(F0)	00000000B
EIE	Interrupt enable 1	E8H	(EF) EED	(EE) EPWMUF	(ED) EPWM	(EC) EWDI	(EB) -	(EA) -	(E9) -	(E8) -	0000xxxxB
ADCCON1	ADC control register 1	E3H	ADCLK.1	ADCLK.0	-	-	-	AADR2	-	-	10xxx0xxB
ADCH	ADC converter result high register	E2H	ADC.9	ADC.8	ADC.7	ADC.6	ADC.5	ADC.4	ADC.3	ADC.2	00000000B
ADCCON	ADC control register	E1H	ADC.1	ADC.0	ADCEX	ADCI	ADCS	RCCLK	AADR1	AADR0	00000000B
ACC	Accumulator	E0H	(E7)	(E6)	(E5)	(E4)	(E3)	(E2)	(E1)	(E0)	00000000B
PWMCON2	PWM control register 2	DFH	BKCH	BKPS	BPEN	BKEN	PWM3B	PWM2B	PWM1B	PWM0B	00000000B
PWM3L	PWM 3 low bits register	DEH	PWM3.7	PWM3.6	PWM3.5	PWM3.4	PWM3.3	PWM3.2	PWM3.1	PWM3.0	00000000B
PWM2L	PWM 2 low bits register	DDH	PWM2.7	PWM2.6	PWM2.5	PWM2.4	PWM2.3	PWM2.2	PWM2.1	PWM2.0	00000000B
PWMCON1	PWM control register 1	DCH	PWMRUN	load	PWMF	CLRPWM	PWM3I	PWM2I	PWM1I	PWM0I	00000000B
PWM1L	PWM 1 low bits register	DBH	PWM1.7	PWM1.6	PWM1.5	PWM1.4	PWM1.3	PWM1.2	PWM1.1	PWM1.0	00000000B
PWM0L	PWM 0 low bits register	DAH	PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0	00000000B
PWMPL	PWM counter low register	D9H	PWMP0.7	PWMP0.6	PWMP0.5	PWMP0.4	PWMP0.3	PWMP0.2	PWMP0.1	PWMP0.0	00000000B
WDCON	Watch-Dog control	D8H	(DF) WDRUN	(DE) -	(DD) WD1	(DC) WD0	(DB) WDIF	(DA) WTRF	(D9) EWRST	(D8) WDCLR	External reset: 0x00 0000B Watchdog reset: 0x00 0100B Power on reset 0x000000B
PWMCON3	PWM control register 3	D7H	-	-	-	-	FP1	FP0	-	BKF	xxxx00x0B
PWM3H	PWM 3 high bits register	D6H	-	-	-	-	-	-	PWM3.9	PWM3.8	xxxxxx00B
PWM2H	PWM 2 high bits register	D5H	-	-	-	-	-	-	PWM2.9	PWM2.8	xxxxxx00B
PWM1H	PWM 1 high bits register	D3H	-	-	-	-	-	-	PWM1.9	PWM1.8	xxxxxx00B
PWM0H	PWM 0 high bits register	D2H	-	-	-	-	-	-	PWM0.9	PWM0.8	xxxxxx00B
PWMPH	PWM counter high register	D1H	-	-	-	-	-	-	PWMP0.9	PWMP0.8	00000000B
PSW	Program status word	D0H	(D7) CY	(D6) AC	(D5) F0	(D4) RS1	(D3) RS0	(D2) OV	(D1) F1	(D0) P	00000000B
NVMDATA	NVM Data	CFH									00000000B
NVMCON	NVM Control	CEH	EER	EWR	-	-	-	-	-	-	00xxxxxxB
TA	Timed Access Protection	C7H	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0	11111111B
NVMADDRL	NVM low byte address	C6H	-	NVMADDR.6	NVMADDR.5	NVMADDR.4	NVMADDR.3	NVMADDR.2	NVMADDR.1	NVMADDR.0	00000000B
IP0	Interrupt priority	B8H	(BF) -	(BE) PADC	(BD) PBO	(BC) -	(BB) PT1	(BA) PX1	(B9) PT0	(B8) PX0	x00x0000B

PORT 0

Bit:	7	6	5	4	3	2	1	0
	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Mnemonic: P0 Address: 80h

P0.7-0: General purpose Input/Output port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. These alternate functions are described below:

BIT	NAME	FUNCTION
7	P0.7	AD7 pin or Timer 1 pin by alternative.
6	P0.6	AD3 pin by alternative.
5	P0.5	AD2 pin by alternative.
4	P0.4	AD1 pin by alternative.
3	P0.3	AD0 pin by alternative.
2	P0.2	AD4 pin or BRAKE pin by alternative.
1	P0.1	AD5 pin or PWM0 pin by alternative.
0	P0.0	AD6 pin or PWM3 pin by alternative.

Note: During power-on-reset, the port pins are tri-stated. After power-on-reset, the value of the port is set by CONFIG0.PRHI bit. The default setting for CONFIG0.PRHI =1 which the alternative function output is turned on upon reset. If CONFIG0.PRHI is set to 0, the user has to write a 1 to port SFR to turn on the alternative function output.

STACK POINTER

Bit:	7	6	5	4	3	2	1	0
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Mnemonic: SP Address: 81h

BIT	NAME	FUNCTION
7-0	SP.[7:0]	The Stack Pointer stores the Scratch-pad RAM address where the stack begins. In other words it always points to the top of the stack.

DATA POINTER LOW

Bit:	7	6	5	4	3	2	1	0
	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0

Mnemonic: DPL Address: 82h

BIT	NAME	FUNCTION
7-0	DPL.[7:0]	This is the low byte of the standard 8052 16-bit data pointer.

1	P2.1	XTAL1 clock input pin.
0	P2.0	XTAL2 or CLKOUT pin by alternative.

Note: During power-on-reset, the port pins are tri-stated. After power-on-reset, the value of the port is set by CONFIG0.PRHI bit. The default setting for CONFIG0.PRHI =1 which the alternative function output is turned on upon reset. If CONFIG0.PRHI is set to 0, the user has to write a 1 to port SFR to turn on the alternative function output.

AUX FUNCTION REGISTER 1

Bit:	7	6	5	4	3	2	1	0
	EDF	BOD	BOI	LPBOV	SRST	ADCEN	BUZE	-

Mnemonic: AUXR1 Address: A2h

BIT	NAME	FUNCTION
7	EDF	Edge detect Interrupt Flag: 1: When any pin of port 1.0-1.2 that is enabled for the Edge Detect Interrupt function trigger (falling/rising edge trigger configurable). Must be cleared by software.
6	BOD	Brown Out Disable: 0: Enable Brownout Detect function. 1: Disable Brownout Detect function and save power.
5	BOI	Brown Out Interrupt: 0: Disable Brownout Detect Interrupt function and it will cause chip reset when BOF is set. 1: This prevents Brownout Detection from causing a chip reset and allows the Brownout Detect function to be used as an interrupt.
4	LPBOV	Low Power Brown Out Detect control: 0: When BOD is enable, the Brown Out detect is always turned on by normal run or Power-down mode. 1: When BOD is enable, the Brown Out detect circuit is turned on by Power-down mode. This control can help save 15/16 of the Brownout circuit power. When uC is in Power-down mode, the BOD will enable internal RC OSC (600KHz+/- 50%)
3	SRST	Software reset: 1: reset the chip as if a hardware reset occurred.
2	ADCEN	0: Disable ADC circuit. 1: Enable ADC circuit.
1	BUZE	Square-wave enable bit: 0: Disable square wave output. 1: The square wave is output to the BUZ (P1.0) pin.
0	-	Reserved.

EDGE DETECT CONTROL REGISTER

Bit:	7	6	5	4	3	2	1	0
	EDFILT.1	EDFILT.0	ED2TRG	ED2EN	ED1TRG	ED1EN	ED0TRG	ED0EN

Mnemonic: EDIC Address: A3h

PWM CONTROL REGISTER 3

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	FP1	FP0	-	BKF

Mnemonic: PWMCON3 Address: D7h

BIT	NAME	FUNCTION
7-4	-	Reserved.
3-2	FP[1:0]	Select PWM frequency pre-scale select bits. The clock source of pre-scaler, Fpwm is in phase with Fosc if PWMRUN=1. FP[1:0] → Fpwm: 00 → Fosc; 01 → Fosc/2; 10 → Fosc/4; 11 → Fosc/16
1	-	Reserved.
0	BKF	The external brake pin flag: 0: The PWM is not brake. 1: The PWM is brake by external brake pin. It is cleared by software.

WATCHDOG CONTROL

Bit:	7	6	5	4	3	2	1	0
	WDRUN	-	WD1	WD0	WDIF	WTRF	EWRST	WDCLR

Mnemonic: WDCON Address: D8h

BIT	NAME	FUNCTION
7	WDRUN	0: The Watchdog is stopped. 1: The Watchdog is running.
6	-	Reserved.
5	WD1	Watchdog Timer Time-out Select bits. These bits determine the time-out period of the watchdog timer. The reset time-out period is 512 clocks longer than the watchdog time-out.
4	WD0	WD1 / WD0 / Interrupt time-out / Reset time-out: 0 / 0 / 2^{17} / 2^{17} + 512 0 / 1 / 2^{20} / 2^{20} + 512 1 / 0 / 2^{23} / 2^{23} + 512 1 / 1 / 2^{26} / 2^{26} + 512
3	WDIF	Watchdog Timer Interrupt Flag 0: If the interrupt is not enabled, then this bit indicates that the time-out period has elapsed. This bit must be cleared by software. 1: If the watchdog interrupt is enabled, hardware will set this bit to indicate that the watchdog interrupt has occurred.
2	WTRF	Watchdog Timer Reset Flag 1: Hardware will set this bit when the watchdog timer causes a reset. Software can read it but must clear it manually. A power-fail reset will also clear the bit. This bit helps software in determining the cause of a reset. If EWRST =

7~0	PWM1.[7:0]	PWM 1 Low Bits Register.

PWM CONTROL REGISTER 1

Bit:	7	6	5	4	3	2	1	0
	PWMRUN	Load	PWMF	CLRPWM	-	-	PWM1I	PWM0I

Mnemonic: PWMCON1 Address: DCh

BIT	NAME	FUNCTION
7	PWMRUN	0: The PWM is not running. 1: The PWM counter is running.
6	Load	0: The registers value of PWMP and PWMn are never loaded to counter and Comparator registers. 1: The PWMP and PWMn registers load value to counter and compare registers at the counter underflow. This bit is auto cleared by hardware at next clock cycle.
5	PWMF	PWM underflow flag: 0: The 10-bit counter down count is not underflow. 1: The 10-bit counter down count is underflow. (PWM interrupt is requested if PWM interrupt is enabled). This bit is Software clear.
4	CLRPWM	1: Clear 10-bit PWM counter to 000H. This bit is auto cleared by hardware.
3	PWM3I	0: PWM3 out is non-inverted. 1: PWM3 output is inverted.
2	PWM2I	0: PWM2 out is non-inverted. 1: PWM2 output is inverted.
1	PWM1I	0: PWM1 out is non-inverted. 1: PWM1 output is inverted.
0	PWM0I	0: PWM0 out is non-inverted. 1: PWM0 output is inverted.

PWM2 LOW BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	PWM2.7	PWM2.6	PWM2.5	PWM2.4	PWM2.3	PWM2.2	PWM2.1	PWM2.0

Mnemonic: PWM2L Address: DDh

BIT	NAME	FUNCTION
7~0	PWM2.[7:0]	PWM 2 Low Bits Register.

Continued

BIT	NAME	FUNCTION
4	PADIDS.4	P0.4 digital input disable bit. 0: Default (With digital/analog input). 1: Disable Digital Input of ADC Input Channel 1.
3	PADIDS.3	P0.3 digital input disable bit. 0: Default (With digital/analog input). 1: Disable Digital Input of ADC Input Channel 0.
2	PADIDS.2	P0.2 digital input disable bit. 0: Default (With digital/analog input). 1: Disable Digital Input of ADC Input Channel 4.
1	PADIDS.1	P0.1 digital input disable bit. 0: Default (With digital/analog input). 1: Disable Digital Input of ADC Input Channel 5.
0	PADIDS.0	P0.0 digital input disable bit. 0: Default (With digital/analog input). 1: Disable Digital Input of ADC Input Channel 6.

Note: Port 0 (ADC input pins) should also be set to Input Only (High Impedance) during when using the port for ADC application. Please see I/O Port Configuration section.

INTERRUPT HIGH PRIORITY 1

Bit:	7	6	5	4	3	2	1	0
	PEDH	PPWMH	PBKH	PWDIH	-	-	-	-

Mnemonic: IP1H Address: F7h

BIT	NAME	FUNCTION
7	PEDH	1: To set interrupt high priority of edge detect is highest priority level.
6	PPWMH	1: To set interrupt priority of PWM underflow is highest priority level.
5	PBKH	1: To set interrupt priority of PWM's external brake is highest priority level.
4	PWDIH	1: To set interrupt high priority of Watchdog is highest priority level.
3-0	-	Reserved.

EXTENDED INTERRUPT PRIORITY

Bit:	7	6	5	4	3	2	1	0
	PED	PPWM	PBK	PWDI	-	-	-	-

Mnemonic: IP1 Address: F8h

INSTRUCTION SET, continued

Op-code	HEX Code	Bytes	W79E8213 series Machine Cycle	W79E8213 series Clock cycles	8032 Clock cycles	W79E8213 series v.s 8032 Speed Ratio
ORL direct, A	42	2	2	8	12	1.5
ORL direct, #data	43	3	3	12	24	2
XRL A, R0	68	1	1	4	12	3
XRL A, R1	69	1	1	4	12	3
XRL A, R2	6A	1	1	4	12	3
XRL A, R3	6B	1	1	4	12	3
XRL A, R4	6C	1	1	4	12	3
XRL A, R5	6D	1	1	4	12	3
XRL A, R6	6E	1	1	4	12	3
XRL A, R7	6F	1	1	4	12	3
XRL A, @R0	66	1	1	4	12	3
XRL A, @R1	67	1	1	4	12	3
XRL A, direct	65	2	2	8	12	1.5
XRL A, #data	64	2	2	8	12	1.5
XRL direct, A	62	2	2	8	12	1.5
XRL direct, #data	63	3	3	12	24	2
CLR A	E4	1	1	4	12	3
CPL A	F4	1	1	4	12	3
RL A	23	1	1	4	12	3
RLC A	33	1	1	4	12	3
RR A	03	1	1	4	12	3
RRC A	13	1	1	4	12	3
SWAP A	C4	1	1	4	12	3
MOV A, R0	E8	1	1	4	12	3
MOV A, R1	E9	1	1	4	12	3
MOV A, R2	EA	1	1	4	12	3
MOV A, R3	EB	1	1	4	12	3
MOV A, R4	EC	1	1	4	12	3
MOV A, R5	ED	1	1	4	12	3
MOV A, R6	EE	1	1	4	12	3
MOV A, R7	EF	1	1	4	12	3
MOV A, @R0	E6	1	1	4	12	3
MOV A, @R1	E7	1	1	4	12	3
MOV A, direct	E5	2	2	8	12	1.5

INSTRUCTION SET, continued

Op-code	HEX Code	Bytes	W79E8213 series Machine Cycle	W79E8213 series Clock cycles	8032 Clock cycles	W79E8213 series v.s 8032 Speed Ratio
MOV direct, R2	8A	2	2	8	12	1.5
MOV direct, R3	8B	2	2	8	12	1.5
MOV direct, R4	8C	2	2	8	12	1.5
MOV direct, R5	8D	2	2	8	12	1.5
MOV direct, R6	8E	2	2	8	12	1.5
MOV direct, R7	8F	2	2	8	12	1.5
MOV direct, @R0	86	2	2	8	12	1.5
MOV direct, @R1	87	2	2	8	12	1.5
MOV direct, direct	85	3	3	12	24	2
MOV direct, #data	75	3	3	12	24	2
MOV DPTR, #data 16	90	3	3	12	24	2
MOVC A, @A+DPTR	93	1	2	8	24	3
MOVC A, @A+PC	83	1	2	8	24	3
MOVX A, @R0	E2	1	2 - 9	8 - 36	24	3 - 0.66
MOVX A, @R1	E3	1	2 - 9	8 - 36	24	3 - 0.66
MOVX A, @DPTR	E0	1	2 - 9	8 - 36	24	3 - 0.66
MOVX @R0, A	F2	1	2 - 9	8 - 36	24	3 - 0.66
MOVX @R1, A	F3	1	2 - 9	8 - 36	24	3 - 0.66
MOVX @DPTR, A	F0	1	2 - 9	8 - 36	24	3 - 0.66
PUSH direct	C0	2	2	8	24	3
POP direct	D0	2	2	8	24	3
XCH A, R0	C8	1	1	4	12	3
XCH A, R1	C9	1	1	4	12	3
XCH A, R2	CA	1	1	4	12	3
XCH A, R3	CB	1	1	4	12	3
XCH A, R4	CC	1	1	4	12	3
XCH A, R5	CD	1	1	4	12	3
XCH A, R6	CE	1	1	4	12	3
XCH A, R7	CF	1	1	4	12	3
XCH A, @R0	C6	1	1	4	12	3
XCH A, @R1	C7	1	1	4	12	3
XCHD A, @R0	D6	1	1	4	12	3
XCHD A, @R1	D7	1	1	4	12	3
XCH A, direct	C5	2	2	8	12	1.5

flag is active in one cycle but not responded to, and is not active when the above conditions are met, the denied interrupt will not be serviced. This means that active interrupts are not remembered; every polling cycle is new.

The processor responds to a valid interrupt by executing an LCALL instruction to the appropriate service routine. This may or may not clear the flag which caused the interrupt. In case of Timer interrupts, the TF0 or TF1 flags are cleared by hardware whenever the processor vectors to the appropriate timer service routine. In case of external interrupt, INT0 and INT1, the flags are cleared only if they are edge triggered. In case of Serial interrupts, the flags are not cleared by hardware. The Watchdog timer interrupt flag WDIF has to be cleared by software. The hardware LCALL behaves exactly like the software LCALL instruction. This instruction saves the Program Counter contents onto the Stack, but does not save the Program Status Word PSW. The PC is reloaded with the vector address of that interrupt which caused the LCALL. These address of vector for the different sources are as following:

VECTOR LOCATIONS FOR INTERRUPT SOURCES

SOURCE	VECTOR ADDRESS	SOURCE	VECTOR ADDRESS
External Interrupt 0	0003h	Timer 0 Overflow	000Bh
External Interrupt 1	0013h	Timer 1 Overflow	001Bh
-	0023h	Brownout Interrupt	002Bh
-	0033h	Edge Detect Interrupt	003Bh
-	0043h	-	004Bh
Watchdog Timer	0053h	ADC Interrupt	005Bh
-	0063h	PWM Brake Interrupt	0073h
PWM Underflow Interrupt	006Bh	-	007Bh

Table 12-1: Vector locations for interrupt sources

Execution continues from the vectored address till an RETI instruction is executed. On execution of the RETI instruction the processor pops the Stack and loads the PC with the contents at the top of the stack. The user must take care that the status of the stack is restored to what it was after the hardware LCALL, if the execution is return to the interrupted program. The processor does not notice anything if the stack contents are modified and will proceed with execution from the address put back into PC. Note that a RET instruction would perform exactly the same process as a RETI instruction, but it would not inform the Interrupt Controller that the interrupt service routine is completed, and would leave the controller still thinking that the service routine is underway.

They are IE0, IE1, BOF, EDF, WDT, TF0, TF1, BKF and ADC. Two interrupt inputs are identical to those present on the standard 80C51 microcontroller as show in below figures.

If an external interrupt is enabled when the W79E8213 series are put into Power-down or Idle mode, the interrupt will cause the processor to wake up and resume operation.

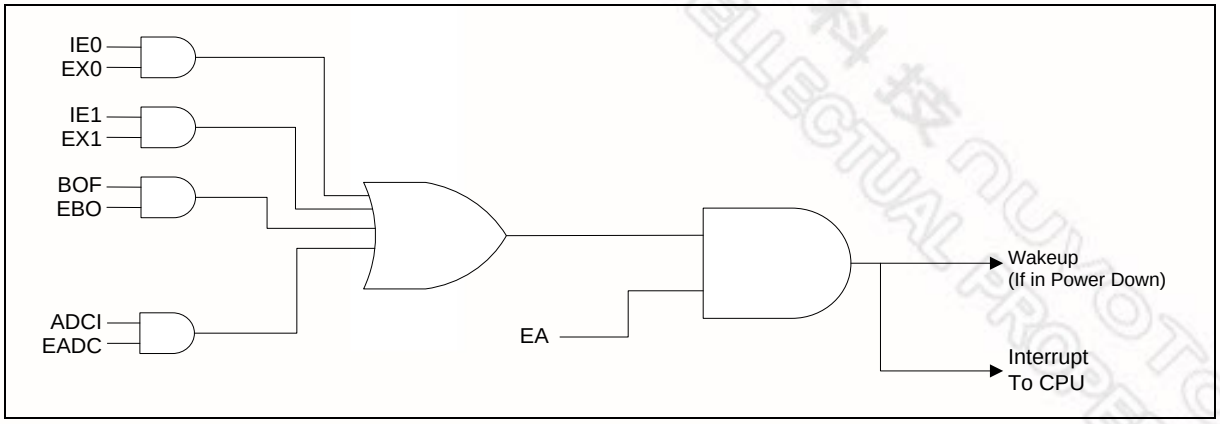


Figure 12-1: Interrupt sources that can wake up from power-down mode

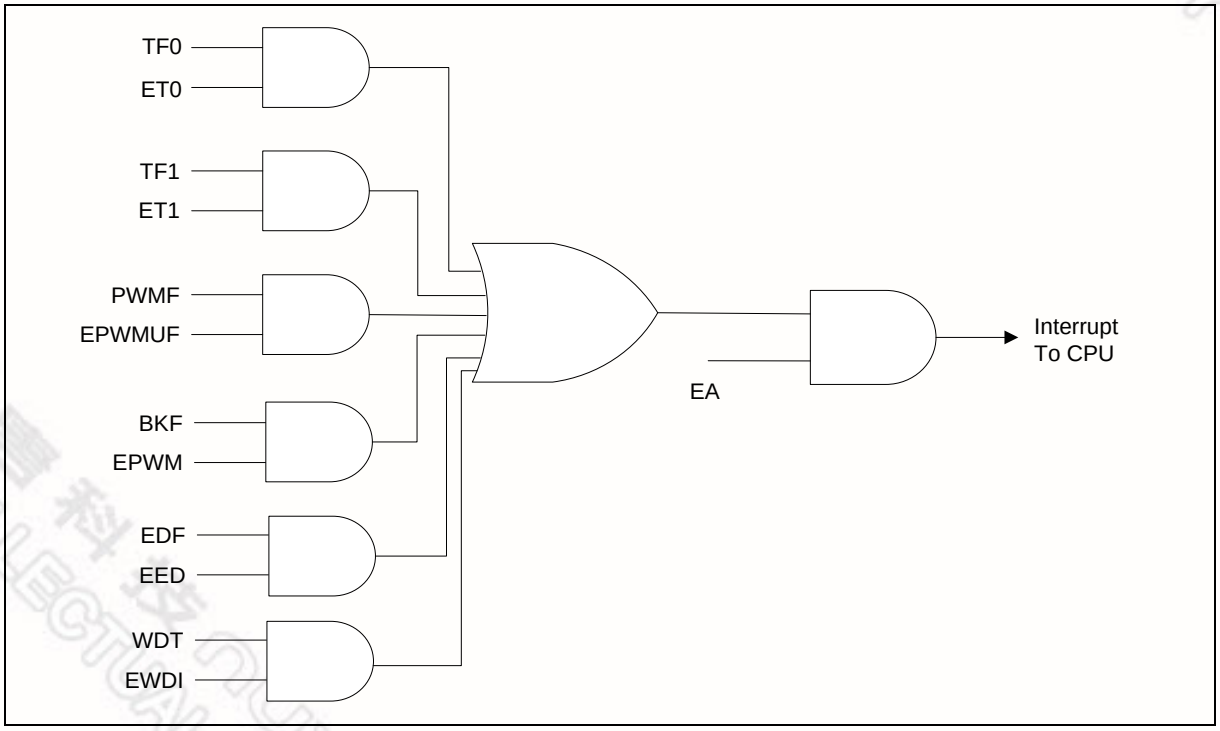


Figure 12-2: Interrupt Sources that cannot wake up from power-down mode

14. NVM MEMORY

The W79E8213 series have NVM data memory of 128 bytes for customer's data store used. The NVM data memory has 8 pages area and each page of 16 bytes.

The NVM memory can be read/write by customer program to access. Read NVM data is by MOVC A,@A+DPTR instruction, and write data is by SFR of NVMADDRL, NVMDATA and NVMCON. Before write data to NVM memory, the page must be erased by providing page address on NVMADDRL, which address of On-Chip Code Memory space will decode, then set EER of NVMCON.7. This will automatically hold fetch program code and PC Counter, and execute page erase. After finished, this bit will be cleared by hardware. The erase time is ~ 5ms.

For writing data to NVM memory, user must set address and data to NVMADDRL and NVMDATA, then set EWR of NVMCON.6 to initiate nvm data write. The uC will hold program code and PC Counter, and then write data to mapping address. Upon write completion, the EWR bit will be cleared by hardware, the uC will continue execute next instruction. The program time is ~50us.

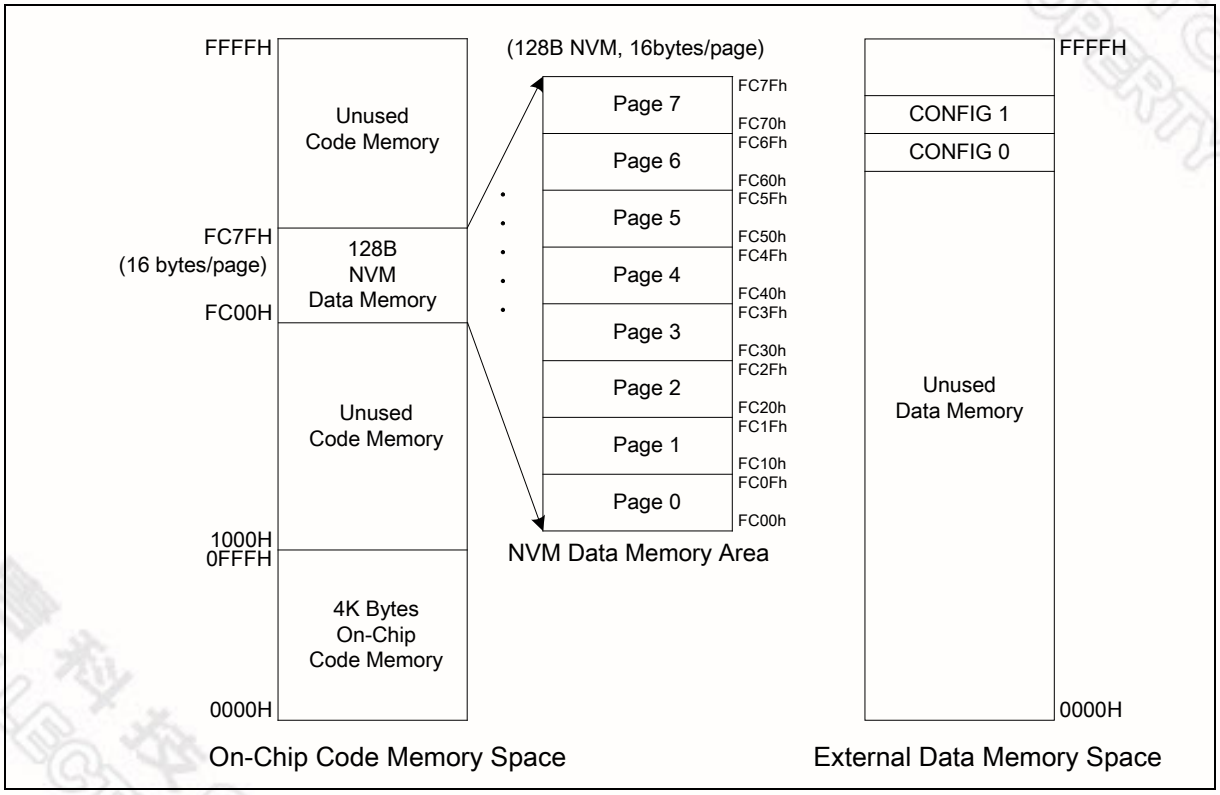


Figure 14-1: W79E8213 Memory Map

Example 5: Invalid Access

```
MOV     TA, #0AAh       ; 3 M/C
NOP                     ; 1 M/C
MOV     TA, #055h       ; 3 M/C
SETB    EWT             ; 2 M/C
```

In the first three examples, the writing to the protected bits is done before the 3 machine cycles window closes. In Example 4, however, the writing to the protected bit occurs after the window has closed, and so there is effectively no change in the status of the protected bit. In Example 5, the second write to TA occurs 4 machine cycles after the first write, therefore the timed access window is not opened at all, and the write to the protected bit fails.

19. OSCILLATOR

The W79E8213 series provides three oscillator input option. These are configured at CONFIG register (CONFIG0) that include Internal RC Oscillator Option, External Clock Input Option and Crystal Oscillator Input Option. The Crystal Oscillator Input frequency may be supported from 4MHz to 20MHz, and without capacitor or resister.

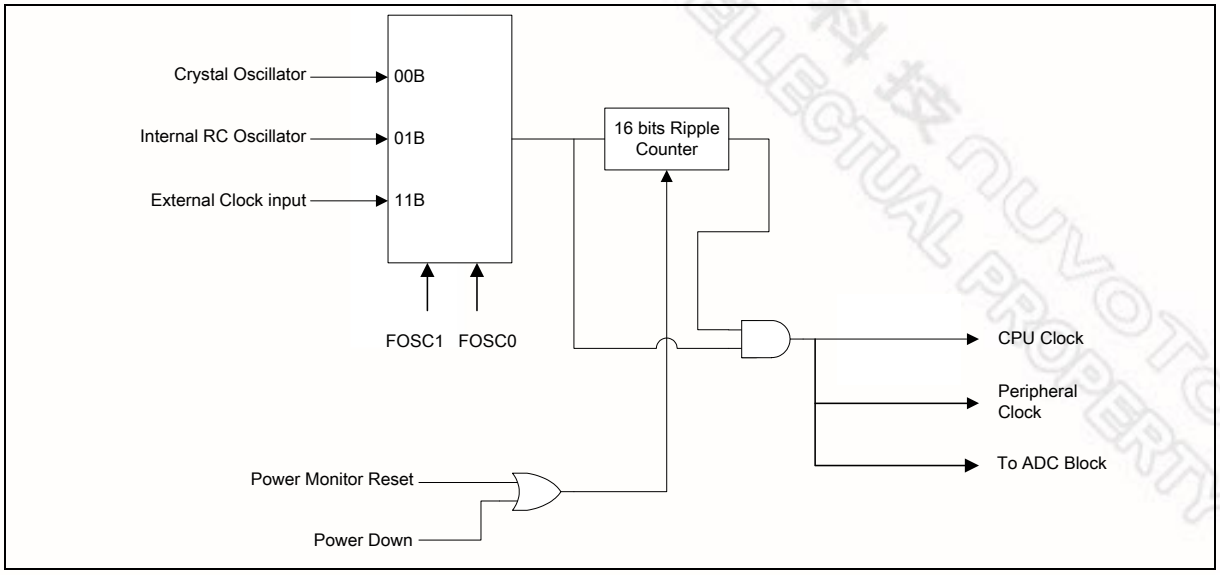


Figure 19-1: Oscillator

19.1 Internal RC Oscillator Option

The internal RC Oscillator is configurable to 10MHz/20MHz (through CONFIG1.FS1 bit) frequency to support clock source. When FOSC1, FOSC0 = 01b, the internal RC oscillator is enabled. A clock output on P2.0 (XTAL2) may be enabled when internal RC oscillator is used.

19.2 External Clock Input Option

The clock source pin (XTAL1) is from External Clock Input by FOSC1, FOSC0 = 11b, and frequency range is form 4MHz up to 20MHz. A clock output on P2.0 (XTAL2) may be enabled when External Clock Input is used.

The W79E8213 series supports a clock output function when either the internal RC oscillator or the external clock input options is selected. This allows external devices to synchronize to the W79E8213 serial. When enabled, via the ENCLK bit in the P2M1 register, the clock output appears on the XTAL2/CLKOUT pin whenever the internal RC oscillator is running, including in Idle Mode. The frequency of the clock output is 1/4 of the CPU clock rate. If the clock output is not needed in Idle Mode, it may be turned off prior to entering Idle mode, saving additional power. The clock output may also be enabled when the external clock input option is selected.

For supporting active low buzzer, this buzzer output is implemented with an off-state of high. The following pseudo code shows the operating procedure when working with active high and low buzzer;

(Assume PRHI=1):

1) During power on, P1.0/BUZ will be high;

```
<For active high buzzer>
Clear SFR P1.0          ; user has to take care to output this pin low
                        ; at the top of s/w code to avoid initial beep sound.
<For active low buzzer>
No action needed.
```

2) To turn-on buzzer;

```
<For active high buzzer>
Set BUZE bit
Set SFR P1.0 bit        ; to push out the buzout.
<For active low buzzer>
Set BUZE bit
```

3) To turn-off buzzer;

```
<For active high buzzer>
Clear SFR P1.0          ; user has to take care to output this pin low.
Clear BUZE bit
<For active low buzzer>
Set BUZE bit
```

25. CONFIG BITS

The W79E8213 series has two CONFIG bits that must be defined at power up and can not be set the program after start of execution. Those features are configured through the use of two flash EPROM bytes, and the flash EPROM can be programmed and verified repeatedly. Until the code inside the Flash EPROM is confirmed OK, the code can be protected. The protection of flash EPROM (CONFIG1) and those operations on it are described below. The data of these bytes may be read by the MOVX instruction at the addresses.

25.1 CONFIG0

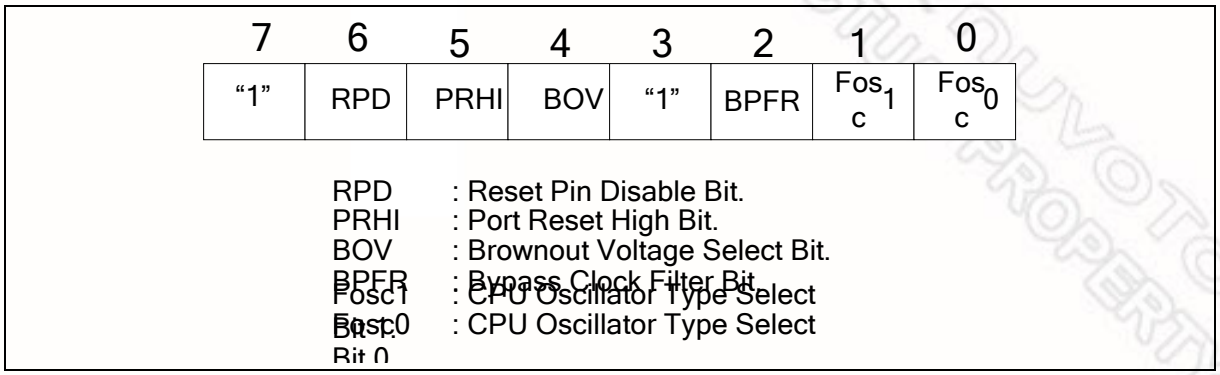
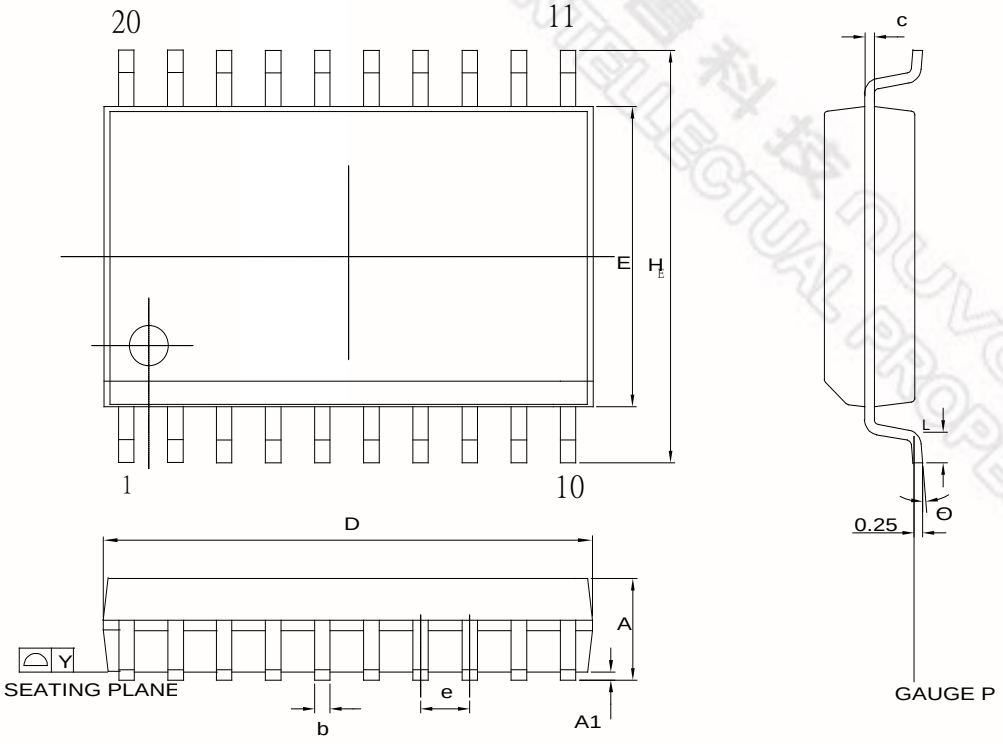


Figure 25-1: Config0 register bits

BIT	NAME	FUNCTION
7	-	***Must be "1"***
6	RPD	Reset Pin Disable bit: 0: Enable Reset function of Pin 1.5. 1: Disable Reset function of Pin 1.5, and it to be used as an input port pin.
5	PRHI	Port Reset High or Low bit: 0: Port reset to low state. 1: Port reset to high state.
4	BOV	Brownout Voltage Select bit: 0: Brownout detect voltage is 3.8V. 1: Brownout detect voltage is 2.5V.
3	-	***Must be "1"***
2	BPFR	Bypass Clock Filter. 0: Disable Clock Filter. 1: Enable Clock Filter.
1	Fosc1	CPU Oscillator Type Select bit 1.
0	Fosc0	CPU Oscillator Type Select bit 0.

27. PACKAGE DIMENSIONS

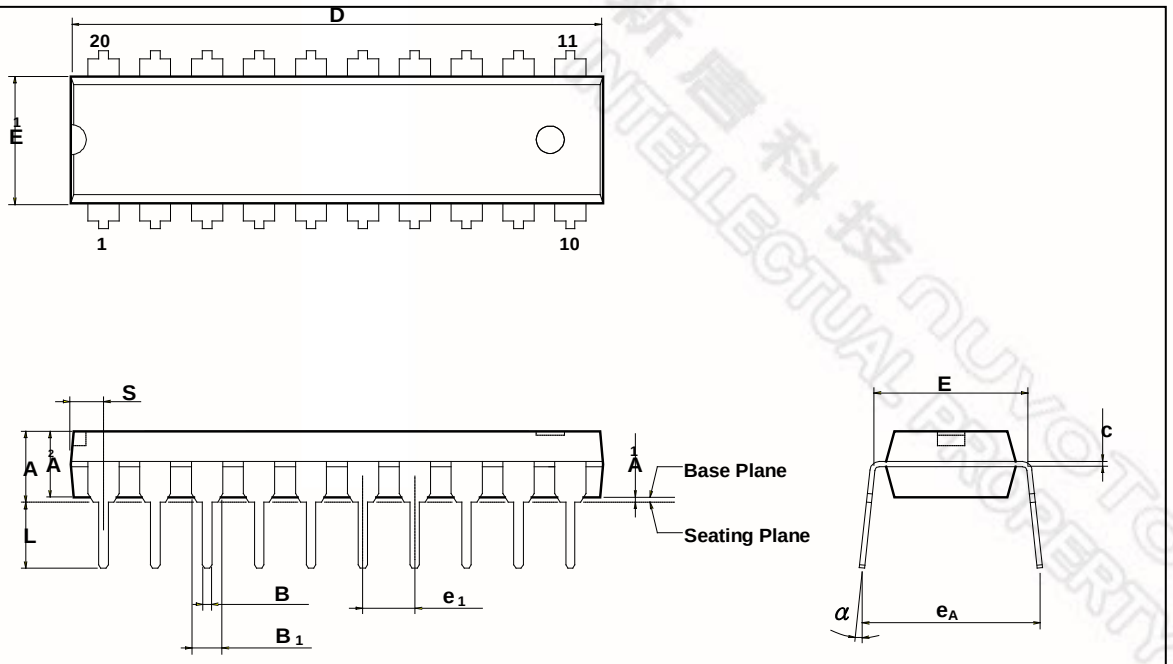
27.1 20-pin SOP-300mil



Control demensions are in milmeters .

SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	2.35	2.65	0.093	0.104
A1	0.10	0.30	0.004	0.012
b	0.33	0.51	0.013	0.020
c	0.23	0.32	0.009	0.013
E	7.40	7.60	0.291	0.299
D	12.60	13.00	0.496	0.512
e	1.27 BSC		0.050 BSC	
H_E	10.00	10.65	0.394	0.419
Y	—	0.10	—	0.004
L	0.40	1.27	0.016	0.050
θ	0	8	0	8

27.2 20-pin PDIP-300mil



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.175	—	—	4.45
A_1	0.010	—	—	0.25	—	—
A_2	0.125	0.130	0.135	3.18	3.30	3.43
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.058	0.060	0.064	1.47	1.52	1.63
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	1.026	1.040	—	20.06	26.42
E	0.290	0.300	0.310	7.37	7.62	7.87
E_1	0.245	0.250	0.255	6.22	6.35	6.48
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
α	0	—	15	0	—	15
e_A	0.335	0.355	0.375	8.51	9.02	9.53
S	—	—	0.075	—	—	1.91

28. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	May 20, 2008	-	Initial Issued
A2	July 11, 2008	5 92	Add VDD = 2.7V to 5.5V @12MHz CPU operation condition Revise ADC current consumption specification
A3	August 5, 2008	91	Revise Power down current to typical 1uA, max.10uA
A4	September 1, 2008	6 93	Revise Lead Free (RoHS) Parts information list Revise Internal RC Oscillator Accuracy table
A5	November 12, 2008	30	Remove duplicate description about SFR WDCON register
A6	November 21, 2009	87 91	Remove the “prelimanry” Add defaule value for the reserved bit of CONFIG0 Add defaule value for the reserved bit of CONFIG1
A7	November 12, 2012	92	Revise chapter 26.4 “Internal RC ± 2% with VDD = 5.0V, TA = 25C”.