Nuvoton Technology Corporation - W79E8213RARG Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	18
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w79e8213rarg

5. PIN DESCRIPTIONS

SYMBOL	ALTERNATE FUNCTION 1	ALTERNATE FUNCTION 2	ALTERNATE FUNCTION 3	ALTERNATE FUNCTION 4 (ICP MODE)	TYPE	DESCRIPTION
VDD					P	POWER SUPPLY: Supply voltage for operation.
VSS					P	GROUND: Ground potential.
P0.0	AD6		PWM3		I/O	Port0: Support 4 output modes and TTL/Schmitt trigger. Multifunction pins for T1, PWM0, PWM3, BRAKE, AD0-7, Data and Clock (for ICP).
P0.1	AD5		PWM0		I/O	
P0.2	AD4		BRAKE		I/O	
P0.3	AD0				I/O	
P0.4	AD1			Data	I/O	
P0.5	AD2			Clock	I/O	
P0.6	AD3				I/O	
P0.7	AD7		T1		I/O	
P1.0	BUZ	ED0			I/O	Port1: Support 4 output modes and TTL/Schmitt trigger (except for P1.5 input only). Multifunction pins for /RST, T0, /INT0-1, BUZ, PWM1-2, ED0-2, STADC, and HV (for ICP). P1.0-P1.7 have 40mA high sink capability.
P1.1		ED1			I/O	
P1.2		ED2	T0		I/O	
P1.3		/INT0			I/O	
P1.4	STADC	/INT1			I/O	
P1.5	$\overline{\text{RST}}$			HV	I	
P1.6	PWM1				I/O	
P1.7	PWM2				I/O	
P2.0	XTAL2/CLKOUT				I/O	CRYSTAL2: This is the crystal oscillator output. It is the inversion of XTAL1. Also a configurable i/o pin. When operating as I/O, it supports 4 output modes and TTL/Schmitt trigger.
P2.1	XTAL1				I/O	CRYSTAL1: This is the crystal oscillator input. This pin may be driven by an external clock or configurable I/O pin. When operating as I/O, it supports 4 output modes and TTL/Schmitt trigger.

* **TYPE:** P: power, I: input, O: output, I/O: bi-directional, H: pull-high, L: pull-low, D: open-drain**.**

Table 5-1: Pin Description

Note:

On power-on-reset, all port pins will be tri-stated.

After power-on-reset, all port pins state will follow CONFIG0.PRHI bit definition.

6. FUNCTIONAL DESCRIPTION

The W79E8213 series architecture consist of a 4T 8051 core controller surrounded by various registers, 4K bytes Flash EPROM, 128 bytes of RAM, up to 18 general purpose I/O ports, two timer/counters, 3 edge detector inputs, 4-channel PWM with 10-bits counter, 8-channel multiplexed with 10-bit ADC analog input, Flash EPROM program by Writer and ICP. W79E8213 series supported 128 bytes NVM Data Flash EPROM.

6.1 On-Chip Flash EPROM

The W79E8213 series include one 4K bytes of main Flash EPROM for application program. A Writer or ICP programming board is required to program the Flash EPROM or NVM Data Flash EPROM.

This ICP (In-Circuit Programming) feature makes the job easy and efficient when the application's firmware needs to be updated frequently. In some applications, the in-circuit programming feature makes it possible for the end-user to easily update the system firmware without opening the chassis.

6.2 I/O Ports

The W79E8213 series have up to 18 I/O pins using internal RC oscillator & /RST is input only by reset options. All ports can be used as four outputs mode when it may set by PxM1.y and PxM2.y SFR's registers, it has strong pull-ups and pull-downs, and does not need any external pull-ups. Otherwise it can be used as general I/O port as open drain circuit. All ports can be used bi-directional and these are as I/O ports. These ports are not true I/O, but rather are pseudo-I/O ports. This is because these ports have strong pull-downs and weak pull-ups.

6.3 Timers

The W79E8213 series have two 16-bit timers that are functionally and similar to the timers of the 8052 family. When used as timers, the user has a choice of 12 or 4 clocks per count that emulates the timing of the original 8052.

6.4 Interrupts

The Interrupt structure in the W79E8213 series is slightly different from that of the standard 8052. Due to the presence of additional features and peripherals, the number of interrupt sources and vectors has been increased.

6.5 Data Pointer

The data pointer of W79E8213 series is same as standard 8052 which have 16-bit Data Pointer (DPTR).

6.6 Architecture

The W79E8213 series are based on the standard 8052 device. It is built around an 8-bit ALU that uses internal registers for temporary storage and control of the peripheral devices. It can execute the standard 8052 instruction set.

6.6.1 ALU

The ALU is the heart of the W79E8213 series. It is responsible for the arithmetic and logical functions. It is also used in decision making, in case of jump instructions, and is also used in calculating jump addresses. The user cannot directly use the ALU, but the Instruction Decoder reads the op-code,

Continued

SYMBOL	DEFINITION	ADDRESS	MSB BIT_ADDRESS, SYMBOL LSB								RESET
IP0H	Interrupt high priority	B7H	-	PADCH	PBOH	-	PT1H	PX1H	PT0H	PX0H	x00x0000B
P2M2	Port 2 output mode 2	B6H	-	-	-	-	-	-	P2M2.1	P2M2.0	xxxxxx 00B
P2M1	Port 2 output mode 1	B5H	P2S	P1S	P0S	ENCLK	T1OE	T0OE	P2M2.1	P2M2.0	00000000B
P1M2	Port 1 output mode 2	B4H	P1M2.7	P1M2.6	-	P1M2.4	P1M2.3	P1M2.2	P1M2.1	P1M2.0	00x00000B
P1M1	Port 1 output mode 1	B3H	P1M1.7	P1M1.6	-	P1M1.4	P1M1.3	P1M1.2	P1M1.1	P1M1.0	00x00000B
P0M2	Port 0 output mode 2	B2H	P0M2.7	P0M2.6	P0M2.5	P0M2.4	P0M2.3	P0M2.2	P0M2.1	P0M2.0	00000000B
P0M1	Port 0 output mode 1	B1H	P0M1.7	P0M1.6	P0M1.5	P0M1.4	P0M1.3	P0M1.2	P0M1.1	P0M1.0	00000000B
IE	Interrupt enable	A8H	(AF) EA	(AE) EADC	(AD) EBO	(AC) -	(AB) ET1	(AA) EX1	(A9) ET0	(A8) EX0	000x0000B
EDIC	Edge detect control register	A3H	EDFLT.1	EDFLT.0	ED2TRG	ED2EN	ED1TRG	ED1EN	ED0TRG	ED0EN	00000000B
AUXR1	AUX function register	A2H	EDF	BOD	BOI	LPBOV	SRST	ADCEN	**BUZE**	-	000X000xB
P2	Port 2	A0H	(A7) -	(A6) -	(A5) -	(A4) -	(A3)	(A2)	(A1) P2.1 XTAL1	(A0) P2.0 XTAL2 CLKOUT	xxxxxxxxB
P1	Port 1	90H	(97) P1.7 PWM2	(96) P1.6 PWM1	(95) P1.5 /RST	(94) P1.4 /INT1 STADC	(93) P1.3 /INT0	(92) P1.2 ED2 T0	(91) P1.1 ED1	(90) P1.0 ED0 BUZ	11111111B
CKCON	Clock control	8EH	-	-	-	T1M	T0M	-	-	-	xxx00xxxB
TH1	Timer high 1	8DH									00000000B
TH0	Timer high 0	8CH									00000000B
TL1	Timer low 1	8BH									00000000B
TL0	Timer low 0	8AH									00000000B
TMOD	Timer mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00000000B
TCON	Timer control	88H	(8F) TF1	(8E) TR1	(8D) TF0	(8C) TR0	(8B) IE1	(8A) IT1	(89) IE0	(88) IT0	00000000B
PCON	Power control	87H	-	-	BOF	POR	GF1	GF0	PD	IDL	xxxx0000B
DPH	Data pointer high	83H									00000000B
DPL	Data pointer low	82H									00000000B
SP	Stack pointer	81H									00000111B
P0	Port 0	80H	(87) P0.7 AD7 T1	(86) P0.6 AD3	(85) P0.5 AD2	(84) P0.4 AD1	(83) P0.3 AD0	(82) P0.2 AD4 BRAKE	(81) P0.1 AD5 PWM0	(80) P0.0 AD6 PWM3	11111111B

Table 8-2: Special Function Registers

BIT	NAME	FUNCTION
7-6		Edge detect filter type bits: 00 – Filter clock = Fosc. 01 – Filter clock = Fosc/2. 10 – Filter clock = Fosc/4. 11 – Filter clock = Fosc/8.
5	ED2TRG	Edge detect 2 (ED2) trigger type bit: 0 – Falling edge on ED2 pin will cause EDF to be set (if ED2EN is enabled). 1 – Either falling or rising edge on ED2 pin will cause EDF to be set (if ED2EN is enabled).
4	ED2EN	Edge detect 2 (ED2) enable bit: 0 – Disabled. 1 – Enable ED2 (P1.2 pin) as a cause of an edge detect interrupt.
3	ED1TRG	Edge detect 1 (ED1) trigger type bit: 0 – Falling edge on ED1 pin will cause EDF to be set (if ED1EN is enabled). 1 – Either falling or rising edge on ED1 pin will cause EDF to be set (if ED1EN is enabled).
2	ED1EN	Edge detect 1 (ED1) enable bit: 0 – Disabled. 1 – Enable ED1 (P1.1 pin) as a cause of an edge detect interrupt.
1	ED0TRG	Edge detect 0 (ED0) trigger type bit: 0 – Falling edge on ED0 pin will cause EDF to be set (if ED0EN is enabled). 1 – Either falling or rising edge on ED0 pin will cause EDF to be set (if ED0EN is enabled).
0	ED0EN	Edge detect 0 (ED0) enable bit: 0 – Disabled. 1 – Enable ED0 (P1.0 pin) as a cause of an edge detect interrupt.

INTERRUPT ENABLE

Bit:	7	6	5	4	3	2	1	0
	EA	EADC	EBO	-	ET1	EX1	ET0	EX0

Mnemonic: IE Address: A8h

BIT	NAME	FUNCTION
7	-	Please Keep it at 0.
6~0	NVMADDR.[7:0]	The NVM address: The register indicates NVM data memory address on On-Chip code memory space.

TIMED ACCESS

Bit:	7	6	5	4	3	2	1	0
	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0

Mnemonic: TA Address: C7h

BIT	NAME	FUNCTION
7-0	TA.[7:0]	The Timed Access register: The Timed Access register controls the access to protected bits. To access protected bits, the user must first write AAH to the TA. This must be immediately followed by a write of 55H to TA. Now a window is opened in the protected bits for three machine cycles, during which the user can write to these bits.

NVM CONTROL

Bit:	7	6	5	4	3	2	1	0
	EER	EWR	-	-	-	-	-	-

Mnemonic: NVMCON Address: CEh

BIT	NAME	FUNCTION
7	EER	NVM page(n) erase bit: 0: Without erase NVM page(n). 1: Set this bit to erase page(n) of NVM. The NVM has **8** pages and each page have 16 bytes data memory. Initiate page select by programming NVMADDL register, which will automaticly enable page area. When user set this bit, the page erase process will begin and program counter will halt at this instruction. After the erase process is completed, program counter will continue executing next instruction.
6	EWR	NVM data write bit: 0: Without write NVM data. 1: Set this bit to write NVM bytes and program counter will halt at this instruction. After write is finished, program counter will kept next instruction then executed.
5-0	-	Reserved

NVM DATA

Bit:	7	6	5	4	3	2	1	0
	NVMDATA.7	NVMDATA.6	NVMDATA.5	NVMDATA.4	NVMDATA3	NVMDATA.2	NVMDATA.1	NVMDATA.0

Mnemonic: NVMDATA Address: CFh

BIT	NAME	FUNCTION
7~0	NVMDATA.[7:0]	The NVM data write register. The read NVM data is by MOVC instruction.

7~0	PWM1.[7:0]	PWM 1 Low Bits Register.

PWM CONTROL REGISTER 1

Bit:	7	6	5	4	3	2	1	0
	PWMRUN	Load	PWMF	CLRPWM	-	-	PWM1I	PWM0I

Mnemonic: PWMCON1 Address: DCh

BIT	NAME	FUNCTION
7	PWMRUN	0: The PWM is not running. 1: The PWM counter is running.
6	Load	0: The registers value of PWMP and PWMn are never loaded to counter and Comparator registers. 1: The PWMP and PWMn registers load value to counter and compare registers at the counter underflow. This bit is auto cleared by hardware at next clock cycle.
5	PWMF	PWM underflow flag: 0: The 10-bit counter down count is not underflow. 1: The 10-bit counter down count is underflow. (PWM interrupt is requested if PWM interrupt is enabled). This bit is Software clear.
4	CLRPWM	1: Clear 10-bit PWM counter to 000H. This bit is auto cleared by hardware.
3	PWM3I	0: PWM3 out is non-inverted. 1: PWM3 output is inverted.
2	PWM2I	0: PWM2 out is non-inverted. 1: PWM2 output is inverted.
1	PWM1I	0: PWM1 out is non-inverted. 1: PWM1 output is inverted.
0	PWM0I	0: PWM0 out is non-inverted. 1: PWM0 output is inverted.

PWM2 LOW BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	PWM2.7	PWM2.6	PWM2.5	PWM2.4	PWM2.3	PWM2.2	PWM2.1	PWM2.0

Mnemonic: PWM2L Address: DDh

BIT	NAME	FUNCTION
7~0	PWM2.[7:0]	PWM 2 Low Bits Register.

PWM3 LOW BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	PWM3.7	PWM3.6	PWM3.5	PWM3.4	PWM3.3	PWM3.2	PWM3.1	PWM3.0

Mnemonic: PWM3L Address: DEh

BIT	NAME	FUNCTION
7~0	PWM3.[7:0]	PWM 3 Low Bits Register.

PWM CONTROL REGISTER 2

Bit:	7	6	5	4	3	2	1	0
	BKCH	BKPS	BPEN	BKEN	PWM3B	PWM2B	PWM1B	PWM0B

Mnemonic: PWMCON2 Address: DFh

BIT	NAME	FUNCTION
7	BKCH	See the below table, when BKEN is set.
6	BKPS	0: Brake is asserted if P0.2 is low. 1: Brake is asserted if P0.2 is high
5	BPEN	See the below table, when BKEN is set.
4	BKEN	0: The Brake is never asserted. 1: The Brake is enabled, and see the below table.
3	PWM3B	0: The PWM3 output is low, when Brake is asserted. 1: The PWM3 output is high, when Brake is asserted.
2	PWM2B	0: The PWM2 output is low, when Brake is asserted. 1: The PWM2 output is high, when Brake is asserted.
1	PWM1B	0: The PWM1 output is low, when Brake is asserted. 1: The PWM1 output is high, when Brake is asserted.
0	PWM0B	0: The PWM0 output is low, when Brake is asserted. 1: The PWM0 output is high, when Brake is asserted.

BIT	NAME	FUNCTION
7-6	ADC.1-0	2 LSB of 10-bit A/D conversion result.
5	ADCEX	Enable STADC-triggered conversion 0: Conversion can only be started by software (i.e., by setting ADCS). 1: Conversion can be started by software or by a rising edge on STADC (pin P1.4).
4	ADCI	ADC Interrupt flag: This flag is set when the result of an A/D conversion is ready. This generates an ADC interrupt, if it is enabled. The flag may be cleared by the ISR. While this flag is 1, the ADC cannot start a new conversion. ADCI can not be set by software.
3	ADCS	ADC Start and Status: Set this bit to start an A/D conversion. It may also be set by STADC if ADCEX is 1. This signal remains high while the ADC is busy and is reset right after ADCI is set. ***Note:*** ***1. It is recommended to clear ADCI before ADCS is set. However, if ADCI is cleared and ADCS is set at the same time, a new A/D conversion may start on the same channel.*** ***2. Software clearing of ADCS will abort conversion in progress.*** ***3. ADC cannot start a new conversion while ADCS is high.***
2	RCCLK	0: The CPU clock is used as ADC clock source. 1: The internal RC 10MHz/20MHz (selectable by CONFIG1.FS1 bit) clock is used as ADC clock source. ***Note:*** ***1. This bit can only be set/cleared when ADCEN=0.*** ***2. The ADC clock source will goes through pre-scalar of /1, /2, /4 or /8, selectable by ADCLK bits (SFR ADCCON1.6-7).***
1	AADR1	The ADC input select. See table below.
0	AADR0	The ADC input select. See table below.

The ADCI and ADCS control the ADC conversion as below:

ADCI	ADCS	ADC STATUS
0	0	ADC not busy; A conversion can be started.
0	1	ADC busy; Start of a new conversion is blocked.
1	0	Conversion completed; Start of a new conversion requires ADCI = 0.
1	1	This is an internal temporary state that user can ignore it.

BIT	NAME	FUNCTION
7	PED	1: To set interrupt priority of Edge Detect is higher priority level.
6	PPWM	1: To set interrupt priority of PWM underflow is higher priority level.
5	PBK	1: To set interrupt priority of PWM's external brake is higher priority level.
4	PWDI	1: To set interrupt priority of Watchdog is higher priority level.
3-0	-	Reserved.

BUZZER CONTROL REGISTER

Bit:	7	6	5	4	3	2	1	0
	-	-	BUZDIV.5	BUZDIV.4	BUZDIV.3	BUZDIV.2	BUZDIV.1	BUZDIV.0

Mnemonic: BUZCON Address: F9h

BIT	NAME	FUNCTION
7-6	-	Reserved.
5-0	BUZDIV	Buzzer division select bits: These bits are division selector. User may configure these bits to further divide the cpu clock in order to generate the desired buzzer output frequency. The following shows the equation for the buzzer output rate; Fbuz = Fcpu x 1/[(256)x(BUZDIV + 1)]

INSTRUCTION SET, continued

Op-code	HEX Code	Bytes	W79E8213 series Machine Cycle	W79E8213 series Clock cycles	8032 Clock cycles	W79E8213 series v.s 8032 Speed Ratio
ORL direct, A	42	2	2	8	12	1.5
ORL direct, #data	43	3	3	12	24	2
XRL A, R0	68	1	1	4	12	3
XRL A, R1	69	1	1	4	12	3
XRL A, R2	6A	1	1	4	12	3
XRL A, R3	6B	1	1	4	12	3
XRL A, R4	6C	1	1	4	12	3
XRL A, R5	6D	1	1	4	12	3
XRL A, R6	6E	1	1	4	12	3
XRL A, R7	6F	1	1	4	12	3
XRL A, @R0	66	1	1	4	12	3
XRL A, @R1	67	1	1	4	12	3
XRL A, direct	65	2	2	8	12	1.5
XRL A, #data	64	2	2	8	12	1.5
XRL direct, A	62	2	2	8	12	1.5
XRL direct, #data	63	3	3	12	24	2
CLR A	E4	1	1	4	12	3
CPL A	F4	1	1	4	12	3
RL A	23	1	1	4	12	3
RLC A	33	1	1	4	12	3
RR A	03	1	1	4	12	3
RRC A	13	1	1	4	12	3
SWAP A	C4	1	1	4	12	3
MOV A, R0	E8	1	1	4	12	3
MOV A, R1	E9	1	1	4	12	3
MOV A, R2	EA	1	1	4	12	3
MOV A, R3	EB	1	1	4	12	3
MOV A, R4	EC	1	1	4	12	3
MOV A, R5	ED	1	1	4	12	3
MOV A, R6	EE	1	1	4	12	3
MOV A, R7	EF	1	1	4	12	3
MOV A, @R0	E6	1	1	4	12	3
MOV A, @R1	E7	1	1	4	12	3
MOV A, direct	E5	2	2	8	12	1.5

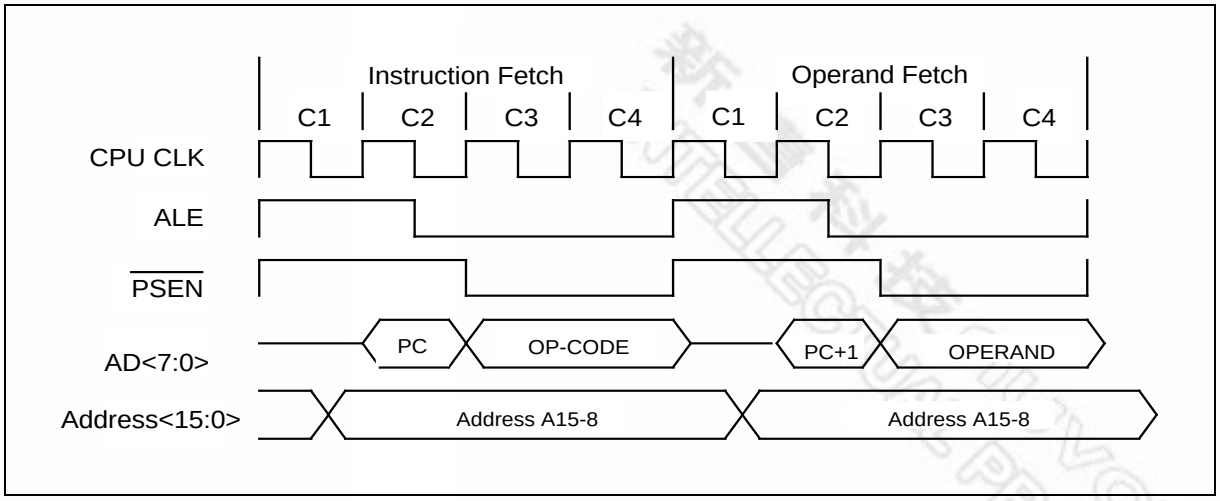


Figure 9-2: Two Cycles Instruction Timing

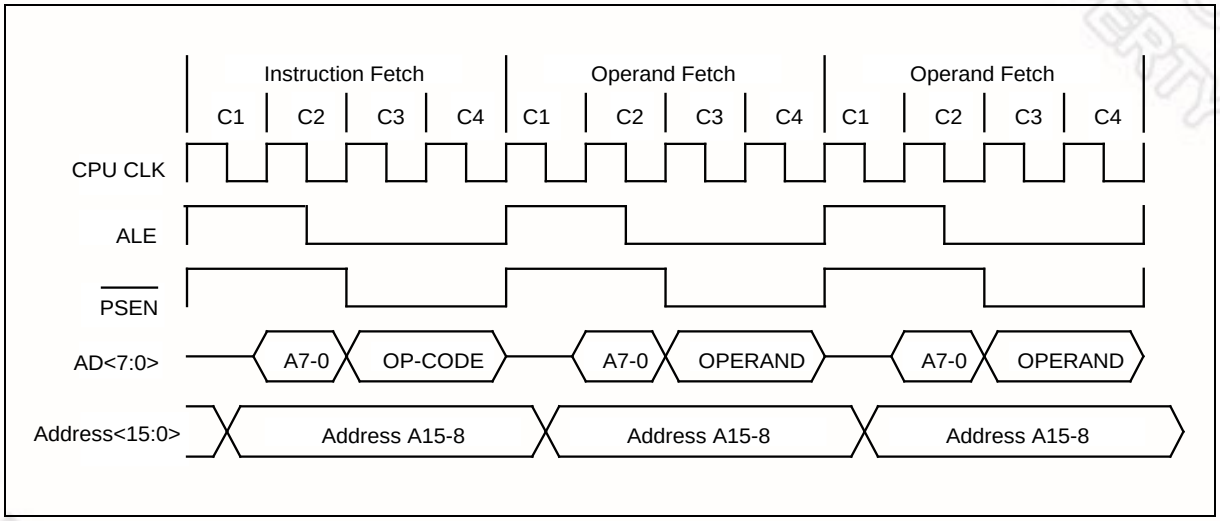


Figure 9-3: Three Cycles Instruction Timing

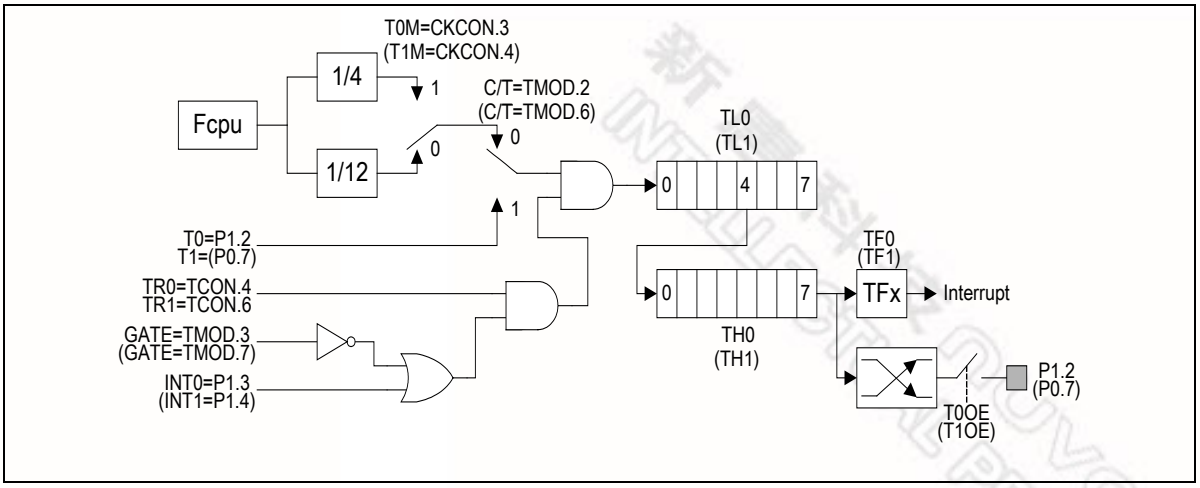


Figure 13-1: Timer/Counters 0 & 1 in Mode 0

13.1.3 Mode 1

Mode 1 is similar to Mode 0 except that the counting register forms a 16-bit counter, rather than a 13-bit counter. This means that all the bits of THx and TLx are used. Roll-over occurs when the timer moves from a count of FFFFh to 0000h. The timer overflow flag TFx of the relevant timer is set and if enabled an interrupt will occur. The selection of the time-base in the timer mode is similar to that in Mode 0. The gate function operates similarly to that in Mode 0.

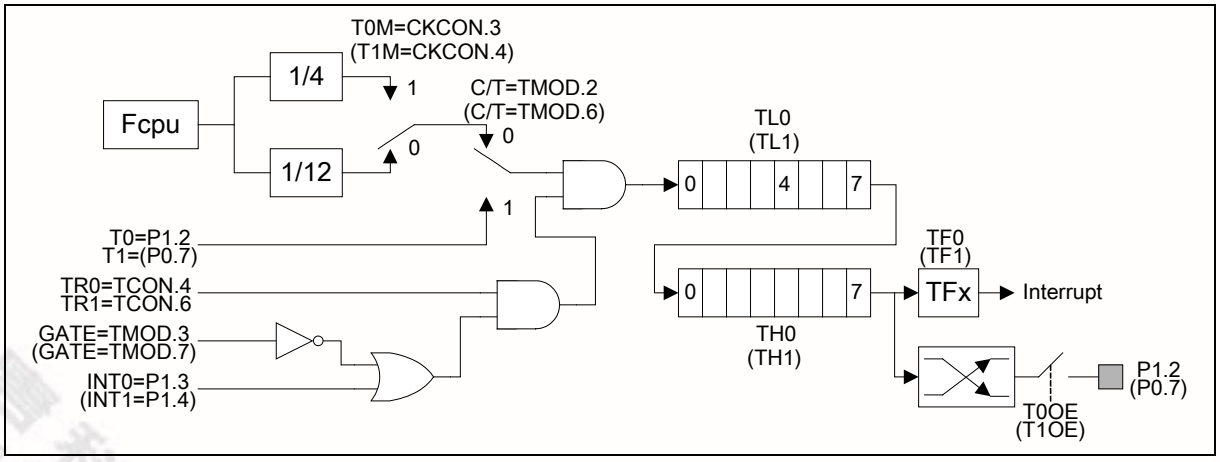


Figure 13-2: Timer/Counters 0 & 1 in Mode 1

16. TIME ACCESS PROCTECTION

The W79E8213 series have a new feature, like the Watchdog Timer which is a crucial to proper operation of the system. If left unprotected, errant code may write to the Watchdog control bits resulting in incorrect operation and loss of control. In order to prevent this, the W79E8213 series have a protection scheme which controls the write access to critical bits. This protection scheme is done using a timed access.

In this method, the bits which are to be protected have a timed write enable window. A write is successful only if this window is active, otherwise the write will be discarded. This write enable window is open for 3 machine cycles if certain conditions are met. After 3 machine cycles, this window automatically closes. The window is opened by writing AAh and immediately 55h to the Timed Access (TA) SFR. This SFR is located at address C7h. The suggested code for opening the timed access window is

```
TA      REG     0C7h            ; Define new register TA, @0C7h
        MOV     TA, #0AAh
        MOV     TA, #055h
```

When the software writes AAh to the TA SFR, a counter is started. This counter waits for 3 machine cycles looking for a write of 55h to TA. If the second write (55h) occurs within 3 machine cycles of the first write (AAh), then the timed access window is opened. It remains open for 3 machine cycles, during which the user may write to the protected bits. Once the window closes the procedure must be repeated to access the other protected bits.

Examples of Timed Assessing are shown below.

Example 1: Valid access

```
        MOV     TA, #0AAh       ; 3 M/C Note: M/C = Machine Cycles
        MOV     TA, #055h       ; 3 M/C
        MOV     WDCON, #00h     ; 3 M/C
```

Example 2: Valid access

```
        MOV     TA, #0AAh       ; 3 M/C
        MOV     TA, #055h       ; 3 M/C
        NOP                     ; 1 M/C
        SETB    EWRST           ; 2 M/C
```

Example 3: Valid access

```
        MOV     TA, #0AAh       ; 3 M/C
        MOV     TA, #055h       ; 3 M/C
        ORL     WDCON, #00000010B ; 3M/C
```

Example 4: Invalid access

```
        MOV     TA, #0AAh       ; 3 M/C
        MOV     TA, #055h       ; 3 M/C
        NOP                     ; 1 M/C
        NOP                     ; 1 M/C
        CLR     EWT             ; 2 M/C
```

provides the most source current for a quasi-bidirectional pin that output is “1” or port latch is logic “0”’.

The “very weak” pull-up is turned on when the port latch is logic “1”. If port latch is logic “0”, it will be turned off. The very weak pull-up is support a very small current that will pull the pin high if it is left floating. And the quasi-bidirectional port configuration is shown as below figure.

If port pin is low, it can drives large sink current for output, and it is similar with push-pull and open drain on sink current output.

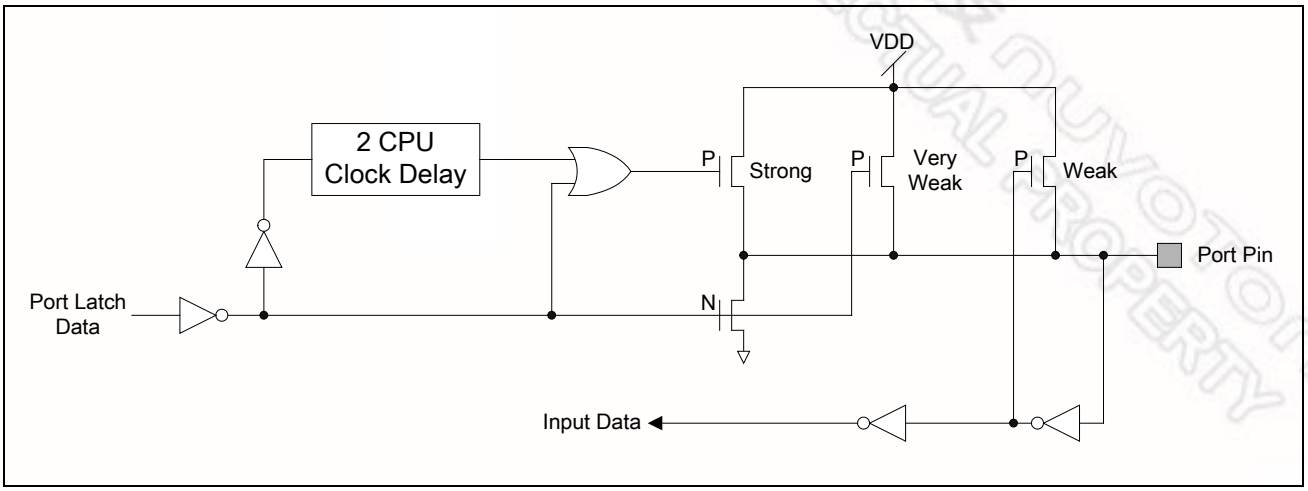


Figure 18-1: Quasi-Bidirectional Output

18.2 Open Drain Output Configuration

To configure this mode is turned off all pull-ups. If used similar as a logic output, the port must has an external pull-up resister. The open drain port configuration is shown as below.

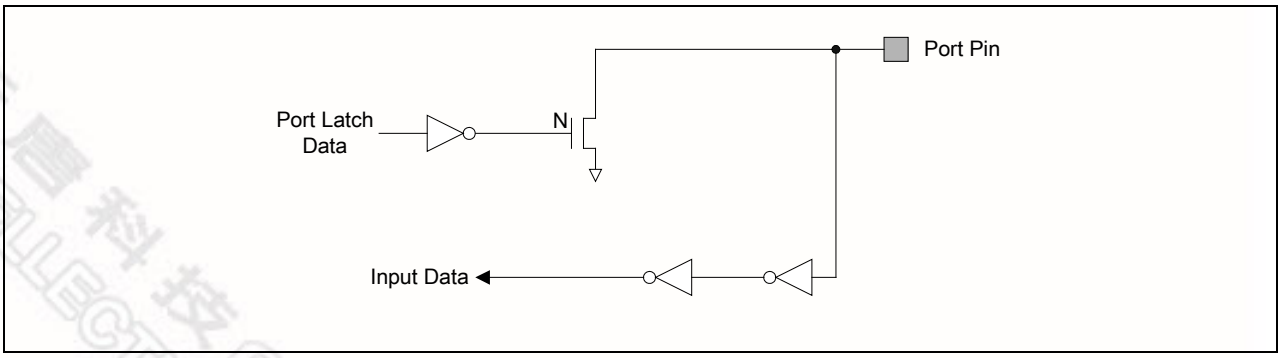


Figure 18-2: Open Drain Output

18.3 Push-Pull Output Configuration

The push-pull output mode has two strong pull-up and pull-down structure that support large source and sink current output. It removes “weak” pull-up and “very weak” pull-up resister and remains “strong pull-up resister on quasi-bidirectional output mode. The “strong” pull-up is always turns on when port latch is logic “1” to support source current. The push-pull port configuration is shown in below Figure.

For supporting active low buzzer, this buzzer output is implemented with an off-state of high. The following pseudo code shows the operating procedure when working with active high and low buzzer;

(Assume PRHI=1):

1) During power on, P1.0/BUZ will be high;

```
<For active high buzzer>
Clear SFR P1.0          ; user has to take care to output this pin low
                        ; at the top of s/w code to avoid initial beep sound.
<For active low buzzer>
No action needed.
```

2) To turn-on buzzer;

```
<For active high buzzer>
Set BUZE bit
Set SFR P1.0 bit        ; to push out the buzout.
<For active low buzzer>
Set BUZE bit
```

3) To turn-off buzzer;

```
<For active high buzzer>
Clear SFR P1.0          ; user has to take care to output this pin low.
Clear BUZE bit
<For active low buzzer>
Set BUZE bit
```

21. POWER MONITORING FUNCTION

Power-On Detect and Brownout are two additional power monitoring functions implemented in W79E8213 series to prevent incorrect operation during power up and power drop or loss.

21.1 Power On Detect

The Power–On Detect function is a designed to detect power up after power voltage reaches to a level where Brownout Detect can work. After power on detect, the POR (PCON.4) will be set to “1” to indicate an initial power up condition. The POR flag will be cleared by software.

21.2 Brownout Detect

The Brownout Detect function is detect power voltage is drops to brownout voltage level, and allows preventing some process work or indicate power warming. The W79E8213 series have two brownout voltage levels to select by BOV (CONFIG0.4). If BOV =0 that brownout voltage level is 3.8V, If BOV = 1 that brownout voltage level is 2.5V. When the Brownout voltage is drop to select level, the brownout detector will detect and keeps this active until VDD is returns to above brownout Detect voltage. The Brownout Detect block is as follow.

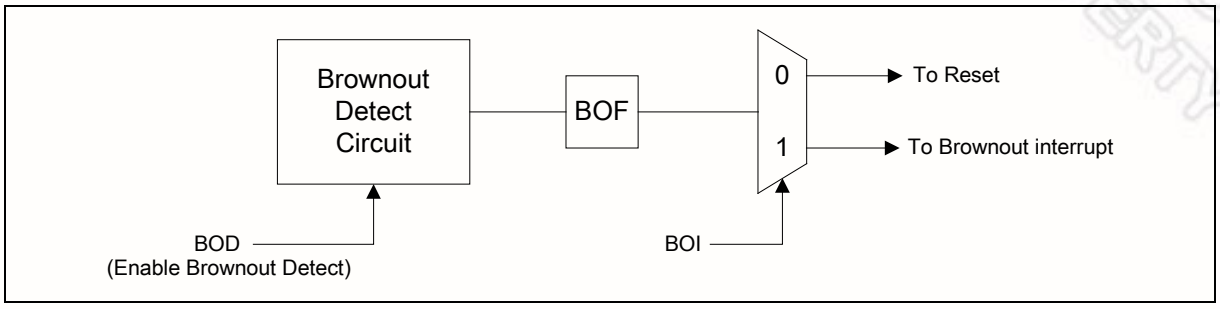


Figure 21-1: Brownout Detect Block

When Brownout Detect is enabled by BOD (AUXR1.6), the BOF (PCON.5) flag will be set and brownout reset will occur. If BOI (AUXR1.5) is set to “1”, the brownout detect will cause interrupt via the EA (IE.7) and EBO (IE.5) bits is set. BOF is cleared by software.

In order to guarantee a correct detection of Brownout, The VDD fail time must be slower than 50mV/us, and rise time is slower than 2mV/us to ensure a proper reset.

Oscillator Configuration bits:

Fosc1	Fosc0	OSC source
0	0	4MHz ~ 20MHz crystal
0	1	Internal RC Oscillator (FS1 bit in CONFIG1.5 will determine either 10MHz or 20MHZ)
1	0	Reserved
1	1	External Oscillator in XTAL1

25.2 CONFIG1

7	6	5	4	3	2	1	0
C7	C6	FS1	"1"	"1"	"1"	"1"	"1"

Bit7: C7 : 4K Flash EPROM Code Lock Bit
Bit6: C6 : 128 byte Data Lock Bit
Bit5: FS1 : Internal RC 10MHz/20MHz Selection Bit
Bit4~0: : Must be "1"

Figure 25-2: Config1 register bits (W79E8213 series)

C7: 4K Flash EPROM Lock bit

This bit is used to protect the customer's program code. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the Flash EPROM data and CONFIG Registers can not be accessed again.

C6: 128 byte Data Flash EPROM Lock bit

This bit is used to protect the customer's 128 bytes of data code. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the 128 bytes of Flash EPROM data and CONFIG Registers can not be accessed again.

BIT 7	BIT 6	FUNCTION DESCRIPTION
1	1	Both security of 4KB program code and 128 Bytes data area are not locked. They can be erased, programmed or read by Writer or ICP.
0	1	The 4KB program code area is locked. It can't be read by Writer or ICP. The 128 Bytes data area can be program or read. The bank erase is invalid.
1	0	Not supported.
0	0	Both security of 4KB program code and 128 Bytes data area are locked. They can't be read by Writer or ICP.

FS1: Internal RC Oscillator 10MHz/20MHz selection bit

This bit is used to select 10MHz or 20MHz internal RC oscillator.

FS1	Internal RC Oscillator Output
0	10MHz
1	20MHz (default)

Internal Oscillator Selection Table

26. ELECTRICAL CHARACTERISTICS

26.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNIT
DC Power Supply	VDD–VSS	-0.3	+7.0	V
Input Voltage	VIN	VSS-0.3	VDD+0.3	V
Operating Temperature	TA	-40	+85	°C
Storage Temperature	Tst	-55	+150	°C
P1 Sink current	ISK	-	90	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

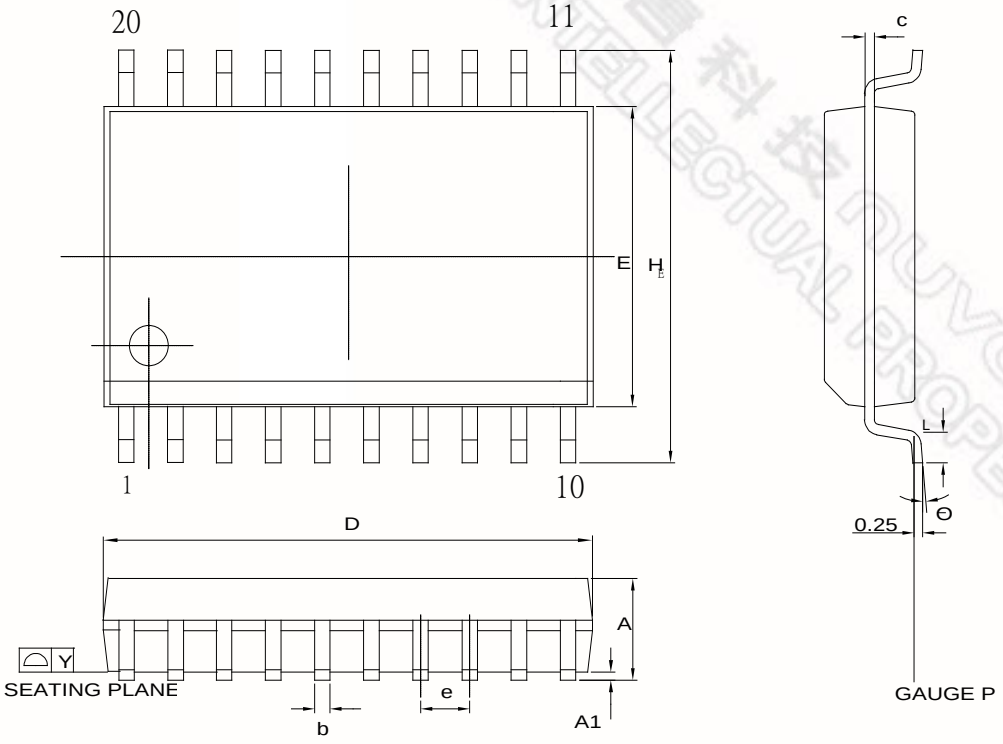
26.2 DC ELECTRICAL CHARACTERISTICS

(TA = -40~85°C, unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating Voltage	V_{DD1}	2.4	-	5.5	V	V_{DD}=4.5V ~ 5.5V @ 20MHz V_{DD}=2.7V ~ 5.5V @ 12MHz V_{DD}=2.4V ~ 5.5V @ 4MHz
	V_{DD2}	3.0	-	5.5		NVM program and erase operation.
Operating Current (20MHz)	I_{DD1}	-	8.30	12	mA	No load, /RST = VSS, V_{DD}= 5.0V @ 20MHz
	I_{DD2}	-	4.20	6		No load, /RST = VSS, V_{DD}= 3.0V @ 20MHz
	I_{DD3}	-	14.50	20		No load, /RST = V_{DD}, V_{DD}= 5.0V @ 20MHz, RUN NOP
	I_{DD4}	-	5.20	7		No load, /RST = V_{DD}, V_{DD}= 3.0V @ 20MHz, RUN NOP
Operating Current (4MHz)	I_{DD5}	-	3.60	5	mA	No load, /RST = VSS, V_{DD}= 5.0V @ 4MHz
	I_{DD6}	-	1.86	3		No load, /RST = VSS, V_{DD}= 3.0V @ 4MHz
	I_{DD7}	-	8.60	12		No load, /RST = V_{DD}, V_{DD}= 5.0V @ 4MHz, RUN NOP
	I_{DD8}	-	2.20	3.5		No load, /RST = V_{DD}, V_{DD}= 3.0V @ 4MHz, RUN NOP
Idle Current	I_{IDLE1}	-	5.70	8	mA	No load, V_{DD} = 5.0V @ 20MHz
	I_{IDLE2}	-	2.48	3.5		No load, V_{DD} = 3.0V @ 20MHz

27. PACKAGE DIMENSIONS

27.1 20-pin SOP-300mil



Control demensions are in milmeters .

SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	2.35	2.65	0.093	0.104
A1	0.10	0.30	0.004	0.012
b	0.33	0.51	0.013	0.020
c	0.23	0.32	0.009	0.013
E	7.40	7.60	0.291	0.299
D	12.60	13.00	0.496	0.512
e	1.27 BSC		0.050 BSC	
H_E	10.00	10.65	0.394	0.419
Y	—	0.10	—	0.004
L	0.40	1.27	0.016	0.050
θ	0	8	0	8