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1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers: PT16 and PT8.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

MC 9 S08 PT AA (V) B CC

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
MC	Qualification status	MC = fully qualified, general market flow
9	Memory	9 = flash based
S08	Core	S08 = 8-bit CPU
PT	Device family	PT
AA	Approximate flash size in KB	16 = 16 KB 8 = 8 KB
(V)	Mask set version	(blank) = Any version - A = Rev. 2 or later version, this is recommended for new design

Table continues on the next page...

Field	Description	Values
B	Operating temperature range (°C)	• V = –40 to 105
CC	Package designator	• LD = 44-LQFP • LC = 32-LQFP • TJ = 20-TSSOP • WJ = 20-SOIC • TG = 16-TSSOP

2.4 Example

This is an example part number:

MC9S08PT16VLD

3 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 1. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	-55	150	°C	1
T _{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	-6000	+6000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I _{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

4.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in below table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this document.

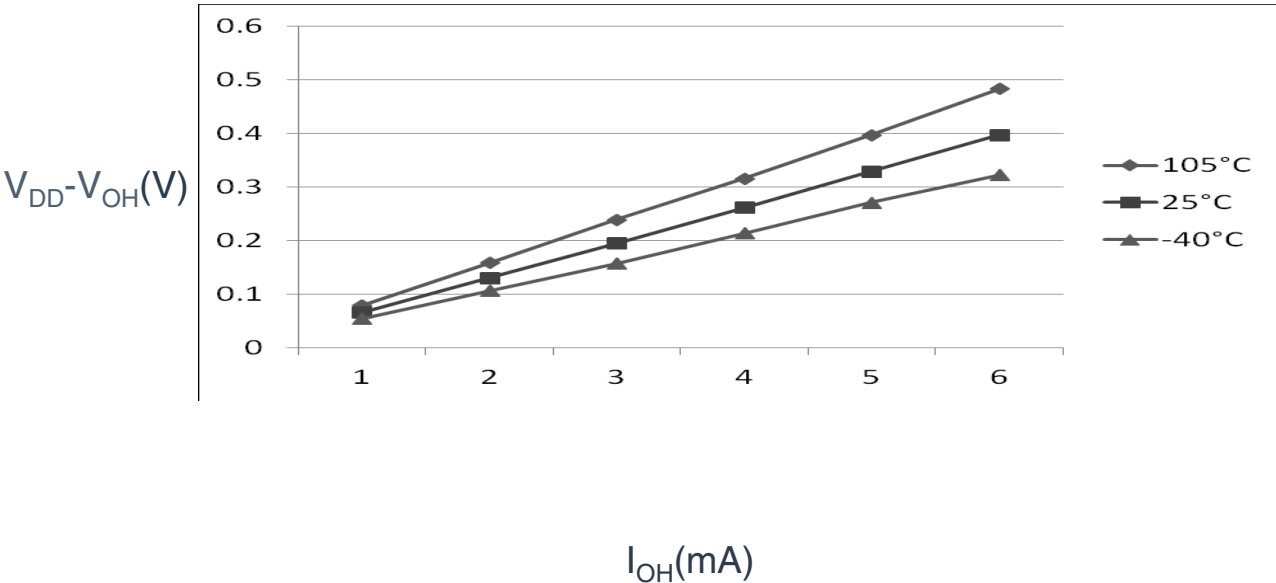


Figure 1. Typical I_{OH} Vs. V_{DD}-V_{OH} (standard drive strength) (V_{DD} = 5 V)

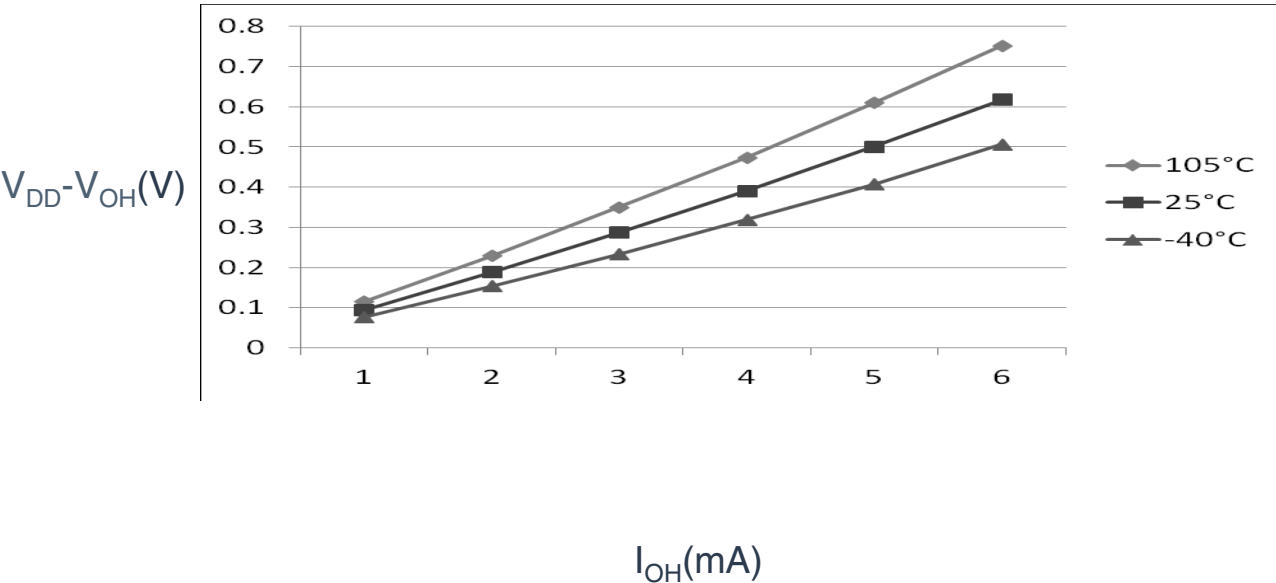


Figure 2. Typical I_{OH} Vs. V_{DD}-V_{OH} (standard drive strength) (V_{DD} = 3 V)

5.1.2 Supply current characteristics

This section includes information about power supply current in various operating modes.

Table 4. Supply current characteristics

Num	C	Parameter	Symbol	Bus Freq	V _{DD} (V)	Typical ¹	Max	Unit	Temp
1	C	Run supply current FEI mode, all modules on; run from flash	RI _{DD}	20 MHz	5	7.60	—	mA	-40 to 105 °C
	C			10 MHz		4.65	—		
	C			1 MHz		1.90	—		
	C			20 MHz	3	7.05	—		
	C			10 MHz		4.40	—		
	C			1 MHz		1.85	—		
2	C	Run supply current FEI mode, all modules off & gated; run from flash	RI _{DD}	20 MHz	5	5.88	—	mA	-40 to 105 °C
	C			10 MHz		3.70	—		
	C			1 MHz		1.85	—		
	C			20 MHz	3	5.35	—		
	C			10 MHz		3.42	—		
	C			1 MHz		1.80	—		
3	P	Run supply current FBE mode, all modules on; run from RAM	RI _{DD}	20 MHz	5	10.9	14.0	mA	-40 to 105 °C
	C			10 MHz		6.10	—		
	C			1 MHz		1.69	—		
	C			20 MHz	3	8.18	—		
	C			10 MHz		5.14	—		
	C			1 MHz		1.44	—		
4	P	Run supply current FBE mode, all modules off & gated; run from RAM	RI _{DD}	20 MHz	5	8.50	13.0	mA	-40 to 105 °C
	C			10 MHz		5.07	—		
	C			1 MHz		1.59	—		
	C			20 MHz	3	6.11	—		
	C			10 MHz		4.10	—		
	C			1 MHz		1.34	—		
5	C	Wait mode current FEI mode, all modules on	WI _{DD}	20 MHz	5	5.95	—	mA	-40 to 105 °C
	C			10 MHz		3.50	—		
	C			1 MHz		1.24	—		
	C			20 MHz	3	5.45	—		
	C			10 MHz		3.25	—		
	C			1 MHz		1.20	—		
6	C	Stop3 mode supply current no clocks active (except 1kHz LPO clock) ^{2,3}	S3I _{DD}	—	5	4.6	—	μA	-40 to 105 °C
	C			—	3	4.5	—		-40 to 105 °C
7	C	ADC adder to stop3	—	—	5	40	—	μA	-40 to 105 °C

Table continues on the next page...

Table 4. Supply current characteristics (continued)

Num	C	Parameter	Symbol	Bus Freq	V _{DD} (V)	Typical ¹	Max	Unit	Temp
	C	ADLPC = 1 ADLSMP = 1 ADCO = 1 MODE = 10B ADICLK = 11B			3	39	—		
8	C	TSI adder to stop3 ⁴	—	—	5	121	—	μA	-40 to 105 °C
	C	PS = 010B NSCN = 0x0F EXTCHRG = 0 REFCHRG = 0 DVOLT = 01B			3	120	—		
9	C	LVD adder to stop3 ⁵	—	—	5	128	—	μA	-40 to 105 °C
	C				3	124	—		

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. RTC adder cause <1 μA I_{DD} increase typically, RTC clock source is 1kHz LPO clock.
3. ACMP adder cause <10 μA I_{DD} increase typically.
4. The current varies with TSI configuration and capacity of touch electrode. Please refer to [TSI electrical specifications](#).
5. LVD is periodically woken up from stop3 by 5% duty cycle. The period is equal to or less than 2 ms.

5.1.3 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as [AN2321](#), [AN1050](#), [AN1263](#), [AN2764](#), and [AN1259](#) for advice and guidance specifically targeted at optimizing EMC performance.

5.1.3.1 EMC radiated emissions operating behaviors

Table 5. EMC radiated emissions operating behaviors for 44-pin LQFP package

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V _{RE1}	Radiated emissions voltage, band 1	0.15–50	8	dBμV	1, 2
V _{RE2}	Radiated emissions voltage, band 2	50–150	8	dBμV	
V _{RE3}	Radiated emissions voltage, band 3	150–500	8	dBμV	
V _{RE4}	Radiated emissions voltage, band 4	500–1000	5	dBμV	
V _{RE_IEC}	IEC level	0.15–1000	N	—	2, 3

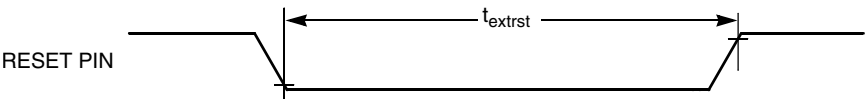


Figure 9. Reset timing

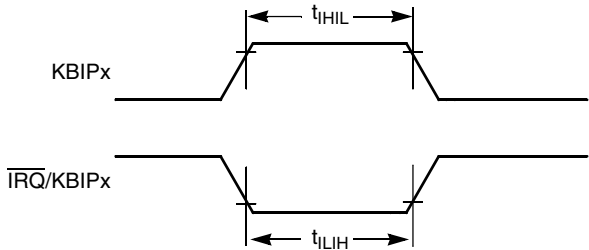


Figure 10. IRQ/KBIPx timing

5.2.2 Debug trace timing specifications

Table 7. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
t_{cyc}	Clock period	Frequency dependent		MHz
t_{wl}	Low pulse width	2	—	ns
t_{wh}	High pulse width	2	—	ns
t_r	Clock and data rise time	—	3	ns
t_f	Clock and data fall time	—	3	ns
t_s	Data setup	3	—	ns
t_h	Data hold	2	—	ns

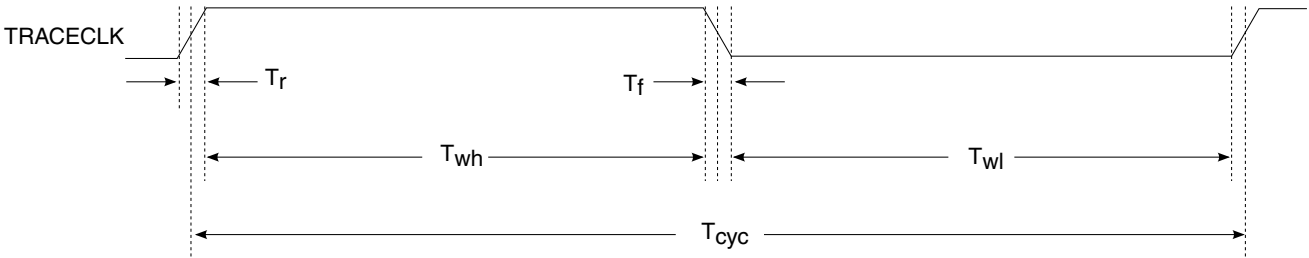


Figure 11. TRACE_CLKOUT specifications

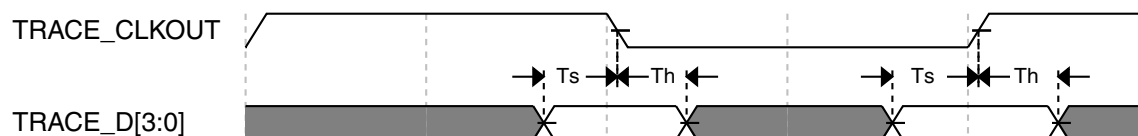


Figure 12. Trace data specifications

5.2.3 FTM module timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 8. FTM input timing

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
2	D	External clock period	t_{TCLK}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

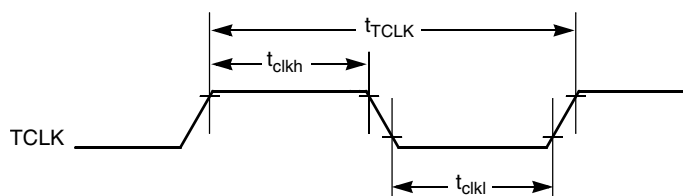


Figure 13. Timer external clock

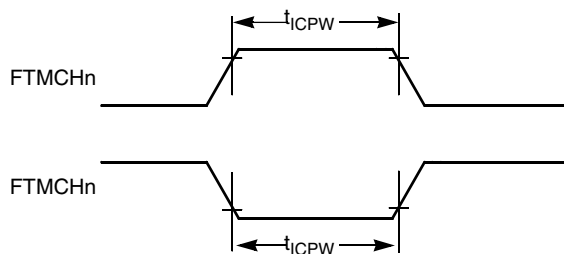


Figure 14. Timer input capture pulse

5.3 Thermal specifications

5.3.1 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 9. Thermal characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A ¹	T_L to T_H -40 to 105	°C
Junction temperature range	T_J	-40 to 150	°C
Thermal resistance single-layer board			
44-pin LQFP	$R_{\theta JA}$	76	°C/W
32-pin LQFP	$R_{\theta JA}$	88	°C/W
20-pin SOIC	$R_{\theta JA}$	82	°C/W
20-pin TSSOP	$R_{\theta JA}$	116	°C/W
16-pin TSSOP	$R_{\theta JA}$	130	°C/W
Thermal resistance four-layer board			
44-pin LQFP	$R_{\theta JA}$	54	°C/W
32-pin LQFP	$R_{\theta JA}$	59	°C/W
20-pin SOIC	$R_{\theta JA}$	54	°C/W
20-pin TSSOP	$R_{\theta JA}$	76	°C/W
16-pin TSSOP	$R_{\theta JA}$	87	°C/W

- Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA} \times \text{chip power dissipation}$.

6 Peripheral operating requirements and behaviors

6.1 External oscillator (XOSC) and ICS characteristics

Table 10. XOSC and ICS specifications (temperature range = -40 to 105 °C ambient)

Num	C	Characteristic		Symbol	Min	Typical ¹	Max	Unit
1	C	Oscillator crystal or resonator	Low range (RANGE = 0)	f_{lo}	31.25	32.768	39.0625	kHz
	C		High range (RANGE = 1) FEE or FBE mode ²	f_{hi}	4	—	20	MHz
	C		High range (RANGE = 1), high gain (HGO = 1), FBELP mode	f_{hi}	4	—	20	MHz
	C		High range (RANGE = 1), low power (HGO = 0), FBELP mode	f_{hi}	4	—	20	MHz
2	D	Load capacitors		C1, C2	See Note ³			
3	D	Feedback resistor	Low Frequency, Low-Power Mode ⁴	R_F	—	—	—	MΩ
			Low Frequency, High-Gain Mode		—	10	—	MΩ
			High Frequency, Low-Power Mode		—	1	—	MΩ
			High Frequency, High-Gain Mode		—	1	—	MΩ
4	D	Series resistor - Low Frequency	Low-Power Mode ⁴	R_S	—	—	—	kΩ
			High-Gain Mode		—	200	—	kΩ
5	D	Series resistor - High Frequency	Low-Power Mode ⁴	R_S	—	—	—	kΩ
	D	Series resistor - High Frequency, High-Gain Mode	4 MHz		—	0	—	kΩ
	D		8 MHz		—	0	—	kΩ
	D		16 MHz		—	0	—	kΩ
6	C	Crystal start-up time Low range = 32.768 kHz crystal; High range = 20 MHz crystal ^{5, 6}	Low range, low power	t_{CSTL}	—	1000	—	ms
	C		Low range, high power		—	800	—	ms
	C		High range, low power	t_{CSTH}	—	3	—	ms
	C		High range, high power		—	1.5	—	ms
7	T	Internal reference start-up time		t_{IRST}	—	20	50	μs
8	D	Square wave input clock frequency	FEE or FBE mode ²	f_{extal}	0.03125	—	5	MHz
	D		FBELP mode		0	—	20	MHz
9	P	Average internal reference frequency - trimmed		f_{int_t}	—	31.25	—	kHz
10	P	DCO output frequency range - trimmed		f_{dco_t}	16	—	20	MHz
11	P	Total deviation of DCO output from trimmed frequency ⁵	Over full voltage and temperature range	Δf_{dco_t}	—	—	±2.0	% f_{dco}
	C		Over fixed voltage and temperature range of 0 to 70 °C				±1.0	
12	C	FLL acquisition time ^{5, 7}		$t_{Acquire}$	—	—	2	ms

Table continues on the next page...

6.3 Analog

6.3.1 ADC characteristics

Table 12. 5 V 12-bit ADC operating conditions

Characteristic	Conditions	Symb	Min	Typ ¹	Max	Unit	Comment
Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	—
	Delta to V_{DD} ($V_{DD}-V_{DDAD}$)	ΔV_{DDA}	-100	0	+100	mV	
Ground voltage	Delta to V_{SS} ($V_{SS}-V_{SSA}$) ²	ΔV_{SSA}	-100	0	+100	mV	
Input voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
Input capacitance		C_{ADIN}	—	4.5	5.5	pF	
Input resistance		R_{ADIN}	—	3	5	k Ω	—
Analog source resistance	12-bit mode	R_{AS}	—	—	2	k Ω	External to MCU
	• $f_{ADCK} > 4$ MHz		—	—	5		
	• $f_{ADCK} < 4$ MHz		—	—	5		
	10-bit mode		—	—	5		
	• $f_{ADCK} > 4$ MHz		—	—	10		
	• $f_{ADCK} < 4$ MHz		—	—	10		
	8-bit mode		—	—	10		
	(all valid f_{ADCK})						
ADC conversion clock frequency	High speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	—
	Low power (ADLPC=1)		0.4	—	4.0		

1. Typical values assume $V_{DDA} = 5.0$ V, Temp = 25°C, $f_{ADCK}=1.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference.

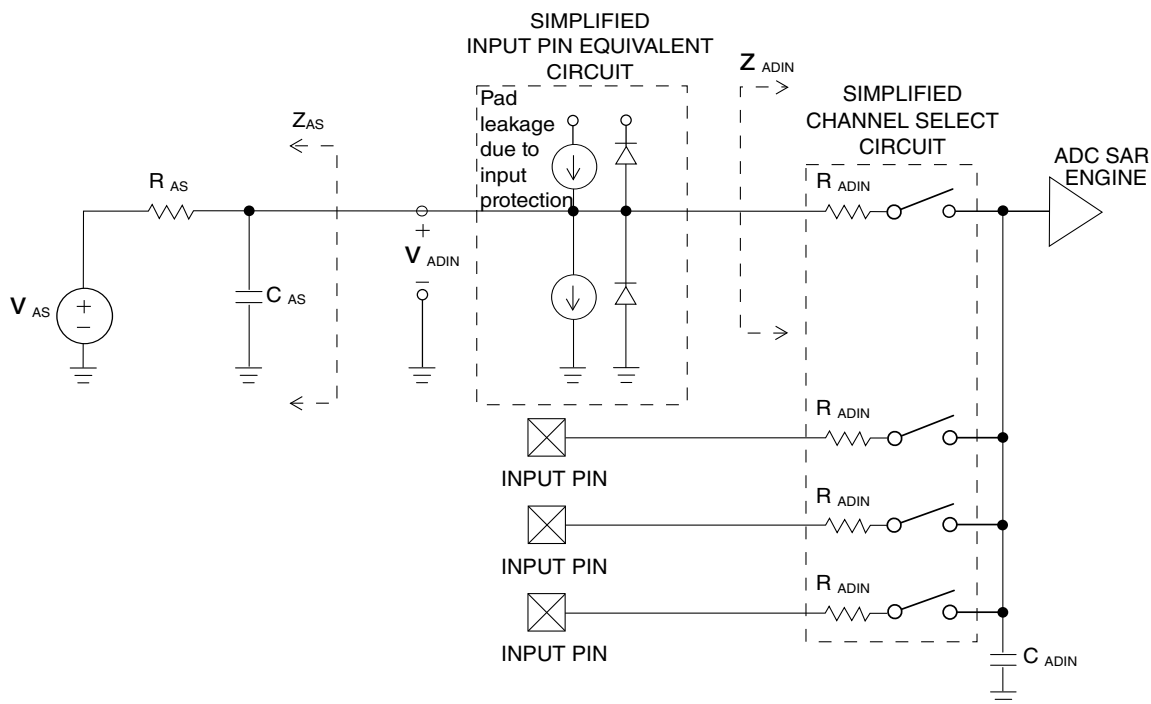


Figure 16. ADC input impedance equivalency diagram

Table 13. 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Characteristic	Conditions	C	Symb	Min	Typ ¹	Max	Unit
Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	133	—	μA
Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		T	I_{DDA}	—	218	—	μA
Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	327	—	μA
Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		T	I_{DDAD}	—	582	990	μA
Supply current	Stop, reset, module off	T	I_{DDA}	—	0.011	1	μA
ADC asynchronous clock source	High speed (ADLPC = 0)	P	f_{ADACK}	2	3.3	5	MHz

Table continues on the next page...

Table 13. 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Characteristic	Conditions	C	Symb	Min	Typ ¹	Max	Unit
	Low power (ADLPC = 1)			1.25	2	3.3	
Conversion time (including sample time)	Short sample (ADLSMP = 0)	T	t_{ADC}	—	20	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	40	—	
Sample time	Short sample (ADLSMP = 0)	T	t_{ADS}	—	3.5	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	23.5	—	
Total unadjusted Error ²	12-bit mode	T	E_{TUE}	—	±5.0	—	LSB ³
	10-bit mode	P		—	±1.5	±2.0	
	8-bit mode	P		—	±0.7	±1.0	
Differential Non-Linearity	12-bit mode	T	DNL	—	±1.0	—	LSB ³
	10-bit mode ⁴	P		—	±0.25	±0.5	
	8-bit mode ⁴	P		—	±0.15	±0.25	
Integral Non-Linearity	12-bit mode	T	INL	—	±1.0	—	LSB ³
	10-bit mode	T		—	±0.3	±0.5	
	8-bit mode	T		—	±0.15	±0.25	
Zero-scale error ⁵	12-bit mode	C	E_{ZS}	—	±2.0	—	LSB ³
	10-bit mode	P		—	±0.25	±1.0	
	8-bit mode	P		—	±0.65	±1.0	
Full-scale error ⁶	12-bit mode	T	E_{FS}	—	±2.5	—	LSB ³
	10-bit mode	T		—	±0.5	±1.0	
	8-bit mode	T		—	±0.5	±1.0	
Quantization error	≤12 bit modes	D	E_Q	—	—	±0.5	LSB ³
Input leakage error ⁷	all modes	D	E_{IL}	$I_{in} * R_{AS}$			mV
Temp sensor slope	-40°C– 25°C	D	m	—	3.266	—	mV/°C
	25°C– 125°C			—	3.638	—	
Temp sensor voltage	25°C	D	V_{TEMP25}	—	1.396	—	V

- Typical values assume $V_{DDA} = 5.0$ V, Temp = 25°C, $f_{ADCK} = 1.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- Includes quantization.
- 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
- Monotonicity and no-missing-codes guaranteed in 10-bit and 8-bit modes
- $V_{ADIN} = V_{SSA}$
- $V_{ADIN} = V_{DDA}$
- I_{in} = leakage current (refer to DC characteristics)

6.3.2 Analog comparator (ACMP) electricals

Table 14. Comparator electrical specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	V_{DDA}	2.7	—	5.5	V
T	Supply current (Operation mode)	I_{DDA}	—	10	20	μA
D	Analog input voltage	V_{AIN}	$V_{SS} - 0.3$	—	V_{DDA}	V
P	Analog input offset voltage	V_{AIO}	—	—	40	mV
C	Analog comparator hysteresis (HYST=0)	V_H	—	15	20	mV
C	Analog comparator hysteresis (HYST=1)	V_H	—	20	30	mV
T	Supply current (Off mode)	I_{DDAOFF}	—	60	—	nA
C	Propagation Delay	t_D	—	0.4	1	μs

6.4 Communication interfaces

6.4.1 SPI switching specifications

The serial peripheral interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. Refer to the SPI chapter of the chip's reference manual for information about the modified transfer formats used for communicating with slower peripheral devices. All timing is shown with respect to 20% V_{DD} and 70% V_{DD} , unless noted, and 100 pF load on all SPI pins. All timing assumes high drive strength is enabled for SPI output pins.

Table 15. SPI master mode timing

Nu m.	Symbol	Description	Min.	Max.	Unit	Comment
1	f_{op}	Frequency of operation	$f_{Bus}/2048$	$f_{Bus}/2$	Hz	f_{Bus} is the bus clock
2	t_{SPSCK}	SPSCK period	$2 \times t_{Bus}$	$2048 \times t_{Bus}$	ns	$t_{Bus} = 1/f_{Bus}$
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	$t_{Bus} - 30$	$1024 \times t_{Bus}$	ns	—
6	t_{SU}	Data setup time (inputs)	15	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_v	Data valid (after SPSCK edge)	—	25	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	$t_{Bus} - 25$	ns	—

Table continues on the next page...

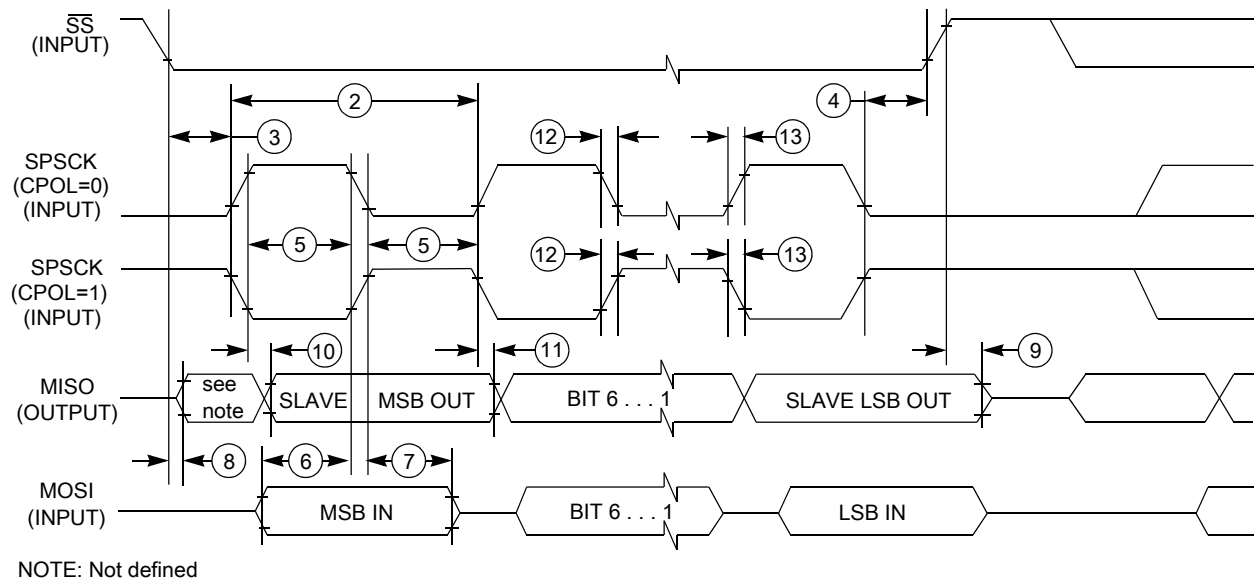


Figure 20. SPI slave mode timing (CPHA=1)

6.5 Human-machine interfaces (HMI)

6.5.1 TSI electrical specifications

Table 17. TSI electrical specifications

Symbol	Description	Min.	Type	Max	Unit
TSI_RUNF	Fixed power consumption in run mode	—	100	—	μA
TSI_RUNV	Variable power consumption in run mode (depends on oscillator's current selection)	1.0	—	128	μA
TSI_EN	Power consumption in enable mode	—	100	—	μA
TSI_DIS	Power consumption in disable mode	—	1.2	—	μA
TSI_TEN	TSI analog enable time	—	66	—	μs
TSI_CREF	TSI reference capacitor	—	1.0	—	pF
TSI_DVOLT	Voltage variation of VP & VM around nominal values	-10	—	10	%

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

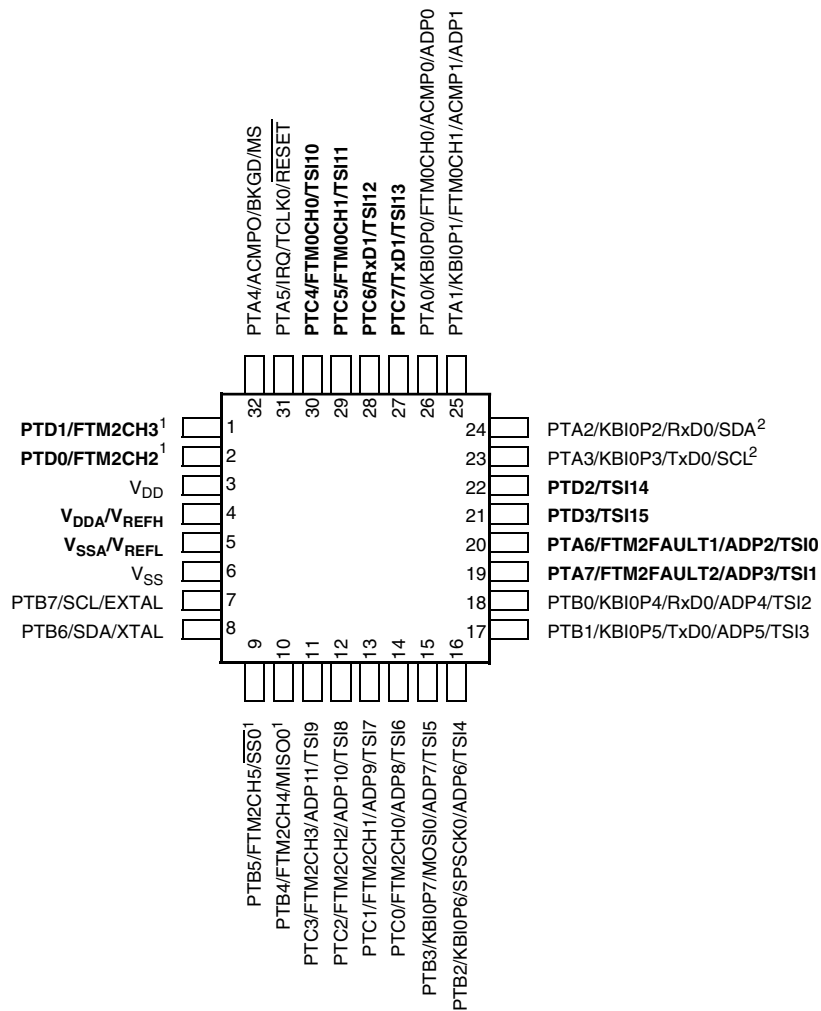
Table 18. Pin availability by package pin-count (continued)

Pin Number				Lowest Priority <-- --> Highest				
44-LQFP	32-LQFP	20-TSSOP	16-TSSOP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
18	—	—	—	PTD5	—	—	—	—
19	13	11	—	PTC1	—	FTM2CH1	ADP9	TSI7
20	14	12	—	PTC0	—	FTM2CH0	ADP8	TSI6
21	15	13	9	PTB3	KBI0P7	MOSI0	ADP7	TSI5
22	16	14	10	PTB2	KBI0P6	SPSCK0	ADP6	TSI4
23	17	15	11	PTB1	KBI0P5	TXD0	ADP5	TSI3
24	18	16	12	PTB0	KBI0P4	RXD0	ADP4	TSI2
25	19	—	—	PTA7	—	FTM2FAULT2	ADP3	TSI1
26	20	—	—	PTA6	—	FTM2FAULT1	ADP2	TSI0
27	—	—	—	—	—	—	—	Vss
28	—	—	—	—	—	—	—	V _{DD}
29	—	—	—	PTD4	—	—	—	—
30	21	—	—	PTD3	—	—	—	TSI15
31	22	—	—	PTD2	—	—	—	TSI14
32	23	17	13	PTA3 ²	KBI0P3	TXD0	SCL	—
33	24	18	14	PTA2 ²	KBI0P2	RXD0	SDA	—
34	25	19	15	PTA1	KBI0P1	FTM0CH1	ACMP1	ADP1
35	26	20	16	PTA0	KBI0P0	FTM0CH0	ACMP0	ADP0
36	27	—	—	PTC7	—	TxD1	—	TSI13
37	28	—	—	PTC6	—	RxD1	—	TSI12
38	—	—	—	PTE2	—	MISO0	—	—
39	—	—	—	PTE1	—	MOSI0	—	—
40	—	—	—	PTE0	—	SPSCK0	—	—
41	29	—	—	PTC5	—	FTM0CH1	—	TSI11
42	30	—	—	PTC4	—	FTM0CH0	—	TSI10
43	31	1	1	PTA5	IRQ	TCLK0	—	RESET
44	32	2	2	PTA4	—	ACMPO	BKGD	MS

1. This is a high current drive pin when operated as output.
2. This is a true open-drain pin when operated as output.

Note

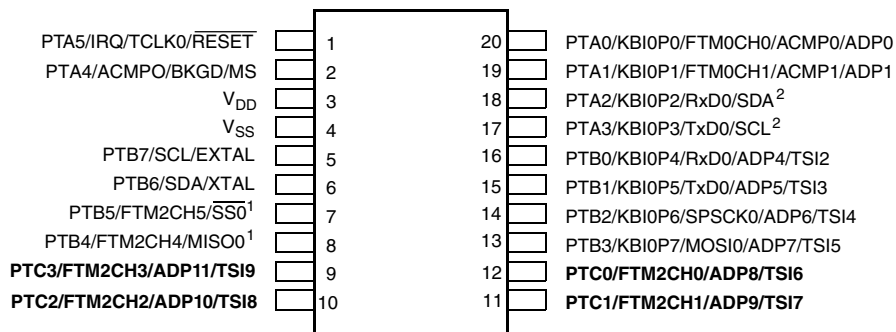
When an alternative function is first enabled, it is possible to get a spurious edge to the module. User software must clear any associated flags before interrupts are enabled. The table above illustrates the priority if multiple modules are enabled. The highest priority module will have control over the pin. Selecting a higher priority pin function with a lower priority function



Pins in **bold** are not available on less pin-count packages.

1. High source/sink current pins
2. True open drain pins

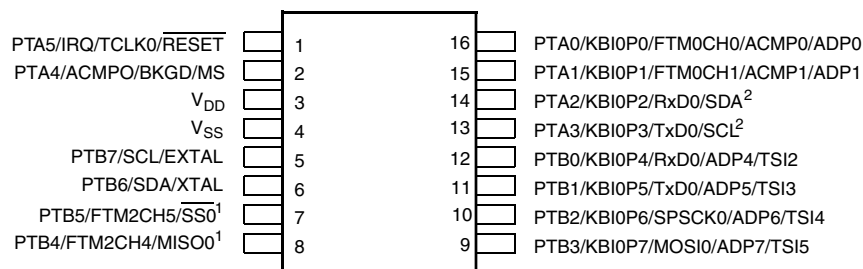
Figure 22. MC9S08PT16 32-pin LQFP package



Pins in **bold** are not available on less pin-count packages.

1. High source/sink current pins
2. True open drain pins

Figure 23. MC9S08PT16 20-pin SOIC and TSSOP package



Pins in **bold** are not available on less pin-count packages.

1. High source/sink current pins

2. True open drain pins

Figure 24. MC9S08PT16 16-pin TSSOP package

9 Revision history

The following table provides a revision history for this document.

Table 19. Revision history

Rev. No.	Date	Substantial Changes
1	7/2012	Initial public release
2	09/2014	- Updated V_{OH} and V_{OL} in DC characteristics - Added footnote on the $S3I_{DD}$ in Supply current characteristics - Added EMC radiated emissions operating behaviors - Updated the typical of f_{int_t} to 31.25 kHz and updated footnote to $t_{Acquire}$ in External oscillator (XOSC) and ICS characteristics - Updated the assumption for all the timing values in SPI switching specifications - Updated the rating descriptions for t_{Rise} and t_{Fall} in Control timing - Updated the part number format to add new field for new part numbers in Fields
3	06/2015	- Corrected the Min. of the t_{extrst} in Control timing - Updated Thermal characteristics to add footnote to the T_A and removed redundant information. Updated the symbol of θ_{JA} to $R_{\theta JA}$.

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