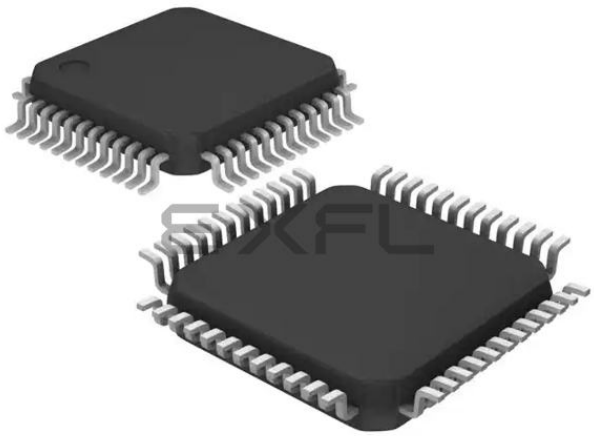

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Details	
Product Status	Active
Applications	Audio Record/Playback
Core Processor	ARM® Cortex®-M0
Program Memory Type	FLASH (145kB)
Controller Series	-
RAM Size	12K x 8
Interface	I²C, IrDA, LIN, SPI, UART/USART
Number of I/O	8
Voltage - Supply	2.5V ~ 5.5V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/isd9160fi-tr

IRQ0 ~ IRQ31 Set-Pending Control Register（NVIC_ISPR）

Register	Offset	R/W	Description	Reset Value
NVIC_ISPR	SCS_BA+0x200	R/W	IRQ0 ~ IRQ31 Set-Pending Control Register	0x0000_0000

Table 5-20 Interrupt Set-Pending Control Register (ISPR, address 0xE000_E200)

Bits	Description	
[31:0]	**SETPEND**	**Set-Pending Control** Writing 1 to a bit forces pending state of the associated interrupt under software control. Each bit represents an interrupt number from IRQ0 ~ IRQ31 (Vector number from 16 ~ 47). Writing 0 has no effect. The register reads back with the current pending state.

IRQ18(I2C0) Interrupt Source Identify Register (IRQ18_SRC)

Register	Offset	R/W	Description	Reset Value
IRQ18_SRC	INT_BA+0x48	R	IRQ18 (I2C0) Interrupt Source Identity Register	0xXXXX_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved					**INT_SRC[2:0]**		

Bits	Description	
[2:0]	**INT_SRC**	**Interrupt Source Identity** Bit2: 0 Bit1: 0 Bit0: I2C0_INT

Application Interrupt and Reset Control Register (SYSCTL_AIRCTL)

Register	Offset	R/W	Description	Reset Value
SYSCTL_AIRCTL	SYSINFO_BA+0xD0C	R/W	**Application Interrupt and Reset Control Register**	0x0000_0000

31	30	29	28	27	26	25	24
VTKEY							
23	22	21	20	19	18	17	16
VTKEY							
15	14	13	12	11	10	9	8
ENDIANES	Reserved						
7	6	5	4	3	2	1	0
Reserved					SRSTREQ	CLRACTVT	Reserved

Bits	Description	
[31:16]	**VTKEY**	**Vector Key** The value 0x05FA must be written to this register, otherwise a write to register is UNPREDICTABLE.
[15]	**ENDIANES**	**Endianess** Read Only. Reads 0 indicating little endian machine.
[2]	**SRSTREQ**	**System Reset Request** 0 =do not request a reset. 1 =request reset. Writing 1 to this bit asserts a signal to request a reset by the external system.
[1]	**CLRACTVT**	**Clear All Active Vector** Clears all active state information for fixed and configurable exceptions. 0= do not clear state information. 1= clear state information. The effect of writing a 1 to this bit if the processor is not halted in Debug, is UNPREDICTABLE.

Interrupt De-bounce Control (GPIO_DBCTL)

Register	Offset	R/W	Description	Reset Value
GPIO_DBCTL	GPIO_BA+0x180	R/W	Interrupt De-bounce Control	0x0000_0020

Table 5-51 GPIO Interrupt De-bounce Control Register (GPIO_DBCTL)

7	6	5	4	3	2	1	0
Reserved		ICLKON	DBCLKSRC	DBCLKSEL			

Bits	Description	
[5]	ICLKON	**Interrupt Clock On Mode** Set this bit “0” will gate the clock to the interrupt generation circuit if the GPIOx[n] interrupt is disabled. 0 = disable the clock if the GPIOx[n] interrupt is disabled 1 = Interrupt generation clock always active.
[4]	DBCLKSRC	**De-bounce Counter Clock Source Select** 0 = De-bounce counter clock source is HCLK 1 = De-bounce counter clock source is the internal 16 kHz clock
[3:0]	DBCLKSEL	**De-bounce Sampling Cycle Selection.** For edge level interrupt GPIO state is sampled every 2^(DBCLKSEL) de-bounce clocks. For example if DBCLKSRC aaa 6, then interrupt is sampled every 2^6 aaa 64 de-bounce clocks. If DBCLKSRC is 16KHz oscillator this would be a 64ms de-bounce.

Detection Time Multiplex Register (BODTALM_BODDTMR)

The BOD detector can be set up to take periodic samples of the supply voltage to minimize power consumption. The circuit can be configured and used in Standby Power Down (SPD) mode and can wake up the device if a BOD is event detected. The detection timer uses the OSC16K oscillator as time base so this oscillator must be active for timer operation. When active the BOD circuit requires ~165uA. With default timer settings, average current reduces to 500nA 165uA*DURTON/(DURTON+DURTOFF).

Register	Offset	R/W	Description	Reset Value
BODTALM_BODDTMR	BODTALM_BA+0x10	R/W	Brown Out Detector Timer Register	0x0003_03E3

Table 5-54 Detection Time Multiplex Register (BODTALM_BODDTMR, address 0x4008_4010)

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved				**DURTON[3:0]**			
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
DURTOFF[15:8]							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
DURTOFF[7:0]							

Bits	Description	
[31:20]	Reserved	Reserved
[19:16]	**DURTON**	**Time BOD Detector Is Active** (DURTON+1) * 100us. Minimum value is 1. (default is 400us)
[15:0]	**DURTOFF**	**Time BOD Detector Is Off** (DURTOFF+1)*100us . Minimum value is 7. (default is 99.6ms)

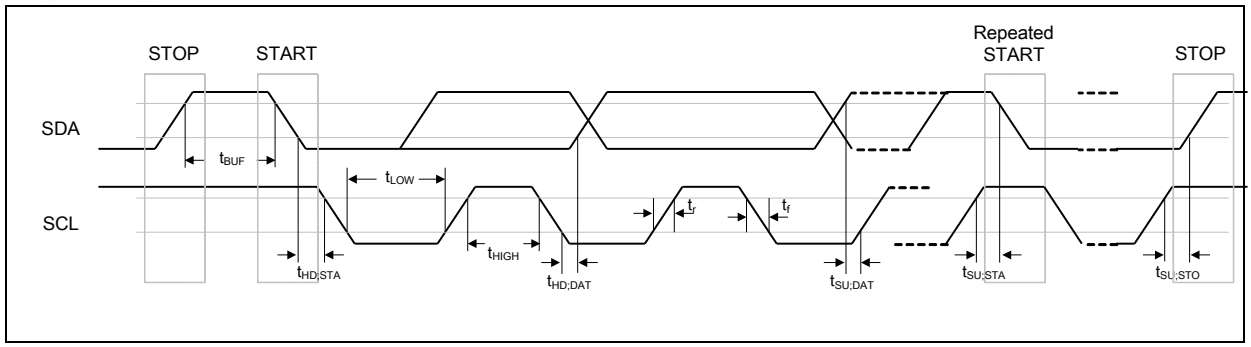

Figure 5-9 I2C Bus Timing

The device's on-chip I2C logic provides the serial interface that meets the I2C bus standard mode specification. The I2C port handles byte transfers autonomously. To enable this port, the bit ENS1 in I2C_CTL should be set to '1'. The I2C H/W interfaces to the I2C bus via two pins: I2C_SDA (which can be configured as GPIOA[10], GPIOB[3] or GPIOA[3], serial data line) and I2C_SCL (which can be configured as GPIOA[11], GPIOB[2] or GPIOA[1], serial clock line). See **Error! Reference source not found.** and **Error! Reference source not found.** for alternate GPIO pin functions. Pull up resistor is needed for these pins for I2C operation as these are open drain pins.

The I2C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the bus are:

- Master/Slave up to 1Mbit/s
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- Built-in a 14-bit time-out counter will request the I2C interrupt if the I2C bus hangs up and timer-out counter overflows.
- External pull-up are needed for high output
- Programmable clocks allow versatile rate control
- Supports 7-bit addressing mode
- I2C-bus controllers support multiple address recognition (Four slave address with mask option)

5.6.1.1 *I^2C Protocol*

Normally, a standard communication consists of four parts:

1) START or Repeated START signal generation
2) Slave address transfer
3) Data transfer
4) STOP signal generation

I2C TIME-OUT COUNTER REGISTER (I2C_TOCTL)

Register	Offset	R/W	Description	Reset Value
I2C_TOCTL	I2C_BA+0x14	R/W	I2C Time out control Register	0x0000_0000

7	6	5	4	3	2	1	0
Reserved					TOCEN	TOCDIV4	TOIF

Bits	Description	
[2]	TOCEN	**Time-out Counter Control Bit** 0 = Disable 1 = Enable When enabled, the 14 bit time-out counter will start counting when SI is clear. Setting flag SI to high will reset counter and re-start up counting after SI is cleared.
[1]	TOCDIV4	**Time-Out Counter Input Clock Divide By 4** 0 = Disable 1 = Enable When enabled, the time-out clock is PCLK/4.
[0]	TOIF	**Time-Out Flag** 0 = No time-out. 1 = Time-out flag is set by H/W. It can interrupt CPU. Write 1 to clear..

[0]	CNTEN0	**PWM-Timer 0 Enable/Disable Start Run** 0 = Stop PWM-Timer 0 Running 1 = Enable PWM-Timer 0 Start/Run

IrDA Control Register (UART_IRDA)

Register	Offset	R/W	Description	Reset Value
UART_IRDA	UART0_BA + 0x28	R/W	UART0 IrDA Control Register.	0x0000_0040

7	6	5	4	3	2	1	0
Reserved	**RXINV**	**TXINV**	**Reserved**		**LOOPBACK**	**TXEN**	**Reserved**

Table 5-111 UART IrDA Control Register (UART_IRDA, address 0x4005_0028)

Bits	Description	
[31:7]	Reserved	Reserved
[6]	**RXINV**	**Receive Inversion Enable** 0= No inversion 1= Invert Rx input signal
[5]	**TXINV**	**Transmit inversion enable** 0= No inversion 1= Invert Tx output signal
[4:3]	Reserved	Reserved
[2]	**LOOPBACK**	**IrDA Loopback Test Mode** Loopback Tx to Rx.
[1]	**TXEN**	**Transmit/Receive Selection** 0=Enable IrDA receiver. 1= Enable IrDA transmitter.
[0]	Reserved	Reserved

I2S Status Register (I2S_STATUS)

Register	Offset	R/W	Description	Reset Value
I2S_STATUS	I2S_BA + 0x0C	R/W	I2S Status Register	0x0014_1000

31	30	29	28	27	26	25	24
TXCNT				RXCNT			
23	22	21	20	19	18	17	16
LZCIF	RZCIF	TXBUSY	TXEMPTY	TXFULL	TXTHIF	TXOVIF	TXUDIF
15	14	13	12	11	10	9	8
Reserved			RXEMPTY	RXFULL	RXTHIF	RXOVIF	RXUDIF
7	6	5	4	3	2	1	0
Reserved				RIGHT	TXIF	RXIF	I2SIF

Table 5-117 I2S Status Register (I2S_STATUS, address 0x400A_000C)

Bits	Description	
[31:28]	TXCNT	**Transmit FIFO level (Read Only)** TXCNT = number of words in transmit FIFO.
[27:24]	RXCNT	**Receive FIFO level (Read Only)** RXCNT = number of words in receive FIFO.
[23]	LZCIF	**Left channel zero cross flag (write '1' to clear, or clear LZCEN)** 0 = No zero cross detected. 1 = Left channel zero cross is detected
[22]	RZCIF	**Right channel zero cross flag (write '1' to clear, or clear RZCEN)** 0 = No zero cross 1 = Right channel zero cross is detected
[21]	TXBUSY	**Transmit Busy (Read Only)** This bit is cleared when all data in transmit FIFO and Tx shift register is shifted out. It is set when first data is loaded to Tx shift register. 0 = Transmit shift register is empty 1 = Transmit shift register is busy
[20]	TXEMPTY	**Transmit FIFO Empty (Read Only)** This is set when transmit FIFO is empty. 0 = Not empty 1 = Empty

[19]	TXFULL	**Transmit FIFO Full (Read Only)** This bit is set when transmit FIFO is full. 0 = Not full. 1 = Full.
[18]	TXTHIF	**Transmit FIFO Threshold Flag (Read Only)** When data word(s) in transmit FIFO is less than or equal to the threshold value set in TXTH[2:0] the TXTHIF bit becomes to 1. It remains set until transmit FIFO level is greater than TXTH[2:0]. Cleared by writing to I2S_TX register until threshold exceeded. 0 = Data word(s) in FIFO is greater than threshold level 1 = Data word(s) in FIFO is less than or equal to threshold level
[17]	TXOVIF	**Transmit FIFO Overflow Flag (Write '1' to clear)** This flag is set if data is written to transmit FIFO when it is full. 0 = No overflow 1 = Overflow
[16]	TXUDIF	**Transmit FIFO underflow flag (Write '1' to clear)** This flag is set if I2S controller requests data when transmit FIFO is empty. 0 = No underflow 1 = Underflow
[15:13]	Reserved	Reserved
[12]	RXEMPTY	**Receive FIFO empty (Read Only)** This is set when receive FIFO is empty. 0 = Not empty 1 = Empty
[11]	RXFULL	**Receive FIFO full (Read Only)** This bit is set when receive FIFO is full. 0 = Not full. 1 = Full.
[10]	RXTHIF	**Receive FIFO Threshold Flag (Read Only)** When data word(s) in receive FIFO is greater than or equal to threshold value set in RXTH[2:0] the RXTHIF bit becomes to 1. It remains set until receive FIFO level is less than RXTH[2:0]. It is cleared by reading I2S_RX until threshold satisfied. 0 = Data word(s) in FIFO is less than threshold level 1 = Data word(s) in FIFO is greater than or equal to threshold level
[9]	RXOVIF	**Receive FIFO Overflow Flag (Write '1' to clear)** This flag is set if I2S controller writes to receive FIFO when it is full. Audio data is lost. 0 = No overflow 1 = Overflow

[1]	BS	**Boot Select** 0 = APROM 1 = LDROM Modify this bit to select which ROM next boot is to occur. This bit also functions as MCU boot status flag, which can be used to check where MCU booted from. This bit is initialized after power-on reset with the inverse of CBS in Config0; It is not reset for any other reset event.
[0]	ISPEN	**ISP Enable** 0 = Disable ISP function 1 = Enable ISP function

ISP Data Register (FMC_ISPDAT)

Register	Offset	R/W	Description	Reset Value
FMC_ISPDAT	FMC_BA+0x08	R/W	ISP Data Register	0x0000_0000

Table 6-8 ISP Data Register (FMC_ISPDAT, address 0x5000_C008)

Bits	Description	
[31:0]	**ISPDAT**	**ISP Data Register** Write data to this register before an ISP program operation. Read data from this register after an ISP read operation

DPWM FIFO Status Register (DPWM_STS)

Register	Offset	R/W	Description	Reset Value
DPWM_STS	DPWM_BA+0x04	R	DPWM FIFO Status Register	0x0000_0002

Table 7-15 DPWM FIFO Status Register (DPWM_STS, address 0x4007_0004)

Bits	Description	
[1]	**EMPTY**	**FIFO Empty** 0= FIFO is not empty 1= FIFO is empty
[0]	**FULL**	**FIFO Full** 0 = FIFO is not full. 1 = FIFO is full.

7.4 Analog Functional Blocks

7.4.1 Overview

The ISD9160 contains a variety of analog functional blocks that facilitate audio processing, enable analog GPIO functions (current source, relaxation oscillator, and comparator), adjust and measure internal oscillator and provide voltage regulation. These blocks are controlled by registers in the analog block address space. This section describes these functions and registers.

7.4.2 Features

- VMID reference voltage generation.
- Current source generation for AGPIO (Analog enabled GPIO).
- LDO control for GPIOA[7:0] power domain and external device use.
- Microphone Bias generator.
- Analog Multiplexor.
- Programmable Gain Amplifier (PGA).
- OSC48M Frequency Control.
- Capacitive Touch Sensing Relaxation Oscillator.
- Oscillator Frequency Measurement block.

7.4.3 Register Map

R: read only, **W**: write only, **R/W**: read/write

Register	Offset	R/W	Description	Reset Value
ANA Base Address: **ANA_BA = 0x4008_0000**				
ANA_VMID	ANA_BA+0x00	R/W	VMID Reference Control Register	0x0000_0007
ANA_CURCTL0	ANA_BA+0x08	R/W	Current Source Control Register	0x0000_0000
ANA_LDOSEL	ANA_BA+0x20	R/W	LDO Voltage Select Register	0x0000_0000
ANA_LDOPD	ANA_BA+0x24	R/W	LDO Power Down Register	0x0000_0001
ANA_MICBSEL	ANA_BA+0x28	R/W	Microphone Bias Select Register	0x0000_0000
ANA_MICBEN	ANA_BA+0x2C	R/W	Microphone Bias Enable Register	0x0000_0000
ANA_MUXCTL	ANA_BA+0x50	R/W	Analog Multiplexer Control Register	0x0000_0000
ANA_PGACTL	ANA_BA+0x60	R/W	PGA Enable Register	0x0000_0000
ANA_SIGCTL	ANA_BA+0x64	R/W	Signal Path Control Register	0x0000_0000
ANA_PGAGAIN	ANA_BA+0x68	R/W	PGA Gain Select Register	0x0000_0010
ANA_TRIM	ANA_BA+0x84	R/W	Oscillator Trim Register	0x0000_XXXX
ANA_CAPSCTL	ANA_BA+0x8C	R/W	Capacitive Touch Sensing Control Register	0x0000_0000

Temperature Sensor Measurement

In addition, the multiplexer can route a PTC (positive temperature coefficient) current, PTAT current, to the ADC to perform temperature measurements. To configure the signal path to do temperature measurement, configure the ADC path as follows:

1) Enable the multiplexer, PGA, IPBOOST, and sigma-delta modulator. (See Section 7.4.9, Section 7.1).
2) Have the multiplexer select I_PTAT current as input and choose VBG (bandgap voltage) as reference (REFSEL).
3) Set the 6-bit ANA_PGAGAIN[5:0] gain value to hex 0x17 and choose 0dB gain setting for IPBOOST gain block.
4) The temperature can be inferred by the information given in Table 7-30 and equation below.

T (°C) = 27 + (ADC_VAL-0x42EA)/50. (Equation 7-1)

The settings corresponding to this configuration are:

ANA_SIGCTL=0x1E, ANA_PGACTL=0x07, ANA_MUXCTL=0x5000, ANA_PGAGAIN=0x17

Table 7-30 Temperature Sensor Measurement.

Parameter	Specification (Reference)				Test Condition
	Min.	Typ.	Max.	Unit	
Temperature Sensor Output		0x42EA		Code	At 27^{o} C
Temperature Sensor Delta Coefficient (number of bits per degree ^{o}C)**		50		LSB/^{o}C	Relative to 27^{o}C

**LSB is the least significant bit of a 16-bit ADC with a defined full-scale RMS input voltage of 0.77V

7.4.11 Oscillator Frequency Measurement and Control

The ISD9160 provides a functional unit that can be used to measure PCLK frequency given a reference frequency such as the 32.768kHz crystal or an I2S frame synchronization signal. This is simply a special purpose timer/counter as shown in Figure 7-16.

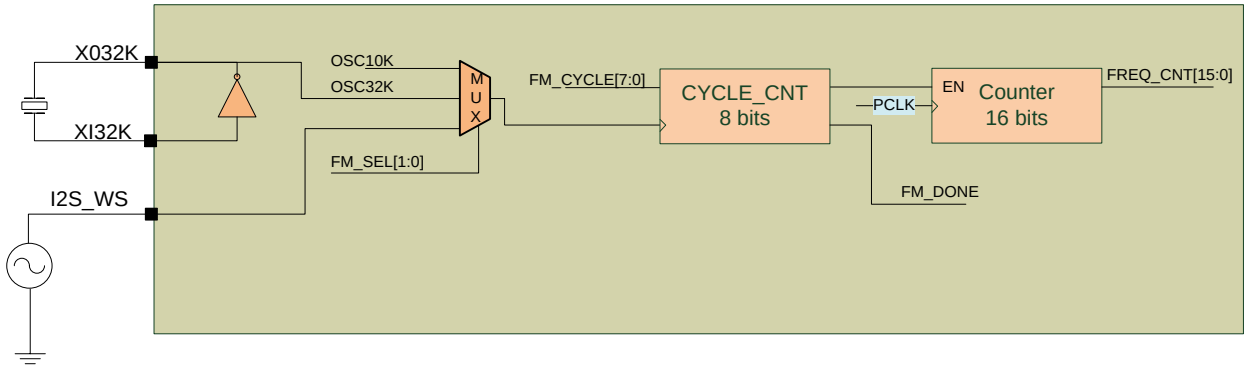

Figure 7-16 Oscillator Frequency Measurement Block Diagram

The block can be used to trim/measure the internal high frequency oscillator to the reference frequency of the 32.768kHz oscillator or an external reference frequency fed in on the I2S frame sync input. With this the internal clock can be set at arbitrary frequencies, other than those trimmed at manufacturing, or can be periodically trimmed to account for temperature variation. The block can also be used to measure the 16kHz oscillator frequency relative to the internal master oscillator.

An example of use would be to measure the internal oscillator with reference to the 32768Hz crystal. To do this:

```
 CLK_APBCLK0.ANACKEN   = 1;              /* Turn on analog peripheral clock */
ANA_FQMMCTL.CLKSEL = 1;   // Select reference source as 32kHz XTAL input
ANA_FQMMCTL.CYCLESEL = DRVOSC_NUM_CYCLES-1;
ANA_FQMMCTL.FQMMEN = TRUE;
while( (ANA_FQMMCTL.MMSTS != 1) && (Timeout++ < 0x100000));
        if(         Timeout >= 0x100000)
                    return(E_DRVOSC_MEAS_TIMEOUT);
Freq = ANA_FQMMCNT;
ANA_FQMMCTL.FQMMEN = FALSE;
Freq = Freq*32768 /DRVOSC_NUM_CYCLES;
```

To adjust the oscillator the user can write to the SYS_IRCTCTL register (see Table 5-11). In addition, to obtain frequencies in between SYS_IRCTCTL trim settings a SUPERFINE function is available. The SUPERFINE function dithers the trim setting between the current setting and FINE trim settings above and below the current setting. An example of how the SUPERFINE trim register can adjust the measured oscillator frequency is shown in the figure below

[24:22]	**MINGAIN**	**ALC Minimum Gain** 0 = -12 dB 1 = -6 dB 2 = 0 dB 3 = 6 dB 4 = 12 dB 5 = 18 dB 6 = 24 dB 7 = 30 dB
[21]	**ZCEN**	**ALC Zero Crossing** 0 = zero crossing disabled 1 = zero crossing enabled
[20:17]	**HOLDTIME**	**ALC Hold Time** (Value: 0~10). Hold Time aaa (2^HOLDTIME) ms
[16:13]	**TARGETLV**	**ALC Target Level** 0 = -28.5 dB 1 = -27 dB 2 = -25.5 dB 3 = -24 dB 4 = -22.5 dB 5 = -21 dB 6 = -19.5 dB 7 = -18 dB 8 = -16.5 dB 9 = -15 dB 10 = -13.5 dB 11 = -12 dB 12 = -10.5 dB 13 = -9 dB 14 = -7.5 dB 15 = -6 dB
[12]	**MODESEL**	**ALC Mode** 0 = ALC normal operation mode 1 = ALC limiter mode
[11:8]	**DECAYSEL**	**ALC Decay Time** (Value: 0~10) When MODESEL aaa 0, Range: 125us to 128ms When MODESEL aaa 1, Range: 31us to 32ms (time doubles with every step)

9.4.5 Specification of Brownout Detector

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation voltage	-	2.2	-	5.5	V
Quiescent current	AVDD=5.5V	-	-	125	μA
Temperature	-	-40	25	85	℃
Brown-out voltage	BOV_VL[1:0]=11		2.15		V
	BOV_VL [1:0]=10		2.25		V
	BOV_VL [1:0]=01		2.45		V
	BOV_VL [1:0]=00		2.55		V
	BOV_VL [2:0]=011		2.7		V
	BOV_VL[2:0]=010		2.8		V
	BOV_VL [2:0]=001		3.0		V
	BOV_VL [2:0]=000		4.55		V
Hysteresis	-				V

9.4.6 Specification of Power-On Reset (VCCD)

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Temperature	-	-40	25	85	℃
Reset voltage	VCC ramping down	-	1.0	-	V
Reset Release voltage	VCC ramping up		1.5		V
Quiescent current	Vin>reset voltage	-	60	-	nA

9.5.1.4 *Watchdog Reset Timing*