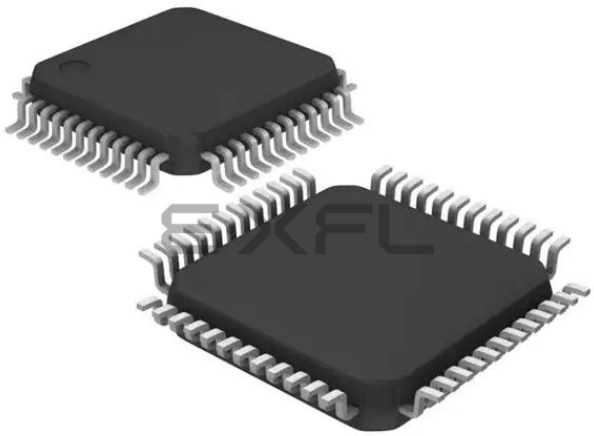

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Product Status	Active
Applications	Audio Record/Playback
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Program Memory Type	FLASH (145kB)
Controller Series	-
RAM Size	12K x 8
Interface	I²C, IrDA, LIN, SPI, UART/USART
Number of I/O	8
Voltage - Supply	2.5V ~ 5.5V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/isd9160fi

IRQ16 ~ IRQ19 Interrupt Priority Register （NVIC_IPR4）

Register	Offset	R/W	Description	Reset Value
NVIC_IPR4	SCS_BA+0x410	R/W	IRQ16 ~ IRQ19 Priority Control Register	0x0000_0000

31	30	29	28	27	26	25	24
PRI_19		Reserved					
23	22	21	20	19	18	17	16
PRI_18		Reserved					
15	14	13	12	11	10	9	8
PRI_17		Reserved					
7	6	5	4	3	2	1	0
PRI_16		Reserved					

Table 5-26 Interrupt Priority Register (IPR4, address 0xE000_E410)

Bits	Description	
[31:30]	PRI_19	**Priority of IRQ19** “0” denotes the highest priority and “3” denotes lowest priority
[23:22]	PRI_18	**Priority of IRQ18** “0” denotes the highest priority and “3” denotes lowest priority
[15:14]	PRI_17	**Priority of IRQ17** “0” denotes the highest priority and “3” denotes lowest priority
[7:6]	PRI_16	**Priority of IRQ16** “0” denotes the highest priority and “3” denotes lowest priority

IRQ26(PDMA) Interrupt Source Identify Register (IRQ26_SRC)

Register	Offset	R/W	Description	Reset Value
IRQ26_SRC	INT_BA+0x68	R	IRQ26 (PDMA) Interrupt Source Identity Register	0xXXXX_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved					INT_SRC[2:0]		

Bits	Description	
[2:0]	INT_SRC	**Interrupt Source Identity** Bit2: 0 Bit1: 0 Bit0: PDMA_INT

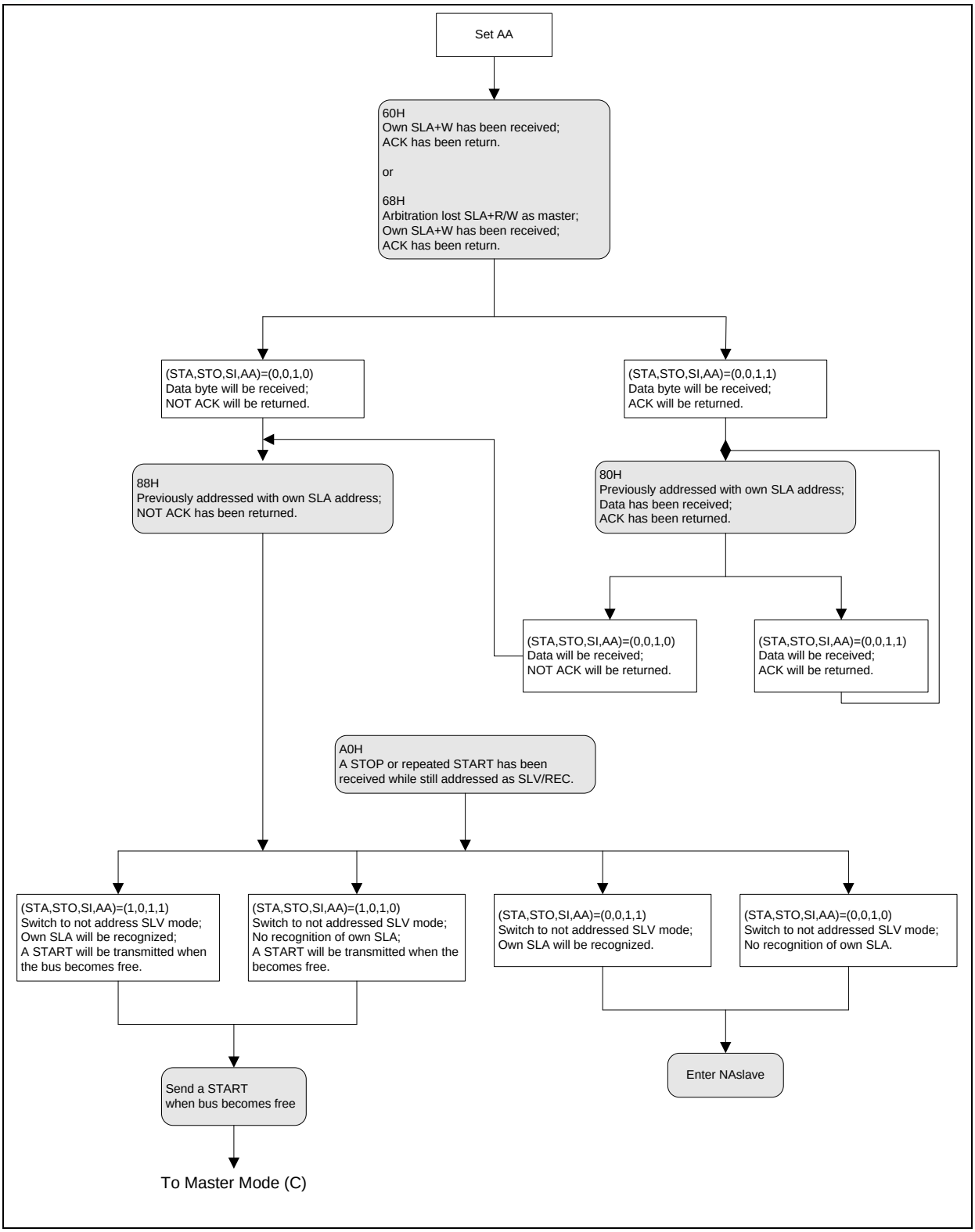

Figure 5-22 Slave Receiver Mode

PWM Interrupt Enable Register (PWM_INTEN)

Register	Offset	R/W	Description	Reset Value
PWM_INTEN	PWM_BA+0x040	R/W	PWM Interrupt Enable Register	0x0000_0000

7	6	5	4	3	2	1	0
Reserved						**PIEN1**	**PIEN0**

Table 5-63 PWM Interrupt Enable Register (PWM_INTEN, address 0x4004_0040).

Bits	Description	
[1]	**PIEN1**	**PWM Timer 1 Interrupt Enable** 0 = Disable 1 = Enable
[0]	**PIEN0**	**PWM Timer 0 Interrupt Enable** 0 = Disable 1 = Enable

RTC Time-Tick Register (RTC_TICK)

Register	Offset	R/W	Description	Reset Value
RTC_TICK	RTC_BA+0x030	R/W	RTC Time Tick Register	0x0000_0000

7	6	5	4	3	2	1	0
Reserved				TWKEN	TICKSEL		

Table 5-83 RTC Time-Tick Register (RTC_TICK, address 0x4000_8030).

Bits	Description	
[3]	TWKEN	**RTC Timer Wakeup CPU Function Enable Bit** If TWKEN is set before CPU is in power-down mode, when a RTC Time-Tick or Alarm Match occurs, CPU will wake up. 0= Disable Wakeup CPU function. 1= Enable the Wakeup function.
[2:0]	TICKSEL	**Time Tick Register** The RTC time tick period for Periodic Time-Tick Interrupt request. Time Tick (second) : 1 / (2^TICKSEL) Note: This register can be read back after the RTC is active.

LSB First

The SPI_CTL.LSB bit defines the **bit** order of data transmission. If LSB=0 then MSB of transfer word is sent first in time. If LSB=1 then LSB of transfer word is sent first in time.

Transmit Edge

The SPI_CTL.TXNEG bit determines whether transmit data is changed on the positive or negative edge of the SPI_SCLK serial clock. If TXNEG=0 then transmitted data will change state on the rising edge of SPI_SCLK. If TXNEG=1 then transmitted data will change state on the falling edge of SPI_SCLK.

Receive Edge

The SPI_CTL.RXNET bit determines whether data is received at either the negative edge or positive edge of serial clock SPI_SCLK. If RXNET=1 then data is clocked in on the falling edge of SPI_SCLK. If RXNET=0 data is clocked in on the rising edge of SPI_SCLK. Note that RXNET should be the inverse of TXNEG for standard SPI operation.

Word Sleep Suspend

The bit field SPI_CTL.SUSPITV provides a configurable suspend interval of SUSPITV+2 serial clock periods between successive word transfers in master mode. The suspend interval is from the last falling clock edge of the preceding transfer word to the first rising clock edge of the following transfer word if CLKPOL = 0. If CLKPOL = 1, the interval is from the rising clock edge of the preceding transfer word to the falling clock edge of the following transfer word. The default value of SUSPITV is 0x0 (2 serial clock cycles). Word Sleep only occurs when TXCNT=1. For TXCNT=0, this parameter will determine a Byte Sleep condition if the BYTEITV bit is set.

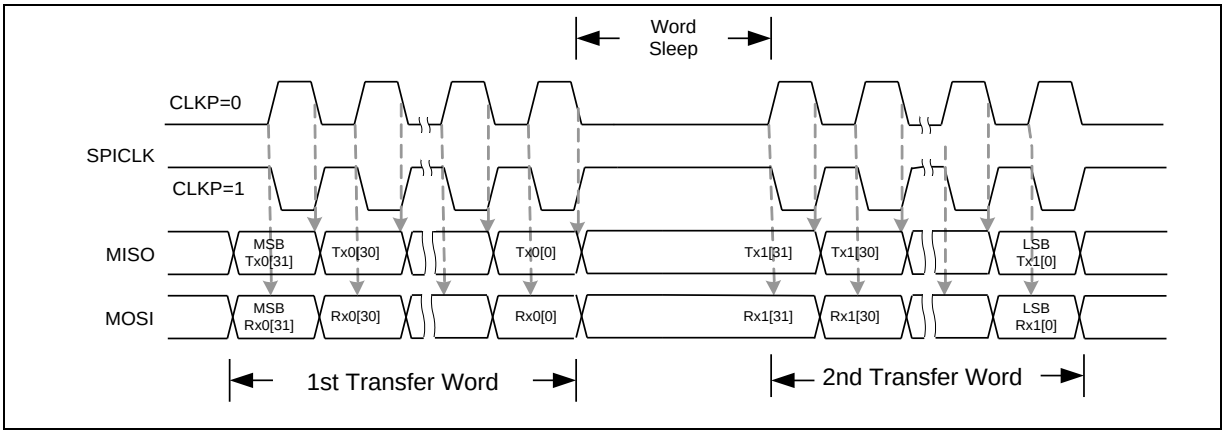

Figure 5-38 Word Sleep Suspend Mode

words. Now consider if this data were to be sent to the SPI port; the user could:

1. Set DWIDTH=8 and send data byte-by-byte SPI_TX0 = ucSPI_DATA[i++]
2. Set DWIDTH=32 and send word-by-word SPI_TX0 = uiSPI_DATA[i++]

Both of these would result in the byte stream {0x01, 0x02, 0x03, 0x04, 0x05, 0x06, 0x07, 0x08} being sent.

It would be common that a byte array of data is constructed but user, for efficiency, wishes to transfer data to SPI via word transfers. Consider the situation of Figure 5-41 where a int pointer points to the byte data array.

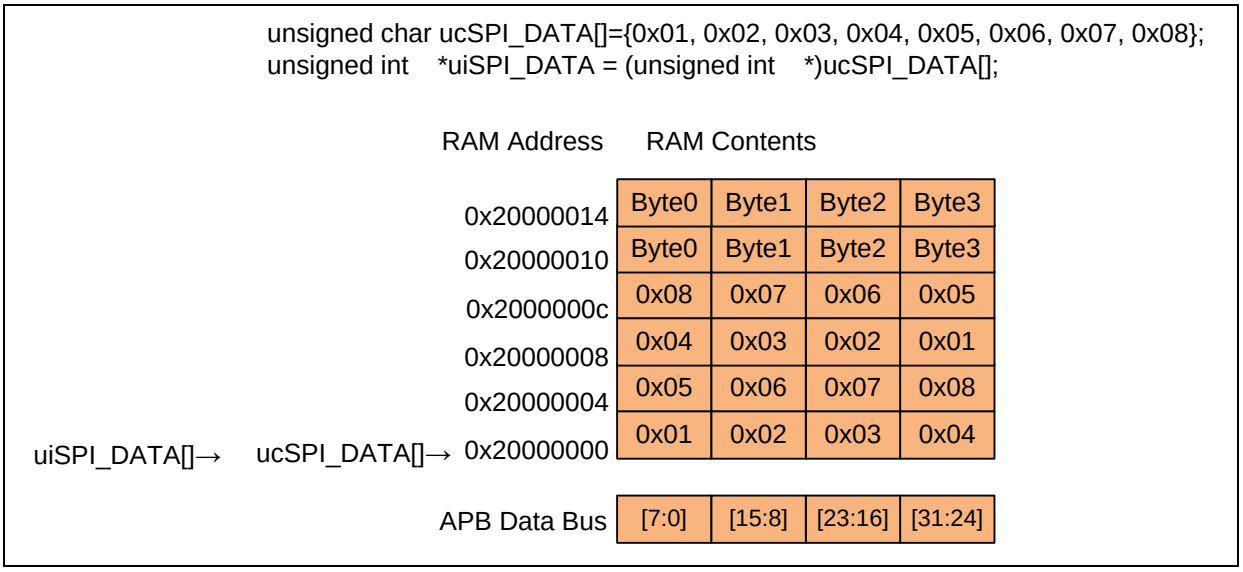

Figure 5-41 Byte Order in Memory

Now if we set DWIDTH=32 and sent word-by-word SPI_TX0 = uiSPI_DATA[i++], the order transmitted would be {0x04, 0x03, 0x02, 0x01, 0x08, 0x07, 0x06, 0x05}. However if we set REORDER=1, we would reverse this order to the desired stream: {0x01, 0x02, 0x03, 0x04, 0x05, 0x06, 0x07, 0x08}.

SPI Divider Register (SPI_CLKDIV)

Register	Offset	R/W	Description	Reset Value
SPI_CLKDIV	SPI0_BA + 0x04	R/W	Clock Divider Register (Master Only)	0x0000_0000

31	30	29	28	27	26	25	24
DIVIDER1[15:8]							
23	22	21	20	19	18	17	16
DIVIDER1[7:0]							
15	14	13	12	11	10	9	8
DIVIDER0[15:8]							
7	6	5	4	3	2	1	0
DIVIDER0[7:0]							

Table 5-85 SPI Clock Divider Register (SPI_CLKDIV, address 0x4003_0004)

Bits	Description	
[31:16]	DIVIDER1	**Clock Divider 2 Register** (master only) The value in this field is the 2nd frequency divider of the system clock, PCLK, to generate the serial clock on the output SCLK. The desired frequency is obtained according to the following equation: Fsclk aaa Fpclk / ((DIVIDER1+1) * 2)
[15:0]	DIVIDER0	**Clock Divider Register** (master only) The value in this field is the frequency division of the system clock, PCLK, to generate the serial clock on the output SCLK. The desired frequency is obtained according to the following equation: Fsclk aaa Fpclk / ((DIVIDER0+1) * 2) In slave mode, the period of SPI clock driven by a master shall satisfy Fsclk < aaa (Fpclk / 5) In other words, the maximum frequency of SCLK clock is one fifth of the SPI peripheral clock.

5.10.4 Timer Controller Register Map

R: read only, **W**: write only, **R/W**: both read and write

Register	Offset	R/W	Description	Reset Value
TMR Base Address: **TMRn_BA=0x4001_0000+(0x20*n)** **n=0,1**				
TIMERx_CTL	TMRn_BA+0x00	R/W	Timer Control and Status Register	0x0000_0005
TIMERx_CMP	TMRn_BA+0x04	R/W	Timer Compare Register	0x0000_0000
TIMERx_INTSTS	TMRn_BA+0x08	R/W	Timer Interrupt Status Register	0x0000_0000
TIMERx_CNT	TMRn_BA+0x0C	R/W	Timer Data Register	0x0000_0000

5.12.2 Features of UART controller

- UART supports 8 byte FIFO for receive and transmit data payloads.
- PDMA access support.
- Auto flow control function (/CTS, /RTS) supported.
- Programmable baud-rate generator.
- Fully programmable serial-interface characteristics:
  - 5-, 6-, 7-, or 8-bit character.
  - Even, odd, or no-parity bit generation and detection.
  - 1-, 1&1/2, or 2-stop bit generation.
  - Baud rate generation.
  - False start bit detection.
- IrDA SIR Function.
- LIN master mode.

[8]	**LINIEN**	**LIN RX Break Field Detected Interrupt Enable** 0 = Mask off Lin bus Rx break field interrupt. 1 = Enable Lin bus Rx break field interrupt.
[7:6]	Reserved	Reserved
[5]	**BUFERRIEN**	**Buffer Error Interrupt Enable** 0 = Mask off BUFERRINT 1 = Enable IBUFERRINT
[4]	**RXTOIEN**	**Receive Time out Interrupt Enable** 0 = Mask off RXTOINT 1 = Enable RXTOINT
[3]	**MODEMIEN**	**Modem Status Interrupt Enable** 0 = Mask off MODEMINT 1 = Enable MODEMINT
[2]	**RLSIEN**	**Receive Line Status Interrupt Enable** 0 = Mask off RLSINT 1 = Enable RLSINT
[1]	**THREIEN**	**Transmit FIFO Register Empty Interrupt Enable** 0 = Mask off THERINT 1 = Enable THERINT
[0]	**RDAIEN**	**Receive Data Available Interrupt Enable**. 0 = Mask off RDAINT 1 = Enable RDAINT

5.13.5 FIFO operation

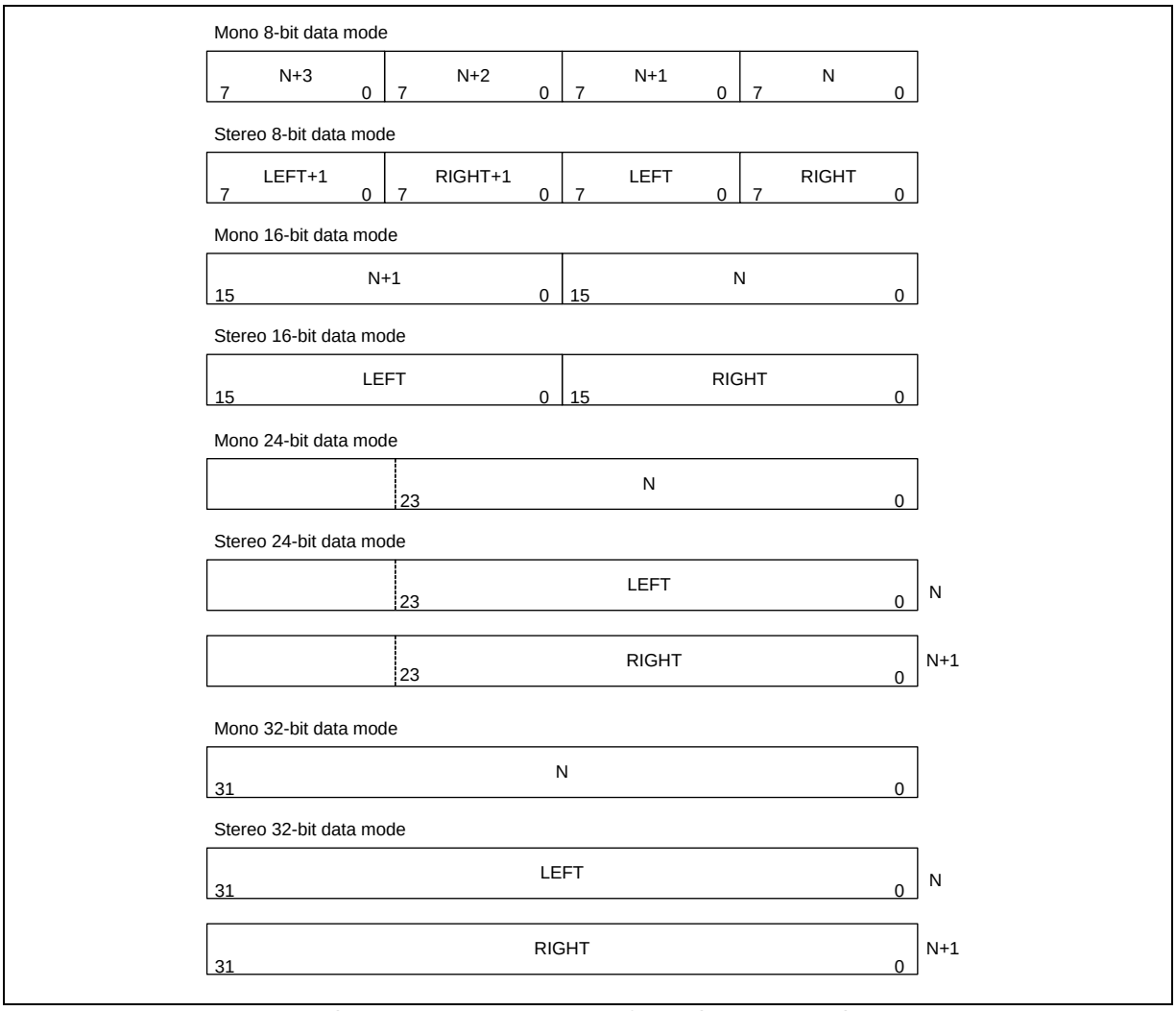

Figure 5-63 FIFO contents for various I2S modes

5.13.6 I2S Control Register Map

R: read only, **W**: write only, **R/W**: both read and write

Register	Offset	R/W	Description	Reset Value
I2S Base Address: **I2S_BA = 0x400A_0000**				
I2S_CTL	I2S_BA + 0x00	R/W	I2S Control Register	0x0000_0000
I2S_CLKDIV	I2S_BA + 0x04	R/W	I2S Clock Divider Register	0x0000_0000
I2S_IEN	I2S_BA + 0x08	R/W	I2S Interrupt Enable Register	0x0000_0000
I2S_STATUS	I2S_BA + 0x0C	R/W	I2S Status Register	0x0014_1000
I2S_TX	I2S_BA + 0x10	W	I2S Transmit FIFO Register	0x0000_0000
I2S_RX	I2S_BA + 0x14	R	I2S Receive FIFO Register	0x0000_0000

I2S Interrupt Enable Register (I2S_IEN)

Register	Offset	R/W	Description	Reset Value
I2S_IEN	I2S_BA + 0x08	R/W	I2S Interrupt Enable Register	0x0000_0000

15	14	13	12	11	10	9	8
Reserved			LZCIEN	RZCIEN	TXTHIEN	TXOVIEN	TXUDIEN
7	6	5	4	3	2	1	0
Reserved					RXTHIEN	RXOVIEN	RXUDIEN

Table 5-116 I2S Interrupt Enable Register (I2S_IEN, address 0x400A_0008)

Bits	Description	
[12]	LZCIEN	**Left Channel Zero Cross Interrupt Enable** Interrupt will occur if this bit is set to 1 and left channel has zero cross event 0 = Disable interrupt 1 = Enable interrupt
[11]	RZCIEN	**Right Channel Zero Cross Interrupt Enable** Interrupt will occur if this bit is set to 1 and right channel has zero cross event 0 = Disable interrupt 1 = Enable interrupt
[10]	TXTHIEN	**Transmit FIFO Threshold Level Interrupt Enable** Interrupt occurs if this bit is set to 1 and data words in transmit FIFO is less than TXTH[2:0]. 0 = Disable interrupt 1 = Enable interrupt
[9]	TXOVIEN	**Transmit FIFO Overflow Interrupt Enable** Interrupt occurs if this bit is set to 1 and transmit FIFO overflow flag is set to 1 0 = Disable interrupt 1 = Enable interrupt
[8]	TXUDIEN	**Transmit FIFO Underflow Interrupt Enable** Interrupt occur if this bit is set to 1 and transmit FIFO underflow flag is set to 1. 0 = Disable interrupt 1 = Enable interrupt
[2]	RXTHIEN	**Receive FIFO Threshold Level Interrupt** Interrupt occurs if this bit is set to 1 and data words in receive FIFO is greater than or equal to RXTH[2:0]. 0 = Disable interrupt 1 = Enable interrupt

CRC Output

Register	Offset	R/W	Description	Reset Value
CRC_CHECKSUM	CRC_BA+0x08	R	CRC Output Register	0x0000_FFFF

Table 5-122 CRC Output Register

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
CHECKSUM[15:8]							
7	6	5	4	3	2	1	0
CHECKSUM[7:0]							

Bits	Description	
[15:0]	CHECKSUM	**CRC Output** The result of CRC computation. The result is valid four clock cycles after last CRC_DAT input data is written to CRC generator.

PDMA Transfer Source Address Register (PDMA_DSCTn_ENDSA)(n=0~3)

Register	Offset	R/W	Description	Reset Value
PDMA_DSCT0_ENDSA	PDMA_BA+0x04	R/W	PDMA Transfer Source Address Register of Channel 0	0x0000_0000
PDMA_DSCT1_ENDSA	PDMA_BA+0x104	R/W	PDMA Transfer Source Address Register of Channel 1	0x0000_0000
PDMA_DSCT2_ENDSA	PDMA_BA+0x204	R/W	PDMA Transfer Source Address Register of Channel 2	0x0000_0000
PDMA_DSCT3_ENDSA	PDMA_BA+0x304	R/W	PDMA Transfer Source Address Register of Channel 3	0x0000_0000

Table 5-124 PDMA Source Address Register (PDMA_DSCTn_ENDSA, address 0x5000_8004 + *n**0x100)

Bits	Description	
[31:0]	**ENDSA**	**PDMA Transfer Source Address Register** This register holds the initial Source Address of PDMA transfer. **Note:** The source address must be word aligned.

PDMA Current Byte Count Register (PDMA_CURBCCHn) (n=0~3)

Register	Offset	R/W	Description	Reset Value
PDMA_CURBCCH0	PDMA_BA+0x1C	R	PDMA Current Byte Count Register of Channel 0	0x0000_0000
PDMA_CURBCCH1	PDMA_BA+0x11C	R	PDMA Current Byte Count Register of Channel 1	0x0000_0000
PDMA_CURBCCH2	PDMA_BA+0x21C	R	PDMA Current Byte Count Register of Channel 2	0x0000_0000
PDMA_CURBCCH3	PDMA_BA+0x31C	R	PDMA Current Byte Count Register of Channel 3	0x0000_0000

Table 5-130 PDMA Current Byte Count Register (PDMA_CURBCCHn, address 0x5000_801C + *n**0x100)

Bits	Description	
[31:16]	Reserved	Reserved
[15:0]	**CURBC**	**PDMA Current Byte Count Register (Read Only)** This field indicates the current remaining byte count of PDMA transfer. This register is initialized with PDMA_TXBCCHn register when PDMA is triggered or when a wraparound occurs

PDMA Interrupt Status Register (PDMA_CHnIF) (n=0~3)

Register	Offset	R/W	Description	Reset Value
PDMA_CH0IF	PDMA_BA+0x24	R/W	PDMA Interrupt Status Register of Channel 0	0x0000_0000
PDMA_CH1IF	PDMA_BA+0x124	R/W	PDMA Interrupt Status Register of Channel 1	0x0000_0000
PDMA_CH2IF	PDMA_BA+0x224	R/W	PDMA Interrupt Status Register of Channel 2	0x0000_0000
PDMA_CH3IF	PDMA_BA+0x324	R/W	PDMA Interrupt Status Register of Channel 3	0x0000_0000

31	30	29	28	27	26	25	24
INTSTS	Reserved						
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved				WAIF			
7	6	5	4	3	2	1	0
Reserved						TXOKIF	TXABTIF

Table 5-132 PDMA Interrupt Enable Status Register (PDMA_CHnIF, address 0x5000_8024 + *n**0x100)

Bits	Description	
[31]	**INTSTS**	**Interrupt Pin Status (Read Only)** This bit is the Interrupt pin status of PDMA channel.
[30:12]	Reserved	Reserved
[11:8]	**WAIF**	**Wrap Around Transfer Byte Count Interrupt Flag** These flags are set whenever the conditions for a wraparound interrupt (complete or half complete) are met. They are cleared by writing one to the bits. 0001 aaa Current transfer finished flag (CURBC aaaaaa 0). 0100 aaa Current transfer half complete flag (CURBC aaaaaa BYTECNT/2).
[1]	**TXOKIF**	**Block Transfer Done Interrupt Flag** This bit indicates that PDMA block transfer complete interrupt has been generated. It is cleared by writing 1 to the bit. 0 = Transfer ongoing or Idle. 1 = Transfer Complete.

Operating Current Normal Run Mode @ 12.288Mhz	I_{DD13}		12.5		mA	V_{DD} = 5.5V, Enable all IP.
	I_{DD14}		10.3		mA	V_{DD} = 5.5V, Disable all IP.
	I_{DD15}		11.4		mA	V_{DD} = 3V, Enable all IP.
	I_{DD16}		9		mA	V_{DD} = 3V, Disable all IP.
Operating Current Normal Run Mode @ 4.9152Mhz	I_{DD9}		9.7		mA	V_{DD} = 5.5V, Enable all IP.
	I_{DD10}		8.1		mA	V_{DD} = 5.5V, Disable all IP.
	I_{DD11}		8.7		mA	V_{DD} = 3V, Enable all IP.
	I_{DD12}		7.0		mA	V_{DD} = 3V, Disable all IP.
Operating Current Sleep Mode	I_{IDLE1}		10		mA	V_{DD}= 5.5V
	I_{IDLE1}		9		mA	V_{DD}= 3.3V
Operating Current Deep Sleep Mode	I_{IDLE1}		10		mA	V_{DD}=5.5V
	I_{IDLE1}		8		mA	V_{DD}= 3.3V
Standby Power down mode(SPD)	I_{IDLE1}		3		uA	V_{DD}=3.3V 32K running with RTC
	I_{IDLE1}		1		uA	V_{DD}= 3.3V 16K running
Operating Current Deep Power down mode(DPD)	I_{IDLE1}		500		nA	V_{DD}=3.3V Wakeup with16K
	I_{IDLE1}				nA	V_{DD}= 3.3V wakeup with wakeup pin

9.5.1.4 *Watchdog Reset Timing*