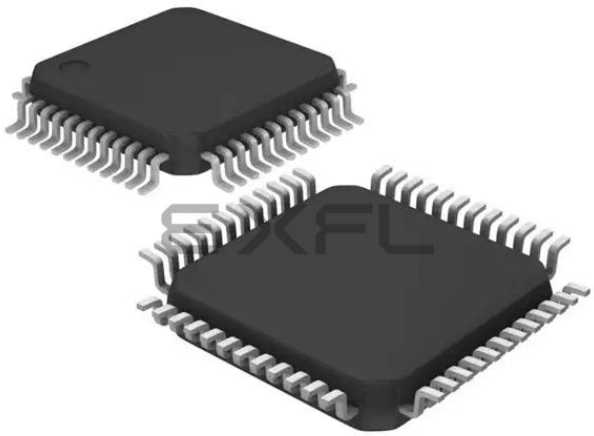

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Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Audio Record/Playback
Core Processor	ARM® Cortex®-M0
Program Memory Type	FLASH (145kB)
Controller Series	-
RAM Size	12K x 8
Interface	I²C, IrDA, LIN, SPI, UART/USART
Number of I/O	8
Voltage - Supply	2.5V ~ 5.5V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/isd9160vfi

- Single step and vector catch capabilities.

- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory.
  - Single 32-bit slave port that supports the DAP (Debug Access Port).

5.2 System Manager

5.2.1 Overview

The following functions are included in system manager section

- System Memory Map
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System management registers for product ID
- System management registers for chip and module functional reset and multi-function pin control
- Brown-Out and chip miscellaneous Control Register
- Combined peripheral interrupt source identify

5.2.2 System Reset

The system reset includes one of the list below event occurs. For these reset event flags can be read by SYS_RSTSTS register.

- The Power-On Reset
- The low level on the RESETN pin
- Watchdog Time Out Reset
- Low Voltage Reset
- Cortex-M0 MCU Reset
- PMU Reset – for details of wakeup events, also examine CLK_PWRCTL register.
- SWD Debug interface.

A power-on reset (POR) will occur if the main external supply rail ramps from 0V or the voltage of the main supply drops below reset threshold. A low voltage reset monitors the regulated core logic (1.8V) supply and will assert if the voltage on this rail drops below reliable logic threshold.

IP Reset Control Register2 (SYS_IPRST1)

Setting these bits “1” will generate an asynchronous reset signal to the corresponding peripheral block. The user needs to set bit to “0” to release block from the reset state.

Register	Offset	R/W	Description	Reset Value
SYS_IPRST1	SYS_BA+0x0C	R/W	IP Reset Control Resister2	0x0000_0000

31	30	29	28	27	26	25	24
Reserved	ANARST	I2S0RST	EADCRST	Reserved	Reserved	Reserved	Reserved
23	22	21	20	19	18	17	16
Reserved	ACMPRST	Reserved	PWM0RST	CRCRST	BIQRST	Reserved	UART0RST
15	14	13	12	11	10	9	8
Reserved	Reserved	DPWMRST	SPI0RST	Reserved	Reserved	Reserved	I2C0RST
7	6	5	4	3	2	1	0
TMR1RST	TMR0RST	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 5-4 IP Reset Control Register 2 (SYS_IPRST1 address 0x5000_000C) Bit Description.

Bits	Description	
[30]	ANARST	**Analog Block Control Reset** 0 = Normal Operation 1 = Reset
[29]	I2S0RST	**I2S Controller Reset** 0 = Normal Operation 1 = Reset
[28]	EADCRST	**ADC Controller Reset** 0 = Normal Operation 1 = Reset
[22]	ACMPRST	**Analog Comparator Reset** 0 = Normal Operation 1 = Reset
[20]	PWM0RST	**PWM10 controller Reset** 0 = Normal Operation 1 = Reset
[19]	CRCRST	**CRC Generation Block Reset** 0 = Normal Operation 1 = Reset

GPIO Alternative Function Control Register (SYS_GPA_MFP)

Each GPIO pin can take on multiple alternate functions depending on the setting of this register. Each pin has two bits of alternate function control. Set to 00 the pin is a standard GPIO pin whose attributes are defined by the GPIO control registers (See Section 0). Set to other values the pin is assigned to a peripheral as outlined in table below.

Register	Offset	R/W	Description	Reset Value
SYS_GPA_MFP	SYS_BA+0x38	R/W	GPIOA multiple function control register	0x0000_0000

31	30	29	28	27	26	25	24
PA15MFP		PA14MFP		PA13MFP		PA12MFP	
23	22	21	20	19	18	17	16
PA11MFP		PA10MFP		PA9MFP		PA8MFP	
15	14	13	12	11	10	9	8
PA7MFP		PA6MFP		PA5MFP		PA4MFP	
7	6	5	4	3	2	1	0
PA3MFP		PA2MFP		PA1MFP		PA0MFP	

Table 5-7 GPIOA Alternate Function Register (SYS_GPA_MFP address 0x5000_0038)

Bits	Description	
[31:30]	PA15MFP	**Alternate Function Setting For PA15MFP** 00 = GPIO 01 = TM1 10 = SDIN
[29:28]	PA14MFP	**Alternate Function Setting For PA14MFP** 00 = GPIO 01 = TM0 10 = SDCLK 11 = SDCLKn
[27:26]	PA13MFP	**Alternate Function Setting For PA13MFP** 00 = GPIO 01 = PWM1 10 = SPKM 11 = I2S_BCLK

IRQ0 ~ IRQ31 Clear-Pending Control Register （NVIC_ICPR）

Register	Offset	R/W	Description	Reset Value
NVIC_ICPR	SCS_BA+0x280	R/W	IRQ0 ~ IRQ31 Clear-Pending Control Register	0x0000_0000

Table 5-21 Interrupt Clear-Pending Control Register (ICPR, address 0xE000_E280)

Bits	Description	
[31:0]	**CLRPEND**	**Clear-Pending Control** Writing 1 to a bit to clear the pending state of associated interrupt under software control. Each bit represents an interrupt number from IRQ0 ~ IRQ31 (Vector number from 16 ~ 47). Writing 0 has no effect. The register reads back with the current pending state.

IRQ21(TALARM) Interrupt Source Identify Register (IRQ21_SRC)

Register	Offset	R/W	Description	Reset Value
IRQ21_SRC	INT_BA+0x54	R	IRQ21 (TALARM) Interrupt Source Identity Register	0xXXXX_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved					INT_SRC[2:0]		

Bits	Description	
[2:0]	INT_SRC	**Interrupt Source Identity** Bit2: 0 Bit1: 0 Bit0: TALARM_INT

during development it is recommended that some checks are placed in the boot sequence to prevent device going to power down. A register bit, CLK_DBGPD.DISPDREQ is included for this purpose that will disable power down features. A check such as:

```
void Reset_Handler(void){
/*  check ICECLKST and ICEDATST to disable power down to the chip */
      if ( CLK_DBGPD.ICECLKST == 0 &&  CLK_DBGPD.ICEDATST == 0)
            CLK_DBGPD.DISPDREQ = 1;
      __main();
}
```

Can check the SWD pin state on boot and prevent power down from occurring.

5.3.4.2 *Level1: Standby Power Down (SPD) mode.*

Standby Power Down mode is the lowest power state that some logic operation can be performed. In this mode power is removed from the majority of the core logic, including the Cortex-M0 and main RAM. A low power standby reference is enabled however that supplies power to a subset of logic including the IO ring, GPIO control, RTC module, 32kHz Crystal Oscillator, Brownout Detector and a 256Byte Standby RAM.

In Standby mode there are three ways to wake up the device:

1. An interrupt from the GPIO block (exclude GPB0 & GPB1), for instance a pin transition.
2. An interrupt from the RTC module, for instance an alarm or timer event.
3. A power cycle of main chip supply triggering a POR event.

When a wake up event occurs the PMU will start the Cortex-M0 processor and execute the reset vector. Software can determine whether the device woke up from SPD by interrogating the register bit CLK_PWRSTSF.SPDF.

To enter the SPD state the user must set the register bit CLK_PWRCTL.PD then execute a WFI or WFE instruction. Note that when debug interface is active, device will not enter SPD. Also once device enters SPD the debug interface will be inactive.

5.3.4.3 *Level2: Deep Sleep mode.*

The Deep Sleep mode is the lowest power state where the Cortex-M0 and all logic state are preserved. In Deep Sleep mode the CLK48M oscillator is shutdown and a low speed oscillator is selected, if CLK32K is active this source is selected, if not then CLK16K is enabled and selected. All clocks to the Cortex-M0 core are gated eliminating dynamic power in the core. Clocks to peripheral are gated according to the CLK_SLEEP register, note however that HCLK is operating at a low frequency and CLK48M is not available. Deep Sleep mode is entered by setting System Control register bit 2: SCB->SCR |= (1UL << 2) and executing a WFI/WFE instruction. Software can determine whether the device woke up from Deep Sleep by interrogating the register bit CLK_PWRSTSF.DSF.

5.3.4.4 *Level3: Sleep mode.*

The Sleep mode gates all clocks to the Cortex-M0 eliminating dynamic power in the core. In addition, clocks to peripherals are gated according to the CLK_SLEEP register. The mode is entered by executing a WFI/WFE instruction and is released when an event occurs. Peripheral functions, including PDMA can be continued while in Sleep mode. Using this mode power consumption can be minimized while waiting for events such as a PDMA operation collecting data from the ADC, once PDMA has finished the core can be woken up to process the data.

5.3.5 Clock Control Register Map

R: read only, **W:** write only, **R/W:** both read and write

GPIO Port [A/B] Input Disable (Px_DINOFF)

Register	Offset	R/W	Description	Reset Value
PA_DINOFF	GPIO_BA+0x004	R/W	GPIO Port A Pin Digital Input Disable	0x0000_0000
PB_DINOFF	GPIO_BA+0x044	R/W	GPIO Port B Pin Digital Input Disable	0x0000_0000

Table 5-43 GPIO Input Disable Register

31	30	29	28	27	26	25	24
DINOFF[31:24]							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
DINOFF[23:16]							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved							

Bits	Description	
[n] **n=16,17..31**	**DINOFF**	**GPIOx Pin[n] OFF Digital Input Path Enable** 0 = Enable IO digital input path (Default) 1 = Disable IO digital input path (low leakage mode)
[15:0]	Reserved	Reserved

GPIO Port [A/B] Interrupt Enable Control (Px_INTEN)

Register	Offset	R/W	Description	Reset Value
PA_INTEN	GPIO_BA+0x01C	R/W	GPIO Port A Interrupt Enable	0x0000_0000
PB_INTEN	GPIO_BA+0x05C	R/W	GPIO Port B Interrupt Enable	0x0000_0000

Table 5-49 GPIO Interrupt Enable Control Register (Px_INTEN)

31	30	29	28	27	26	25	24
RHIEN[15:8]							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RHIEN[7:0]							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
FLIEN[15:8]							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FLIEN[7:0]							

Bits	Description	
[n+16] **n=0,1..15**	**RHIEN**	**Port [A/B] Interrupt Enable by Input Rising Edge or Input Level High** RHIEN[n] is used to enable the rising/high interrupt for each of the corresponding GPIO pins. It also enables the pin wakeup function. If the interrupt is configured in level trigger mode, a level “high” will generate an interrupt. If the interrupt is configured in edge trigger mode, a state change from “low-to-high” will generate an interrupt. GPB.0 and GPB.1 trigger individual IRQ vectors (IRQ2/IRQ3) while remaining GPIO trigger a single interrupt vector IRQ4. 0 = Disable GPIOx[n] for level-high or low-to-high interrupt. 1 = Enable GPIOx[n] for level-high or low-to-high interrupt
[n] **n=0,1..15**	**FLIEN**	**Port [A/B] Interrupt Enable by Input Falling Edge or Input Level Low** FLIEN[n] is used to enable the falling/low interrupt for each of the corresponding GPIO pins. It also enables the pin wakeup function. If the interrupt is configured in level trigger mode, a level “low” will generate an interrupt. If the interrupt is configured in edge trigger mode, a state change from “high-to-low” will generate an interrupt. GPB.0 and GPB.1 trigger individual IRQ vectors (IRQ2/IRQ3) while remaining GPIO trigger a single interrupt vector IRQ4. 0 = Disable GPIOx[n] for low-level or high-to-low interrupt 1 = Enable GPIOx[n] for low-level or high-to-low interrupt

- CMP < PERIOD: PWM low width= (PERIOD-CMP) unit[1]; PWM high width = (CMP+1) unit.
- CMP = 0: PWM low width = (PERIOD) unit; PWM high width = 1 unit

Note: 1. Unit = one PWM clock cycle.

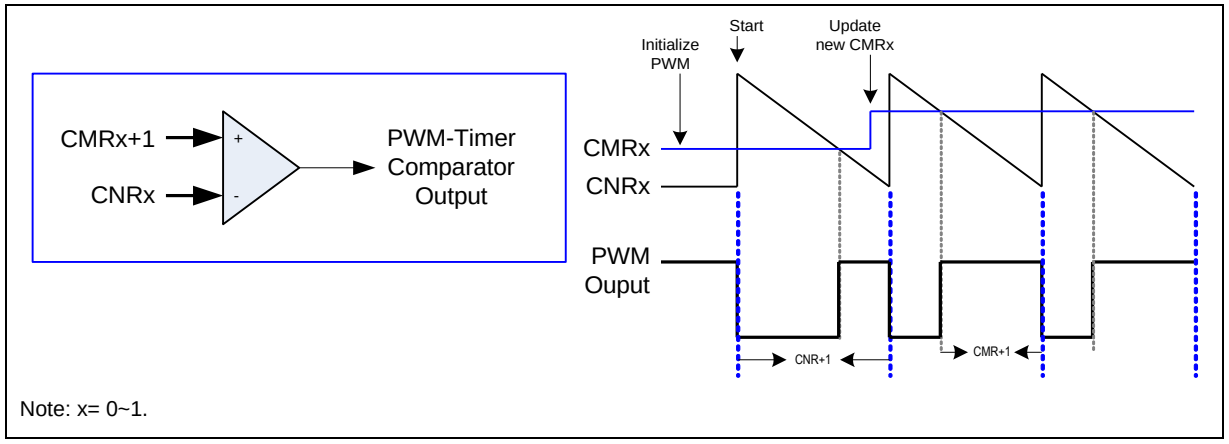


Figure 5-26 PWM Generation Timing

The procedure to operate the PWM generator is shown in Figure 5-27. First initialize the PWM settings. At the same time ensure that GPIO are configured to PWM function. Next step is to enable PWM channel. After this, if PERIOD or CMP register is written by software, it is double buffered until the next counter reload, at which time the registers are updated to new values.

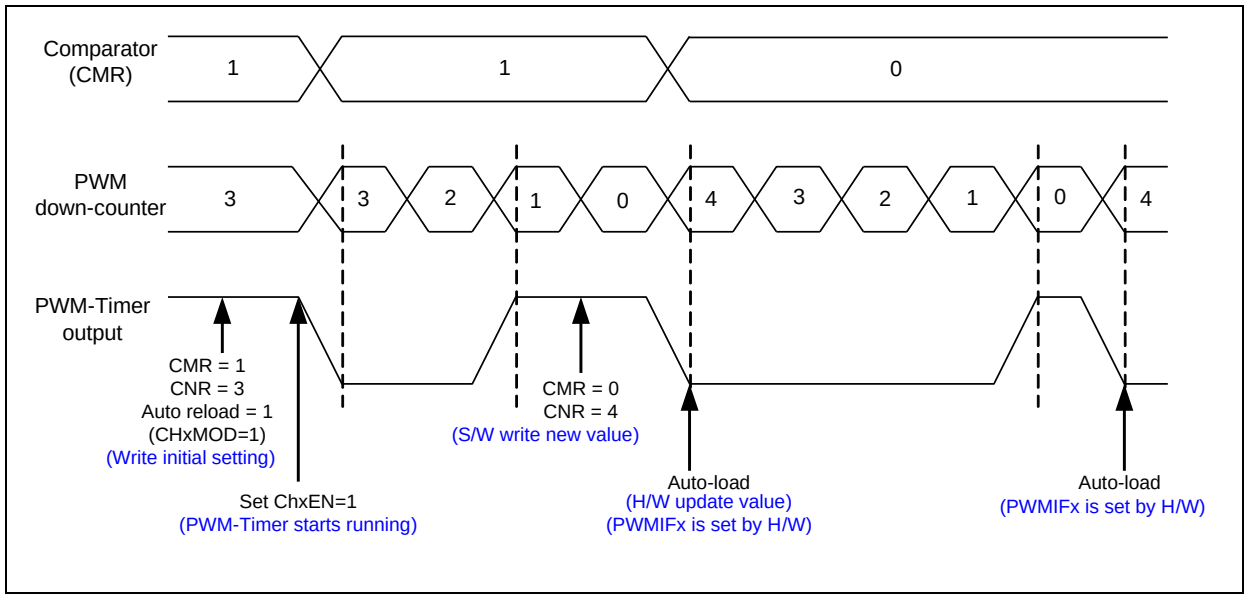
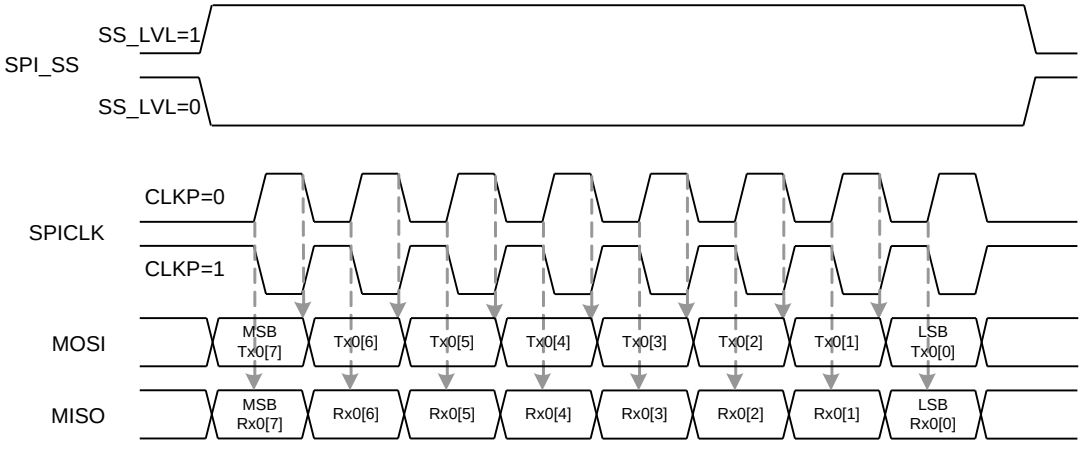


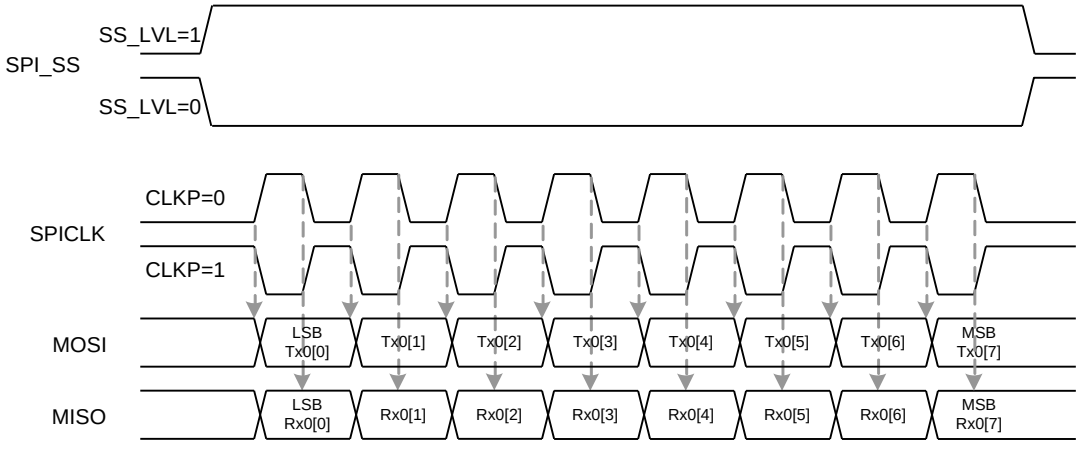
Figure 5-27 PWM-Timer Operation Timing



Master Mode: CNTRL[SLVAE]=0, CNTRL[LSB]=0, CNTRL[Tx_NUM]=0x0, CNTRL[Tx_BIT_LEN]=0x08

1. CNTRL[CLKP]=0, CNTRL[Tx_NEG]=1, CNTRL[Rx_NEG]=0 or
2. CNTRL[CLKP]=1, CNTRL[Tx_NEG]=0, CNTRL[Rx_NEG]=1

Figure 5-45 SPI Timing in Master Mode



Master Mode: CNTRL[SLVAE]=0, CNTRL[LSB]=1, CNTRL[Tx_NUM]=0x0, CNTRL[Tx_BIT_LEN]=0x08

1. CNTRL[CLKP]=0, CNTRL[Tx_NEG]=0, CNTRL[Rx_NEG]=1 or
2. CNTRL[CLKP]=1, CNTRL[Tx_NEG]=1, CNTRL[Rx_NEG]=0

Figure 5-46 SPI Timing in Master Mode (Alternate Phase of SPICLK)

5.12.2 Features of UART controller

- UART supports 8 byte FIFO for receive and transmit data payloads.
- PDMA access support.
- Auto flow control function (/CTS, /RTS) supported.
- Programmable baud-rate generator.
- Fully programmable serial-interface characteristics:
  - 5-, 6-, 7-, or 8-bit character.
  - Even, odd, or no-parity bit generation and detection.
  - 1-, 1&1/2, or 2-stop bit generation.
  - Baud rate generation.
  - False start bit detection.
- IrDA SIR Function.
- LIN master mode.

5.13.7 I2S Control Register Description

I2S Control Register (I2S_CTL)

Register	Offset	R/W	Description	Reset Value
I2S_CTL	I2S_BA + 0x00	R/W	I2S Control Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved	Reserved	RXPDMAEN	TXPDMAEN	RXCLR	TXCLR	LZCEN	RZCEN
15	14	13	12	11	10	9	8
MCLKEN	RXTH			TXTH			SLAVE
7	6	5	4	3	2	1	0
FORMAT	MONO	WDWIDTH		MUTE	RXEN	TXEN	I2SEN

Table 5-114 I2S Control Register (I2S_CTL, address 0x400A_0000)

Bits	Description	
[31:22]	Reserved	Reserved
[21]	**RXPDMAEN**	**Enable Receive DMA** When RX DMA is enabled, I2S requests DMA to transfer data from receive FIFO to SRAM if FIFO is not empty. 0 = Disable RX DMA 1 = Enable RX DMA
[20]	**TXPDMAEN**	**Enable Transmit DMA** When TX DMA is enables, I2S request DMA to transfer data from SRAM to transmit FIFO if FIFO is not full. 0 = Disable TX DMA 1 = Enable TX DMA
[19]	**RXCLR**	**Clear Receive FIFO** Write 1 to clear receiving FIFO, internal pointer is reset to FIFO start point, and RXTH returns to zero and receive FIFO becomes empty. This bit is cleared by hardware automatically when clear operation complete.
[18]	**TXCLR**	**Clear Transmit FIFO** Write 1 to clear transmitting FIFO, internal pointer is reset to FIFO start point, and TXTH returns to zero and transmit FIFO becomes empty. Data in transmit FIFO is not changed. This bit is cleared by hardware automatically when clear operation complete.

PDMA Internal Buffer Pointer Register (PDMA_INLBPCHn)(n=0~3)

Register	Offset	R/W	Description	Reset Value
PDMA_INLBPCH0	PDMA_BA+0x10	R	PDMA Internal Buffer Pointer Register of Channel 0	0xXXXX_XX00
PDMA_INLBPCH1	PDMA_BA+0x110	R	PDMA Internal Buffer Pointer Register of Channel 1	0xXXXX_XX00
PDMA_INLBPCH2	PDMA_BA+0x210	R	PDMA Internal Buffer Pointer Register of Channel 2	0xXXXX_XX00
PDMA_INLBPCH3	PDMA_BA+0x310	R	PDMA Internal Buffer Pointer Register of Channel 3	0xXXXX_XX00

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved				**BUFPTR**			

Table 5-127 PDMA Internal Buffer Point Register (PDMA_INLBPCHn, address 0x5000_8010 + *n**0x100)

Bits	Description	
[31:4]	Reserved	Reserved
[3:0]	**BUFPTR**	**PDMA Internal Buffer Pointer Register (Read Only)** A PDMA transaction consists of two stages, a read from the source address and a write to the destination address. Internally this data is buffered in a 32bit register. If transaction width between the read and write transactions are different, this register tracks which byte/half-word of the internal buffer is being processed by the current transaction.

[0]	DFENB	**Data Flash Enable Bar** When data flash is enabled, flash memory is partitioned between APROM and DATAF memory depending on the setting of data flash base address in Config1 register. If set to '0' then no DATAF partition exists. 0 = Enable data flash 1 = Disable data flash

A/D Compare Register 0(ADCMPR0)

Register	Offset	R/W	Description	Reset Value
ADC_CMP0	ADC_BA+0x18	R/W	ADC Comparator 0 Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CMPDAT[15:8]							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CMPDAT[7:0]							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved				**CMPMCNT**			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CMPFLAG	**Reserved**				**CMPCOND**	**ADCMPIE**	**CPMEN**

Table 7-11 ADC Comparator Control Registers (ADC_CMP0, address 0x400E_0018)

Bits	Description	
[31:16]	**CMPDAT**	**Comparison Data** 16 bit value to compare to FIFO output word.
[11:8]	**CMPMCNT**	**Compare Match Count** When the A/D FIFO result matches the compare condition defined by CMPCOND, the internal match counter will increase by 1. When the internal counter reaches the value to (CMPMCNT +1), the CMPFLAG bit will be set.
[7]	**CMPFLAG**	**Compare Flag** When the conversion result meets condition in ADCMPR0 this bit is set to 1. It is cleared by writing 1 to self.
[2]	**CMPCOND**	**Compare Condition** 0= Set the compare condition that result is less than CMPDAT 1= Set the compare condition that result is greater or equal to CMPDAT Note: When the internal counter reaches the value (CMPMCNT +1), the CMPFLAG bit will be set.
[1]	**ADCMPIE**	**Compare Interrupt Enable** 0 = Disable compare function interrupt. 1 = Enable compare function interrupt. If the compare function is enabled and the compare condition matches the setting of CMPCOND and CMPMCNT, CMPFLAG bit will be asserted, if ADCMPIE is set to 1, a compare interrupt request is generated.
[0]	**ADCMPEN**	**Compare Enable** 0 = Disable compare. 1 = Enable compare. Set this bit to 1 to enable compare CMPDAT with FIFO data output.

7.4.4 VMID Reference Voltage Generation

The analog path and blocks require a low noise, mid-rail, Voltage reference for operation, the VMID generation block provides this. Control of this block allows user to power down the block, select its power down condition and control over the reference impedance. The block consists of a switchable resistive divider connected to the device VMID pin. A 4.7µF capacitor should be placed on this pin and returned to analog ground (VSSA) as shown in Figure 7-7.

Before using the ADC, PGA or other analog blocks, the VMID reference needs to be enabled. A low impedance option allows fast charging of the external noise de-coupling capacitor, while a higher impedance options provides lower power consumption. A pulldown option allows the reference to be discharged when off.

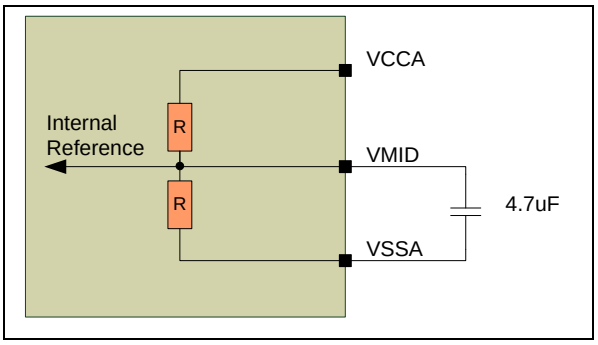


Figure 7-7 VMID Reference Generation

Microphone Bias Select (ANA_MICBSEL)

Register	Offset	R/W	Description	Reset Value
ANA_MICBSEL	ANA_BA+0x28	R/W	Microphone Bias Select Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved					REFSEL	VOLSEL	

Table 7-27 Microphone Bias Selection Register (ANA_MICBSEL, address 0x4008_0028).

Bits	Description	
[31:3]	**Reserved**	Reserved
[2]	**REFSEL**	**Select Reference Source For MICBIAS Generator** VMID provides superior noise performance for MICBIAS generation and should be used unless fixed voltage is absolutely necessary, then noise performance can be sacrificed and bandgap voltage used as reference. 0= VMID aaa VCCA/2 is reference source. 1= VBG (bandgap voltage reference) is reference source.
[1:0]	**VOLSEL**	**Select Microphone Bias Voltage** MICBMODE aaa 0 0: 90% VCCA 1: 65% VCCA 2: 75% VCCA 3: 50% VCCA MICBMODE aaa 1 0: 2.4V 1: 1.7V 2: 2.0V 3: 1.3V

7.4.9 Programmable Gain Amplifier

The ISD9160 provides a Programmable Gain Amplifier (PGA) as the front-end to the ADC to allow the adjustment of signal path gain. It is used in conjunction with the ALC block to provide automatic level control of incoming audio signals. Figure 7-13 shows the signal path diagram. The PGA provides a gain from -12dB to 35.25dB in increments of 0.75dB steps using a 6-bit control, ANA_PGAGAIN[5:0]. The gain is monotonically increasing with 0x00 for lowest gain (-12dB) and 0x3f for the maximum gain (35.25dB). The signal path is enabled by powering up the gain elements (PUPGA, PUBOOST). The PGA and IP BOOST blocks can be muted with the ANA_SIGCTL register. Input to the PGA can be either differential or single-ended on the PGA_INN input. The Analog MUX controls connection of the signal path to external pins. PGA input impedance varies based on the gain setting. Table 7-31 shows a table of input impedance for different gain setting.

The IP BOOST block can provide 0dB or 26dB of gain to provide a maximum gain of 61dB in the signal path. Front-end anti-alias filtering for the sigma-delta ADC is also provided by PGA/IP-BOOST blocks with an attenuation of -45dB at 6MHz frequency. The signal path defaults to have VCCA/2 as the reference voltage.

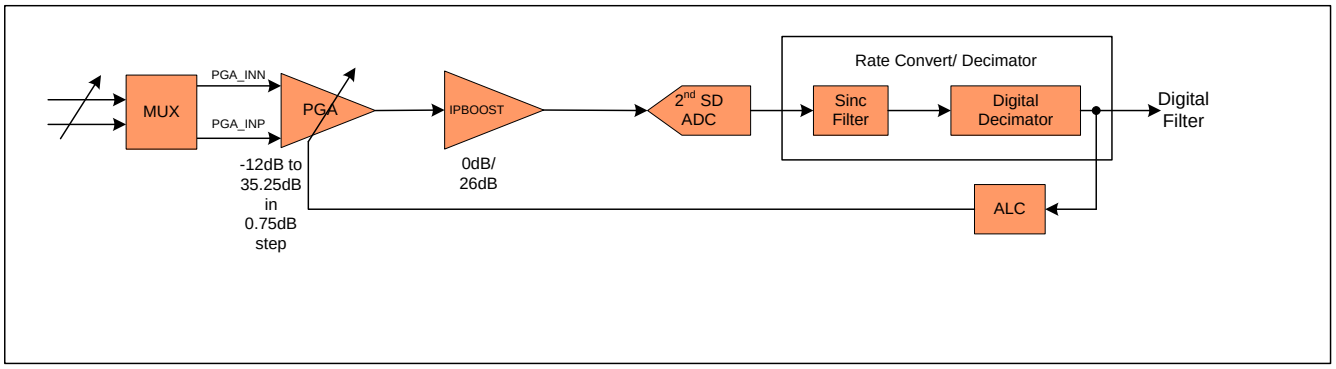


Figure 7-13 PGA Signal Path Block Diagram

Frequency Measurement Count (ANA_FQMMCNT)

Register	Offset	R/W	Description	Reset Value
ANA_FQMMCNT	ANA_BA+0x98	R	Frequency Measurement Count Register	0x0000_0000

Table 7-39 Frequency Measurement Count Register (ANA_FQMMCNT, address 0x4008_0098).

Bits	Description	
[15:0]	FQMMCNT	**Frequency Measurement Count** When MMSTS aaa 1 and G0 aaa 1, this is number of PCLK periods counted for frequency measurement. The frequency will be PCLK aaa FQMMCNT * Fref /(CYCLESEL+1) Hz Maximum resolution of measurement is Fref /(CYCLESEL+1)*2 Hz

9.3 AC Electrical Characteristics

9.3.1 External 32kHz XTAL Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	-	32.768	-	kHz
Temperature	-	-40	-	85	℃
V_{DD}	-	2.4	-	5.5	V

9.3.2 Internal 49.152MHz Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage[1]	-	2.4	-	5.5	V
Center Frequency	-	-	49.152		MHz
Calibrated Internal Oscillator Frequency	+25°C; V_{DD} =5V	-1	-	1	%
	-40°C~+85°C; V_{DD}=2.5V~5.5V	-4	-	4	%

9.3.3 Internal 16 kHz Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage	-	2.4	-	5.5	V
Center Frequency	-	-	16	-	kHz
Calibrated Internal Oscillator Frequency	+25°C; V_{DD} =5V	-10	-	10	%
	-40°C~+85°C; V_{DD}=2.5V~5.5V	-20	-	20	%