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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, LCD, LVD, POR, PWM, SmartSense, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b SAR; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4246azi-l423

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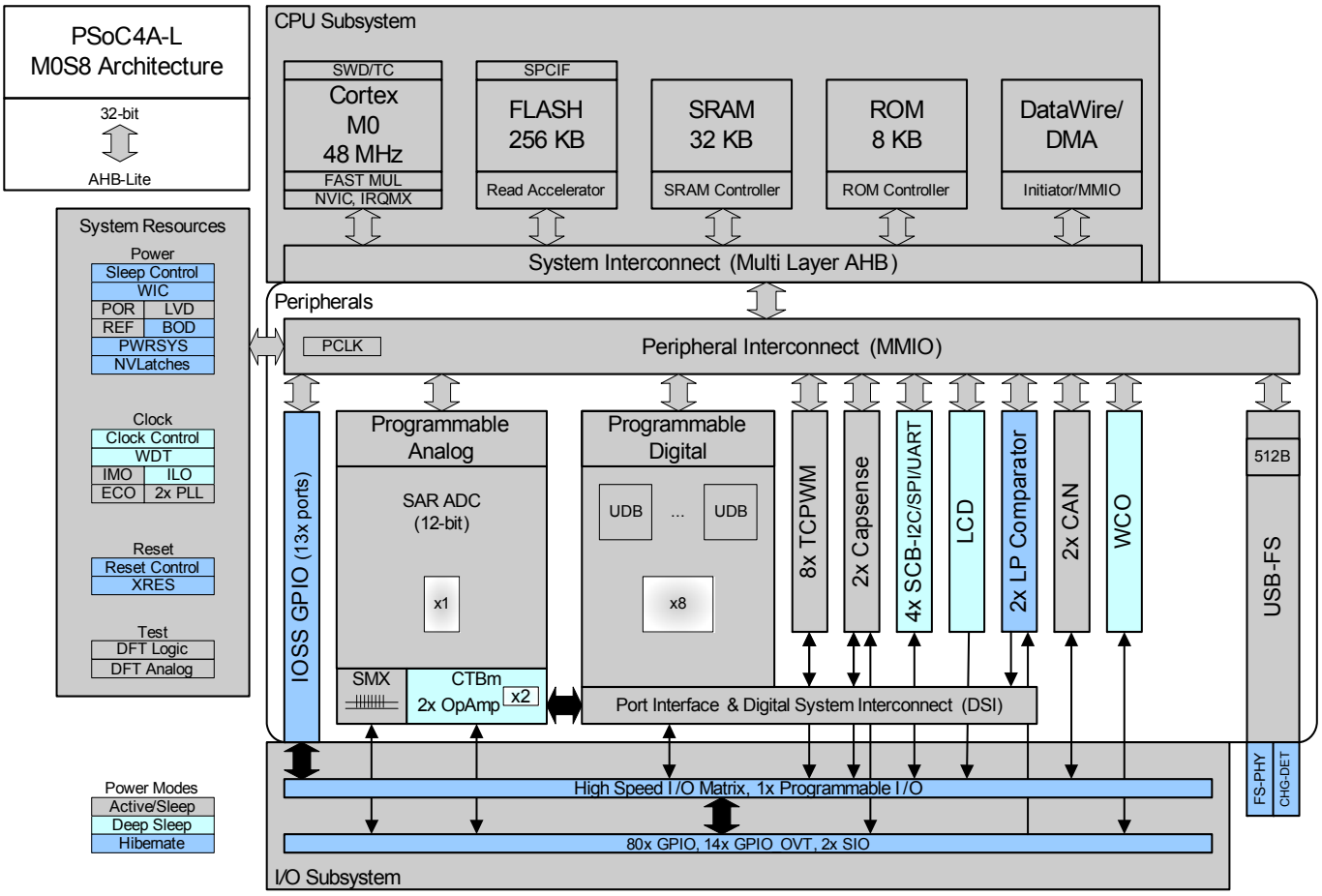
Figure 2. Block Diagram



PSoC 4200-L Block Diagram

The PSoC 4200-L devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM Serial_Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator Integrated Development Environment (IDE) provides fully integrated programming and debug support for PSoC 4200-L devices. The SWD interface is fully compatible with industry-standard third-party tools. The PSoC 4200-L family provides a level of security not possible with multi-chip application solutions or with microcontrollers. This is due to its ability to disable debug features, robust flash protection, and because it allows customer-proprietary functionality to be implemented in on-chip programmable blocks.

The debug circuits are enabled by default and can only be disabled in firmware. If not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. Because all programming, debug, and test interfaces are disabled when maximum device security is enabled, PSoC 4200-L with device security enabled may not be returned for failure analysis. This is a trade-off the PSoC 4200-L allows the customer to make.

Functional Definition

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in the PSoC 4200-L is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and execute a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC), which can wake the processor up from the Deep Sleep mode allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a 2-wire form of JTAG; the debug configuration used for PSoC 4200-L has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The PSoC 4200-L has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 2 wait-state (WS) access time at 48 MHz and with 1-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

SRAM

SRAM memory is retained during Hibernate.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

DMA

A DMA engine is provided that can do 32-bit transfers and has chainable ping-pong descriptors.

System Resources

Power System

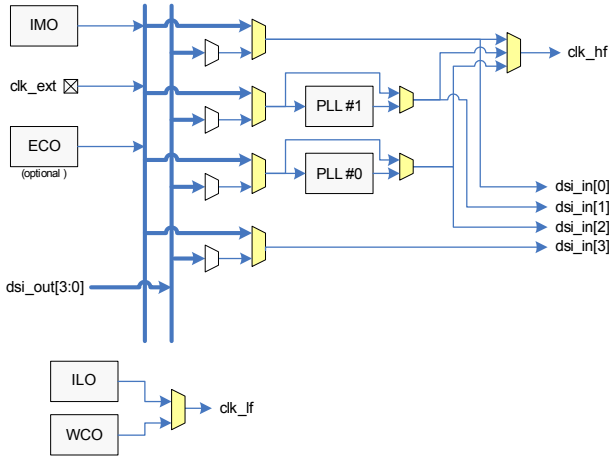
The power system is described in detail in the section Power on page 15. It provides assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (brown-out detect (BOD)) or interrupts (low voltage detect (LVD)). The PSoC 4200-L operates with a single external supply over the range of 1.71 to 5.5 V and has five different power modes, transitions between which are managed by the power system. The PSoC 4200-L provides Sleep, Deep Sleep, Hibernate, and Stop low-power modes.

Clock System

The PSoC 4200-L clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that no meta-stable conditions occur.

The clock system for the PSoC 4200-L consists of a crystal oscillator (4 to 33 MHz), a watch crystal oscillator (32 kHz), a phase-locked loop (PLL), the IMO and the ILO internal oscillators, and provision for an external clock.

Figure 3. PSoC 4200-L MCU Clocking Architecture



The clk_hf signal can be divided down to generate synchronous clocks for the UDBs, and the analog and digital peripherals. There are a total of 16 clock dividers for the PSoC 4200-L, each with 16-bit divide capability; this allows 12 to be used for the fixed-function blocks and four for the UDBs. The analog clock leads the digital clocks to allow analog events to occur before digital clock-related noise is generated. The 16-bit capability allows a lot of flexibility in generating fine-grained frequency values and is fully supported in PSoC Creator.

IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 4200-L. It is trimmed during testing to achieve the specified accuracy. Trim values are stored in nonvolatile latches (NVL). Additional trim settings from flash can be used to compensate for changes. The IMO default frequency is 24 MHz and it can be adjusted between 3 to 48 MHz in steps of 1 MHz. IMO tolerance with Cypress-provided calibration settings is ±2%.

ILO Clock Source

The ILO is a very low power oscillator, nominally 32 kHz, which is primarily used to generate clocks for peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

Crystal Oscillators and PLL

The PSoC 4200-L clock subsystem also implements two oscillators: high-frequency (4 to 33 MHz) and low-frequency (32-kHz watch crystal) that can be used for precision timing applications. The PLL can generate a 48-MHz output from the high-frequency oscillator.

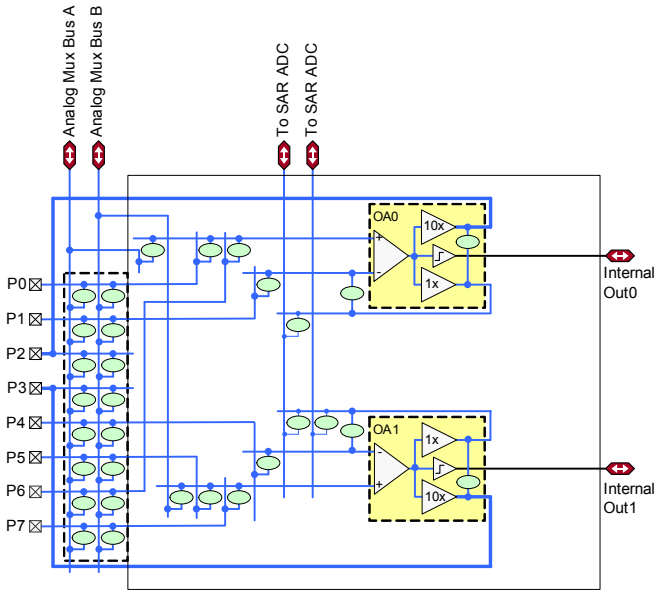
Analog Multiplex Bus

The PSoC4200-L has two concentric analog buses (Analog Mux Bus A and Analog Mux Bus B) that circumnavigate the periphery of the chip. These buses can transport analog signals from any pin to various analog blocks (including the opamps) and to the CapSense blocks allowing, for instance, the ADC to monitor any pin on the chip. These buses are independent and can also be split into three independent sections. This allows one section to be used for CapSense purposes, one for general analog signal processing, and the third for general-purpose digital peripherals and GPIO.

Four Opamps (CTBm Blocks)

The PSoC 4200-L has four opamps with Comparator modes, which allow most common analog functions to be performed on-chip eliminating external components; PGAs, voltage buffers, filters, trans-impedance amplifiers, and other functions can be realized with external passives saving power, cost, and space. The on-chip opamps are designed with enough bandwidth to drive the Sample-and-Hold circuit of the ADC without requiring external buffering. The opamps can operate in the Deep Sleep mode at very low power levels. The following diagram shows one of two identical opamp pairs of the opamp subsystem.

Figure 5. Identical Opamp Pairs in Opamp Subsystem



The ovals in Figure 5 represent analog switches, which may be controlled via user firmware, the SAR sequencer, or user-defined programmable logic. The opamps (OA0 and OA1) are configurable via these switches to perform all standard opamp functions with appropriate feedback components.

The opamps (OA0 and OA1) are programmable and reconfigurable to provide standard opamp functionality via switchable feedback components, unity gain functionality for driving pins directly, or for internal use (such as buffering SAR ADC inputs as indicated in the diagram), or as true comparators.

The opamp inputs provide highly flexible connectivity and can connect directly to dedicated pins or, via the analog mux buses, to any pin on the chip. Analog switch connectivity is controllable by user firmware as well as user-defined programmable digital state machines (implemented via UDBs).

The opamps operate in Deep Sleep mode at very low currents allowing analog circuits to remain operational during Deep Sleep.

Temperature Sensor

The PSoC 4200-L has one on-chip temperature sensor. This consists of a diode, which is biased by a current source that can be disabled to save power. The temperature sensor is connected to the ADC, which digitizes the reading and produces a temperature value using Cypress-supplied software that includes calibration and linearization.

Low-power Comparators

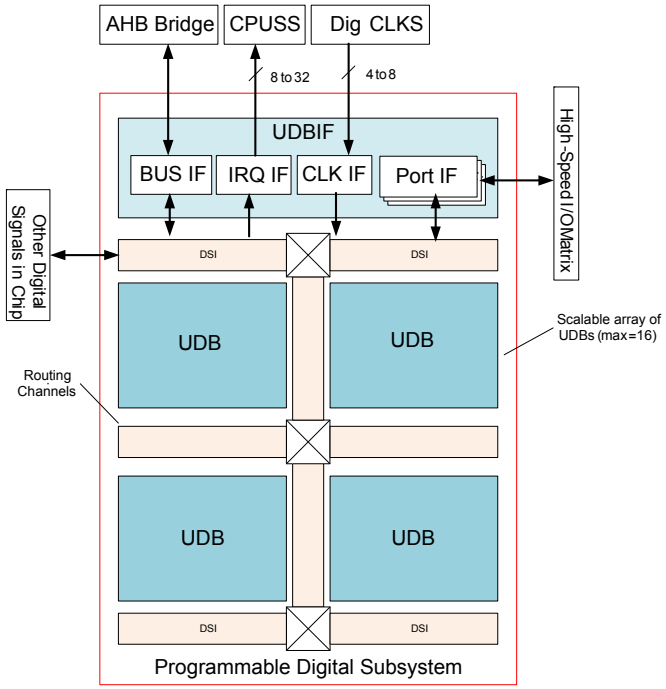
The PSoC 4200-L has a pair of low-power comparators, which can also operate in the Deep Sleep and Hibernate modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid meta-stability unless operating in an asynchronous power mode (Hibernate) where the system wake-up circuit is activated by a comparator switch event.

Programmable Digital

Universal Digital Blocks (UDBs) and Port Interfaces

The PSoC 4200-L has eight UDBs; the UDB array also provides a switched Digital System Interconnect (DSI) fabric that allows signals from peripherals and ports to be routed to and through the UDBs for communication and control. The UDB array is shown in the following figure.

Figure 6. UDB Array



CAN Blocks

There are two independent CAN 2.0B blocks, which are certified CAN conformant.

GPIO

The PSoC 4200-L has 96 GPIOs. The GPIO block implements the following:

- Eight drive strength modes including strong push-pull, resistive pull-up and pull-down, weak (resistive) pull-up and pull-down, open drain and open source, input only, and disabled
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output disables
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode and Hibernate modes)
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals are also fixed to reduce internal multiplexing complexity (these signals do not go through the DSI network). DSI signals are not affected by this and any pin may be routed to any UDB through the DSI network.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (13 for PSoC 4200-L).

There are 14 GPIO pins that are overvoltage tolerant (V_{IN} can exceed V_{DD}). The overvoltage cells will not sink more than 10 µA when their inputs exceed V_{DDIO} in compliance with I^2C specifications. Meeting the I^2C minimum fall time requirement for FM and FM+ may require the slower slew rate setting depending on bus loading (also applies to all GPIO and SIO pins).

SIO

The Special I/O (SIO) pins have the following features in addition to the GPIO features:

- Overvoltage protection and hot swap capability
- Programmable switching thresholds
- Programmable output pull-up voltage capability

They allow interfacing to buses, such as I^2C with full I^2C compatibility and interfacing to devices operating at different voltage levels. There are two SIO pins on the PSoC4200-L.

Special Function Peripherals

LCD Segment Drive

The PSoC 4200-L has an LCD controller, which can drive up to eight commons and up to 56 segments. Any pin can be either a common or a segment pin. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as digital correlation and PWM.

Digital correlation pertains to modulating the frequency and levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays.

PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep refreshing a small display buffer (4 bits; 1 32-bit register per port).

CapSense

CapSense is supported on all pins in the PSoC 4200-L through two CapSense Sigma-Delta (CSD) blocks that can be connected to any pin through an analog mux bus that any GPIO pin can be connected to via an Analog switch. CapSense function can thus be provided on any pin or group of pins in a system under software control. A component is provided for the CapSense block to make it easy for the user.

Shield voltage can be driven on another Mux Bus to provide water tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input.

Each CapSense block has two IDACs which can be used for general purposes if CapSense is not being used.(both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available). The two CapSense blocks can be used independently.

124-BGA		68-QFN		64-TQFP		48-TQFP		48-TQFP-USB	
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
C3	VSSA	61	VSSA	57	VSSA	41	VSSA	41	VSSA
C5	P1.0	62	P1.0	58	P1.0	42	P1.0	42	P1.0
B5	P1.1	63	P1.1	59	P1.1	43	P1.1	43	P1.1
A5	P1.2	64	P1.2	60	P1.2	44	P1.2	44	P1.2
A4	P1.3	65	P1.3	61	P1.3	45	P1.3	45	P1.3
B4	P1.4	66	P1.4	62	P1.4	46	P1.4	46	P1.4
C4	P1.5	67	P1.5	63	P1.5	47	P1.5	47	P1.5
A3	P1.6	68	P1.6	64	P1.6	48	P1.6	48	P1.6
B3	P1.7	1	P1.7/VREF	1	P1.7/VREF	1	P1.7/VREF	1	P1.7/VREF
B1	VREF	1	P1.7/VREF	1	P1.7/VREF	1	P1.7/VREF	1	P1.7/VREF
C3	VSSA								
D4	VSSA								
B2	VDDA								
C1	P2.0	2	P2.0	2	P2.0	2	P2.0	2	P2.0
C2	P2.1	3	P2.1	3	P2.1	3	P2.1	3	P2.1
D1	P2.2	4	P2.2	4	P2.2	4	P2.2	4	P2.2
D2	P2.3	5	P2.3	5	P2.3	5	P2.3	5	P2.3
D3	P2.4	6	P2.4	6	P2.4	6	P2.4	6	P2.4
E1	P2.5	7	P2.5	7	P2.5	7	P2.5	7	P2.5
E2	P2.6	8	P2.6	8	P2.6	8	P2.6	8	P2.6
E3	P2.7	9	P2.7	9	P2.7	9	P2.7	9	P2.7
K4	VSSD	10	VSSA	10	VSSA	10	VSSD	10	VSSD
A1	VDDA	11	VDDA	11	VDDA				
F1	P10.0								
F2	P10.1								
F3	P10.2								
G1	P10.3								
G2	P10.4								
G3	P10.5								
H1	P10.6								
H2	P10.7								
K4	VSSD								
J1	P6.0	12	P6.0	12	P6.0				
J2	P6.1	13	P6.1	13	P6.1				
J3	P6.2	14	P6.2	14	P6.2				
K1	P6.3	15	P6.3						
K2	P6.4	16	P6.4/P12.0	15	P6.4/P12.0				
L1	P12.0	16	P6.4/P12.0	15	P6.4/P12.0				
L2	P12.1	17	P6.5/P12.1	16	P6.5/P12.1				
K3	P6.5	17	P6.5/P12.1	16	P6.5/P12.1				
L3	VSSD	18	VSSIO	17	VSSIO	10	VSSD	10	VSSD
N2	P3.0	19	P3.0	18	P3.0	12	P3.0	12	P3.0
M2	P3.1	20	P3.1	19	P3.1	13	P3.1	13	P3.1
N3	P3.2	21	P3.2	20	P3.2	14	P3.2	14	P3.2

Port/Pin	Analog	PRGIO & USB	Alt. Function 1	Alt. Function 2	Alt. Function 3	Alt. Function 4	Alt. Function 5
P1.5	ctb0_pads[5]		tcpwm.line_compl[6]:1				scb[0].spi_select2:1
P1.6	ctb0_pads[6]		tcpwm.line[7]:1				scb[0].spi_select3:1
P1.7	ctb0_pads[7], sar_ext_vref		tcpwm.line_compl[7]:1				
P2.0	sarmux_pads[0]		tcpwm.line[4]:1	scb[1].uart_rx:1		scb[1].i2c_scl:1	scb[1].spi_mosi:1
P2.1	sarmux_pads[1]		tcpwm.line_compl[4]:1	scb[1].uart_tx:1		scb[1].i2c_sda:1	scb[1].spi_miso:1
P2.2	sarmux_pads[2]		tcpwm.line[5]:1	scb[1].uart_cts:1			scb[1].spi_clk:1
P2.3	sarmux_pads[3]		tcpwm.line_compl[5]:1	scb[1].uart_rts:1			scb[1].spi_select0:1
P2.4	sarmux_pads[4]		tcpwm.line[0]:1				scb[1].spi_select1:0
P2.5	sarmux_pads[5]		tcpwm.line_compl[0]:1				scb[1].spi_select2:0
P2.6	sarmux_pads[6]		tcpwm.line[1]:1				scb[1].spi_select3:0
P2.7	sarmux_pads[7]		tcpwm.line_compl[1]:1				
P10.0				scb[2].uart_rx:1		scb[2].i2c_scl:1	scb[2].spi_mosi:1
P10.1				scb[2].uart_tx:1		scb[2].i2c_sda:1	scb[2].spi_miso:1
P10.2				scb[2].uart_cts:1			scb[2].spi_clk:1
P10.3				scb[2].uart_rts:1			scb[2].spi_select0:1
P10.4							scb[2].spi_select1:1
P10.5							scb[2].spi_select2:1
P10.6							scb[2].spi_select3:1
P10.7							
P6.0			tcpwm.line[4]:0	scb[3].uart_rx:1	can[0].can_tx_enb_n:0	scb[3].i2c_scl:1	scb[3].spi_mosi:1
P6.1			tcpwm.line_compl[4]:0	scb[3].uart_tx:1	can[0].can_rx:0	scb[3].i2c_sda:1	scb[3].spi_miso:1
P6.2			tcpwm.line[5]:0	scb[3].uart_cts:1	can[0].can_tx:0	scb[2].i2c_scl:3	scb[3].spi_clk:1
P6.3			tcpwm.line_compl[5]:0	scb[3].uart_rts:1		scb[2].i2c_sda:3	scb[3].spi_select0:1
P6.4			tcpwm.line[6]:0			scb[0].i2c_scl:3	scb[3].spi_select1:1
P12.0			tcpwm.line[7]:0			scb[1].i2c_scl:3	scb[3].spi_select3:1
P12.1			tcpwm.line_compl[7]:0			scb[1].i2c_sda:3	
P6.5			tcpwm.line_compl[6]:0			scb[0].i2c_sda:3	scb[3].spi_select2:1
P3.0			tcpwm.line[0]:0	scb[1].uart_rx:2		scb[1].i2c_scl:2	scb[1].spi_mosi:2
P3.1			tcpwm.line_compl[0]:0	scb[1].uart_tx:2		scb[1].i2c_sda:2	scb[1].spi_miso:2
P3.2			tcpwm.line[1]:0	scb[1].uart_cts:2		cpuss.swd_data:0	scb[1].spi_clk:2
P3.3			tcpwm.line_compl[1]:0	scb[1].uart_rts:2		cpuss.swd_clk:0	scb[1].spi_select0:2
P3.4			tcpwm.line[2]:0				scb[1].spi_select1:1
P3.5			tcpwm.line_compl[2]:0				scb[1].spi_select2:1
P3.6			tcpwm.line[3]:0				scb[1].spi_select3:1
P3.7			tcpwm.line_compl[3]:0				
P11.0		prgio[0].io[0]	tcpwm.line[4]:3	scb[2].uart_rx:2		scb[2].i2c_scl:2	scb[2].spi_mosi:2
P11.1		prgio[0].io[1]	tcpwm.line_compl[4]:3	scb[2].uart_tx:2		scb[2].i2c_sda:2	scb[2].spi_miso:2
P11.2		prgio[0].io[2]	tcpwm.line[5]:3	scb[2].uart_cts:2		cpuss.swd_data:1	scb[2].spi_clk:2
P11.3		prgio[0].io[3]	tcpwm.line_compl[5]:3	scb[2].uart_rts:2		cpuss.swd_clk:1	scb[2].spi_select0:2
P11.4		prgio[0].io[4]	tcpwm.line[6]:3				scb[2].spi_select1:2
P11.5		prgio[0].io[5]	tcpwm.line_compl[6]:3				scb[2].spi_select2:2
P11.6		prgio[0].io[6]	tcpwm.line[7]:3				scb[2].spi_select3:2
P11.7		prgio[0].io[7]	tcpwm.line_compl[7]:3				
P4.0				scb[0].uart_rx:2	can[0].can_rx:1	scb[0].i2c_scl:2	scb[0].spi_mosi:2
P4.1				scb[0].uart_tx:2	can[0].can_tx:1	scb[0].i2c_sda:2	scb[0].spi_miso:2

Analog Peripherals

Opamp

Table 8. Opamp Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
	I_{DD}	Opamp block current. No load.	–	–	–	–	
SID269	I_{DD_HI}	Power = high	–	1100	1850	µA	
SID270	I_{DD_MED}	Power = medium	–	550	950	µA	
SID271	I_{DD_LOW}	Power = low	–	150	350	µA	
	GBW	Load = 20 pF, 0.1 mA. V_{DDA} = 2.7 V	–	–	–	–	
SID272	GBW_HI	Power = high	6	–	–	MHz	
SID273	GBW_MED	Power = medium	4	–	–	MHz	
SID274	GBW_LO	Power = low	–	1	–	MHz	
	I_{OUT_MAX}	$V_{DDA} \geq 2.7$ V, 500 mV from rail	–	–	–	–	
SID275	$I_{OUT\_MAX\_HI}$	Power = high	10	–	–	mA	
SID276	$I_{OUT\_MAX\_MID}$	Power = medium	10	–	–	mA	
SID277	$I_{OUT\_MAX\_LO}$	Power = low	–	5	–	mA	
	I_{OUT}	V_{DDA} = 1.71 V, 500 mV from rail	–	–	–	–	
SID278	$I_{OUT\_MAX\_HI}$	Power = high	4	–	–	mA	
SID279	$I_{OUT\_MAX\_MID}$	Power = medium	4	–	–	mA	
SID280	$I_{OUT\_MAX\_LO}$	Power = low	–	2	–	mA	
SID281	V_{IN}	Input voltage range	–0.05	–	V_{DDA}– 0.2	V	Charge-pump on, $V_{DDA} \geq$ 2.7 V
SID282	V_{CM}	Input common mode voltage	–0.05	–	VDDA – 0.2	V	Charge-pump on, $V_{DDA} \geq$ 2.7 V
	V_{OUT}	$V_{DDA} \geq 2.7$ V	–	–	–		
SID283	V_{OUT_1}	Power = high, I_{load}=10 mA	0.5	–	VDDA – 0.5	V	
SID284	V_{OUT_2}	Power = high, I_{load}=1 mA	0.2	–	VDDA – 0.2	V	
SID285	V_{OUT_3}	Power = medium, I_{load}=1 mA	0.2	–	VDDA – 0.2	V	
SID286	V_{OUT_4}	Power = low, I_{load}=0.1mA	0.2	–	VDDA – 0.2	V	
SID288	V_{OS_TR}	Offset voltage, trimmed	1	±0.5	1	mV	High mode
SID288A	V_{OS_TR}	Offset voltage, trimmed	–	±1	–	mV	Medium mode
SID288B	V_{OS_TR}	Offset voltage, trimmed	–	±2	–	mV	Low mode
SID290	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–10	±3	10	µV/°C	High mode
SID290A	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/°C	Medium mode
SID290B	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/°C	Low mode
SID291	CMRR	DC	60	70	–	dB	V_{DDD} = 3.6 V
SID292	PSRR	At 1 kHz, 100 mV ripple	70	85	–	dB	VDDD = 3.6 V
	Noise		–	–	–	–	
SID293	V_{N1}	Input referred, 1 Hz - 1GHz, power = high	–	94	–	µVrms	
SID294	V_{N2}	Input referred, 1 kHz, power = high	–	72	–	nV/rtHz	

Table 10. Comparator AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID91	T_{RESP1}	Response time, normal mode	–	38	110	ns	50-mV overdrive
SID258	T_{RESP2}	Response time, low power mode	–	70	200	ns	50-mV overdrive
SID92	T_{RESP3}	Response time, ultra low power mode	–	2.3	15	µs	200-mV overdrive. $V_{DDD} \geq 2.2$ V for Temp < 0 °C, $V_{DDD} \geq 1.8$ V for Temp > 0 °C

Temperature Sensor

Table 11. Temperature Sensor Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID93	$T_{SENSACC}$	Temperature sensor accuracy	–5	±1	+5	°C	–40 to +85 °C

SAR ADC

Table 12. SAR ADC DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID94	A_RES	Resolution	–	–	12	bits	
SID95	A_CHNIS_S	Number of channels - single ended	–	–	16		8 full speed
SID96	A-CHNKS_D	Number of channels - differential	–	–	8		Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity	–	–	–		Yes. Based on characterization
SID98	A_GAINERR	Gain error	–	–	±0.1	%	With external reference.
SID99	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V V_{REF}.
SID100	A_ISAR	Current consumption	–	–	1	mA	
SID101	A_VINS	Input voltage range - single ended	V_{SS}	–	V_{DDA}	V	Based on device characterization
SID102	A_VIND	Input voltage range - differential	V_{SS}	–	V_{DDA}	V	Based on device characterization
SID103	A_INRES	Input resistance	–	–	2.2	KΩ	Based on device characterization
SID104	A_INCAP	Input capacitance	–	–	10	pF	Based on device characterization

Table 13. SAR ADC AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID106	A_PSRR	Power supply rejection ratio	70	–	–	dB	
SID107	A_CMRR	Common mode rejection ratio	66	–	–	dB	Measured at 1 V
SID108	A_SAMP_1	Sample rate with external reference bypass cap	–	–	1	Msps	
SID108A	A_SAMP_2	Sample rate with no bypass cap. Reference = V_{DD}	–	–	500	Ksps	

Table 13. SAR ADC AC Specifications

(Guaranteed by Characterization) *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID108B	A_SAMP_3	Sample rate with no bypass cap. Internal reference	–	–	100	ksps	
SID109	A_SNDR	Signal-to-noise and distortion ratio (SINAD)	65	–	–	dB	F_{IN} = 10 kHz
SID111	A_INL	Integral non linearity	–1.7	–	+2	LSB	V_{DD} = 1.71 to 5.5, 1 Msps, Vref = 1 to 5.5.
SID111A	A_INL	Integral non linearity	–1.5	–	+1.7	LSB	V_{DDD} = 1.71 to 3.6, 1 Msps, Vref = 1.71 to V_{DDD}.
SID111B	A_INL	Integral non linearity	–1.5	–	+1.7	LSB	V_{DDD} = 1.71 to 5.5, 500 ksps, Vref = 1 to 5.5.
SID112	A_DNL	Differential non linearity	–1	–	+2.2	LSB	V_{DDD} = 1.71 to 5.5, 1 Msps, Vref = 1 to 5.5.
SID112A	A_DNL	Differential non linearity	–1	–	+2	LSB	V_{DDD} = 1.71 to 3.6, 1 Msps, Vref = 1.71 to V_{DDD}.
SID112B	A_DNL	Differential non linearity	–1	–	+2.2	LSB	V_{DDD} = 1.71 to 5.5, 500 ksps, Vref = 1 to 5.5.
SID113	A_THD	Total harmonic distortion	–	–	–65	dB	F_{IN} = 10 kHz.

CSD

Table 14. CSD Block Specification

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
CSD Specification							
SID308	VCSD	Voltage range of operation	1.71	–	5.5	V	
SID309	IDAC1	DNL for 8-bit resolution	–1	–	1	LSB	
SID310	IDAC1	INL for 8-bit resolution	–3	–	3	LSB	
SID311	IDAC2	DNL for 7-bit resolution	–1	–	1	LSB	
SID312	IDAC2	INL for 7-bit resolution	–3	–	3	LSB	
SID313	SNR	Ratio of counts of finger to noise. Guaranteed by characterization	5	–	–	Ratio	Capacitance range of 9 to 35 pF, 0.1 pF sensitivity
SID314	IDAC1_CRT1	Output current of Idac1 (8-bits) in High range	–	612	–	µA	
SID314A	IDAC1_CRT2	Output current of Idac1(8-bits) in Low range	–	306	–	µA	
SID315	IDAC2_CRT1	Output current of Idac2 (7-bits) in High range	–	304.8	–	µA	
SID315A	IDAC2_CRT2	Output current of Idac2 (7-bits) in Low range	–	152.4	–	µA	

SPI Specifications

Table 22. Fixed SPI DC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units
SID163	I_{SPI1}	Block current consumption at 1 Mbits/sec	–	–	360	µA
SID164	I_{SPI2}	Block current consumption at 4 Mbits/sec	–	–	560	µA
SID165	I_{SPI3}	Block current consumption at 8 Mbits/sec	–	–	600	µA

Table 23. Fixed SPI AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units
SID166	F_{SPI}	SPI operating frequency (master; 6X oversampling)	–	–	8	MHz

Table 24. Fixed SPI Master Mode AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units
SID167	T_{DMO}	MOSI valid after Sclock driving edge	–	–	15	ns
SID168	T_{DSI}	MISO valid before Sclock capturing edge. Full clock, late MISO Sampling used	20	–	–	ns
SID169	T_{HMO}	Previous MOSI data hold time with respect to capturing edge at Slave	0	–	–	ns

Table 25. Fixed SPI Slave mode AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units
SID170	T_{DMI}	MOSI valid before Sclock capturing edge	40	–	–	ns
SID171	T_{DSO}	MISO valid after Sclock driving edge	–	–	$42 + 3 \times T_{SCB}$	ns
SID171A	T_{DSO_ext}	MISO valid after Sclock driving edge in Ext. Clock mode	–	–	48	ns
SID172	T_{HSO}	Previous MISO data hold time	0	–	–	ns
SID172A	$T_{SSELSCK}$	SSEL Valid to first SCK Valid edge	100	–	–	ns

SWD Interface

Table 32. SWD Interface Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID213	F_SWDCLK1	3.3 V ≤ V_{DD} ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID214	F_SWDCLK2	1.71 V ≤ V_{DD} ≤ 3.3 V	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID215	T_SWDI_SETUP	T = 1/f SWDCLK	0.25*T	–	–	ns	Guaranteed by characterization
SID216	T_SWDI_HOLD	T = 1/f SWDCLK	0.25*T	–	–	ns	Guaranteed by characterization
SID217	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5*T	ns	Guaranteed by characterization
SID217A	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	Guaranteed by characterization

Internal Main Oscillator

Table 33. IMO DC Specifications

(Guaranteed by Design)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I_{IMO1}	IMO operating current at 48 MHz	–	–	1000	µA	
SID219	I_{IMO2}	IMO operating current at 24 MHz	–	–	325	µA	
SID220	I_{IMO3}	IMO operating current at 12 MHz	–	–	225	µA	
SID221	I_{IMO4}	IMO operating current at 6 MHz	–	–	180	µA	
SID222	I_{IMO5}	IMO operating current at 3 MHz	–	–	150	µA	

Table 34. IMO AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	$F_{IMOTOL1}$	Frequency variation from 3 to 48 MHz	–	–	±2	%	
SID226	$T_{STARTIMO}$	IMO startup time	–	–	12	µs	
SID227	$T_{JITRMSIMO1}$	RMS Jitter at 3 MHz	–	156	–	ps	
SID228	$T_{JITRMSIMO2}$	RMS Jitter at 24 MHz	–	145	–	ps	
SID229	$T_{JITRMSIMO3}$	RMS Jitter at 48 MHz	–	139	–	ps	

Internal Low-Speed Oscillator

Table 35. ILO DC Specifications

(Guaranteed by Design)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	I_{ILO1}	ILO operating current at 32 kHz	–	0.3	1.05	µA	Guaranteed by Characterization
SID233	$I_{ILOLEAK}$	ILO leakage current	–	2	15	nA	Guaranteed by Design

Table 36. ILO AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	$T_{STARTILO1}$	ILO startup time	–	–	2	ms	Guaranteed by characterization
SID236	$T_{ILODUTY}$	ILO duty cycle	40	50	60	%	Guaranteed by characterization
SID237	$F_{ILOTRIM1}$	32 kHz trimmed frequency	15	32	50	kHz	±60% with trim.

Table 37. PLL DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID410	IDD_PLL_48	In = 3 MHz, Out = 48 MHz	–	530	610	µA	
SID411	IDD_PLL_24	In = 3 MHz, Out = 24 MHz	–	300	405	µA	

Table 38. PLL AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID412	F_{PLLIN}	PLL input frequency	1	–	48	MHz	
SID413	F_{PLLINT}	PLL intermediate frequency; prescaler out	1	–	3	MHz	
SID414	F_{PLLVCO}	VCO output frequency before post-divide	22.5	–	104	MHz	
SID415	D_{IVVCO}	VCO Output post-divider range; PLL output frequency is F_{PPLVCO}/D_{IVVCO}	1	–	8	–	
SID416	PLLlocktime	Lock time at startup	–	–	250	us	
SID417	Jperiod_1	Period jitter for VCO ≥ 67 MHz	–	–	150	ps	Guaranteed By Design
SID416A	Jperiod_2	Period jitter for VCO ≤ 67 MHz	–	–	200	ps	Guaranteed By Design

Table 39. External Clock Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305	ExtClkFreq	External Clock input Frequency	0	–	48	MHz	Guaranteed by characterization
SID306	ExtClkDuty	Duty cycle; Measured at $V_{DD/2}$	45	–	55	%	Guaranteed by characterization

Table 40. Watch Crystal Oscillator (WCO) Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
IMO WCO-PLL calibrated mode							
SID330	IMOWCO1	Frequency variation with IMO set to 3 MHz	–0.6	–	0.6	%	Does not include WCO tolerance
SID331	IMOWCO2	Frequency variation with IMO set to 5 MHZ	–0.4	–	0.4	%	Does not include WCO tolerance
SID332	IMOWCO3	Frequency variation with IMO set to 7 or 9 MHZ	–0.3	–	0.3	%	Does not include WCO tolerance
SID333	IMOWCO4	All other IMO frequency settings	–0.2	–	0.2	%	Does not include WCO tolerance

Table 46. SIO Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SIO DC Specifications							
SID330	V_{IH}	Input voltage high threshold	0.7*VDD	–	–	V	CMOS input; with respect to V_{DDIO}
SID331	V_{IL}	Input voltage low threshold	–	–	0.3*VDD	V	CMOS input; with respect to V_{DDIO}
SID332	V_{IH}	Differential input mode high voltage; hysteresis disabled	Vr+0.2	–	–	V	Vr is the SIO reference voltage
SID333	V_{IL}	Differential input mode low voltage, hysteresis disabled	–	–	Vr-0.2	V	Vr is the SIO reference voltage
SID334	V_{OH}	Output high voltage in unregulated mode	VDDIO - 0.4	–	–	V	I_{OH} = 4 mA, V_{DD} = 3.3 V
SID335	V_{OH}	Output high voltage in regulated mode	Vr - 0.65	–	Vr + 0.2	V	I_{OH} = 1 mA
SID336	V_{OH}	Output high voltage in regulated mode	Vr - 0.3	–	Vr + 0.2	V	I_{OH} = 0.1 mA
SID337	V_{OL}	Output low voltage	–	–	0.8	V	V_{DDIO} = 3.3 V, I_{OL} = 25 mA
SID338	V_{OL}	Output low voltage	–	–	0.4	V	V_{DDIO} = 1.8 V, I_{OL} = 4 mA
SID339	Vinref	Input voltage reference	0.48	–	0.52*VDDIO	V	
SID340	Voutref	Output voltage reference (regulated mode)	1	–	VDDIO-1	V	V_{DDIO} > 3.3
SID341	Voutref	Output voltage reference (regulated mode)	1	–	VDDIO-0.5	V	V_{DDIO} < 3.3
SID342	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID343	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	
SID344	I_{IL}	Input leakage current (absolute value)	–	–	14	nA	$V_{IH} \le V_{DDSIO}$; 25 °C
SID345	I_{IL}	Input leakage current (absolute value)	–	–	10	nA	$V_{IH} > V_{DDSIO}$; 25 °C
SID346	C_{IN}	Input capacitance	–	–	7	pF	
SID347	VHYST-Single	Hysteresis in single-ended mode	–	40	–	mV	
SID348	VHYST_Diff	Hysteresis in differential mode	–	35	–	mV	
SID349	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	
SIO AC Specifications (Guaranteed By Design)							
SID350	T_{RISEF}	Rise time in Fast Strong mode	–	–	12	ns	3.3-V V_{DD}, Cload = 25 pF
SID351	T_{FALLF}	Fall time in Fast Strong mode	–	–	12	ns	3.3-V V_{DD}, Cload = 25 pF
SID352	T_{RISES}	Rise time in Slow Strong mode	–	–	75	ns	3.3-V V_{DD}, Cload = 25 pF
SID353	T_{FALLS}	Fall time in Slow Strong mode	–	–	70	ns	3.3-V V_{DD}, Cload = 25 pF
SID354	F_{SIOUT1}	SIO Fout; Unregulated, Fast Strong mode	–	–	33	MHz	3.3-V ≤ V_{DD} ≤ 5.5 V, 25 pF. Guaranteed by design.
SID355	F_{SIOUT2}	SIO Fout; Unregulated, Fast Strong mode	–	–	16	MHz	1.71-V ≤ V_{DD} ≤ 3.3 V, 25 pF
SID356	F_{SIOUT3}	SIO Fout; Regulated, Fast Strong mode	–	–	20	MHz	3.3-V ≤ V_{DD} ≤ 5.5 V, 25 pF
SID357	F_{SIOUT4}	SIO Fout; Regulated, Fast Strong mode	–	–	10	MHz	1.71 V ≤ V_{DD} ≤ 3.3 V, 25 pF

Table 46. SIO Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID358	F_{SIOUT3}	SIO Fout; Unregulated, Slow Strong mode.	–	–	5	MHz	3.3 V ≤ V_{DD} ≤ 5.5 V, 25 pF
SID359	F_{SIOUT4}	SIO Fout, Unregulated, Slow Strong mode.	–	–	3.5	MHz	1.71 V ≤ V_{DD} ≤ 3.3 V, 25 pF
SID360	F_{SIOUT5}	SIO Fout, Regulated, Slow Strong mode.	–	–	2.5	MHz	1.7 V ≤ V_{DD} ≤ 5.5 V, 25 pF
SID361	F_{GPIOIN}	GPIO input operating frequency;1.71 V ≤ V_{DD} ≤ 5.5 V	–	–	48	MHz	1.71 V ≤ V_{DD} ≤ 5.5 V

Table 47. CAN Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID420	IDD_CAN	Block current consumption	–	–	200	uA	
SID421	CAN_bits	CAN Bit rate (Min 8-MHz clock)	–	–	1	Mbps	

Packaging

The description of the PSoC4200-L package dimensions follows.

SPEC ID#	Package	Description	Package DWG #
PKG_1	124-ball VFBGA	124-ball, 9 mm x 9 mm x 1.0 mm height with 0.65 mm ball pitch	001-97718
PKG_2	64-pin TQFP	64-pin TQFP, 10 mm x10 mm x 1,4 mm height with 0.5 mm pitch	51-85051
PKG_3	68-pin QFN	68-pin QFN, 8 mm x 8 mm x 1.0 mm height with 0.4 mm pitch	001-09618
PKG_4	48-pin TQFP	48-pin TQFP, 7 mm x 7 mm x 1.4 mm height with 0.5 mm pitch	51-85135

Table 49. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature		–40	25.00	85	°C
T_J	Operating junction temperature		–40	–	100	°C
T_{JA}	Package θ_{JA} (124-ball VFBGA)		–	35	–	°C/Watt
T_{JA}	Package θ_{JA} (64-pin TQFP)		–	54	–	°C/Watt
T_{JA}	Package θ_{JA} (68-pin QFN)		–	17	–	°C/Watt
T_{JA}	Package θ_{JA} (48-pin TQFP)		–	67	–	°C/Watt

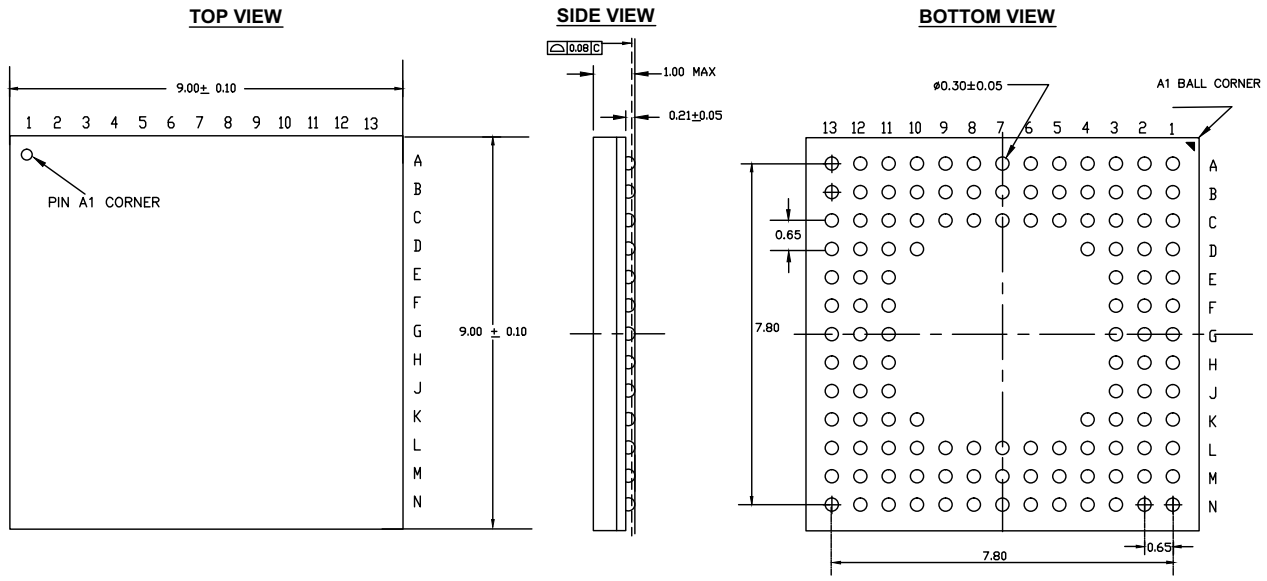
Table 50. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
All packages	260 °C	30 seconds

Table 51. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
All packages	MSL 3

Figure 8. 124-Ball VFBGA Package Outline

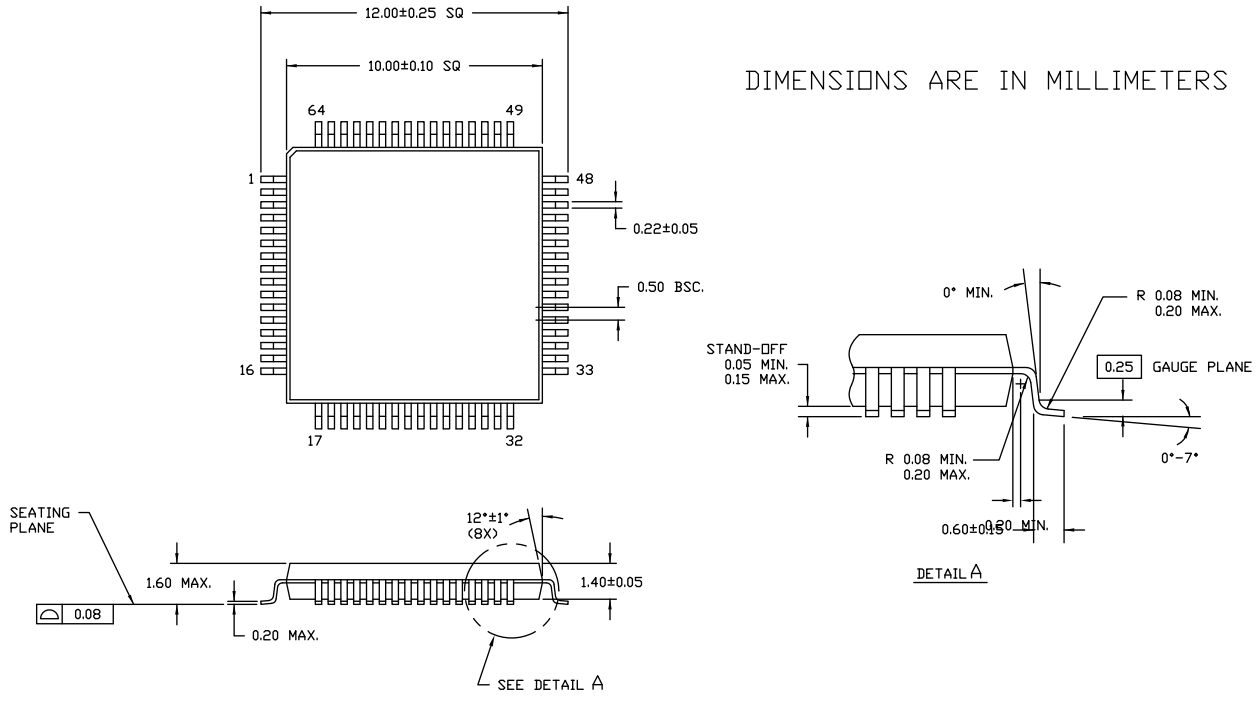


NOTES:

1. REFERENCE JEDEC # MO-280
2. ALL DIMENSIONS ARE IN MILLIMETERS

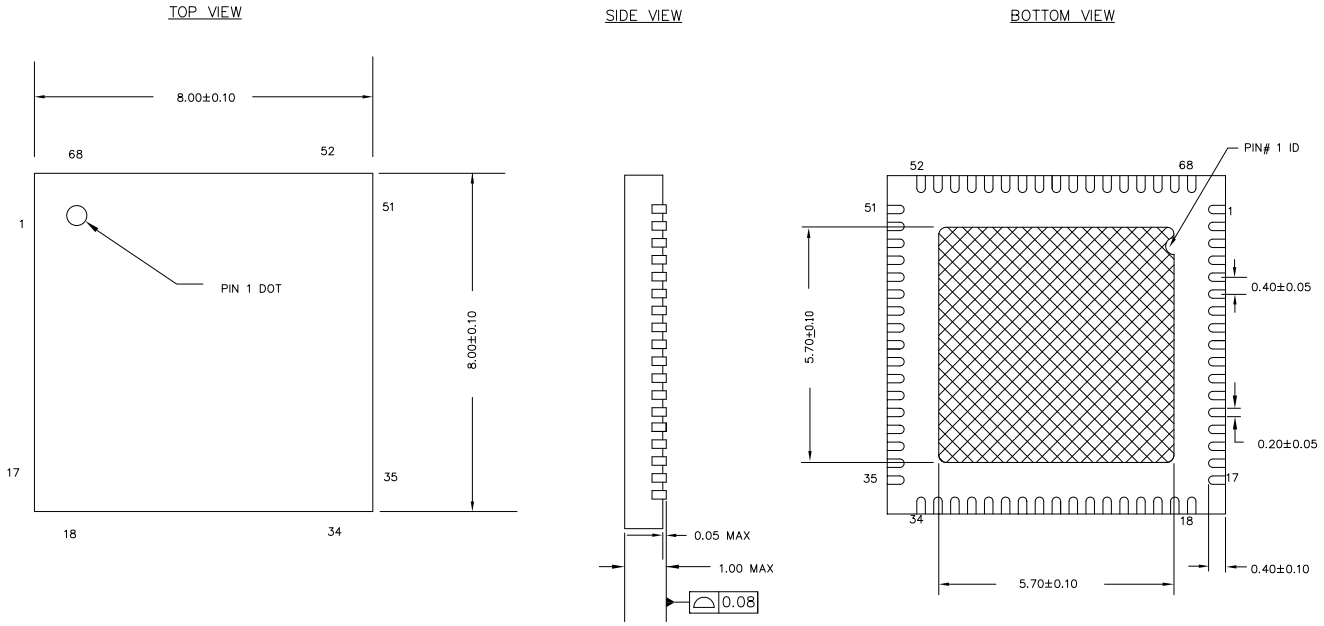
001-97718 **

Figure 9. 64-Pin TQFP Package Outline



51-85051 *D

Figure 10. 68-Pin QFN Package Outline

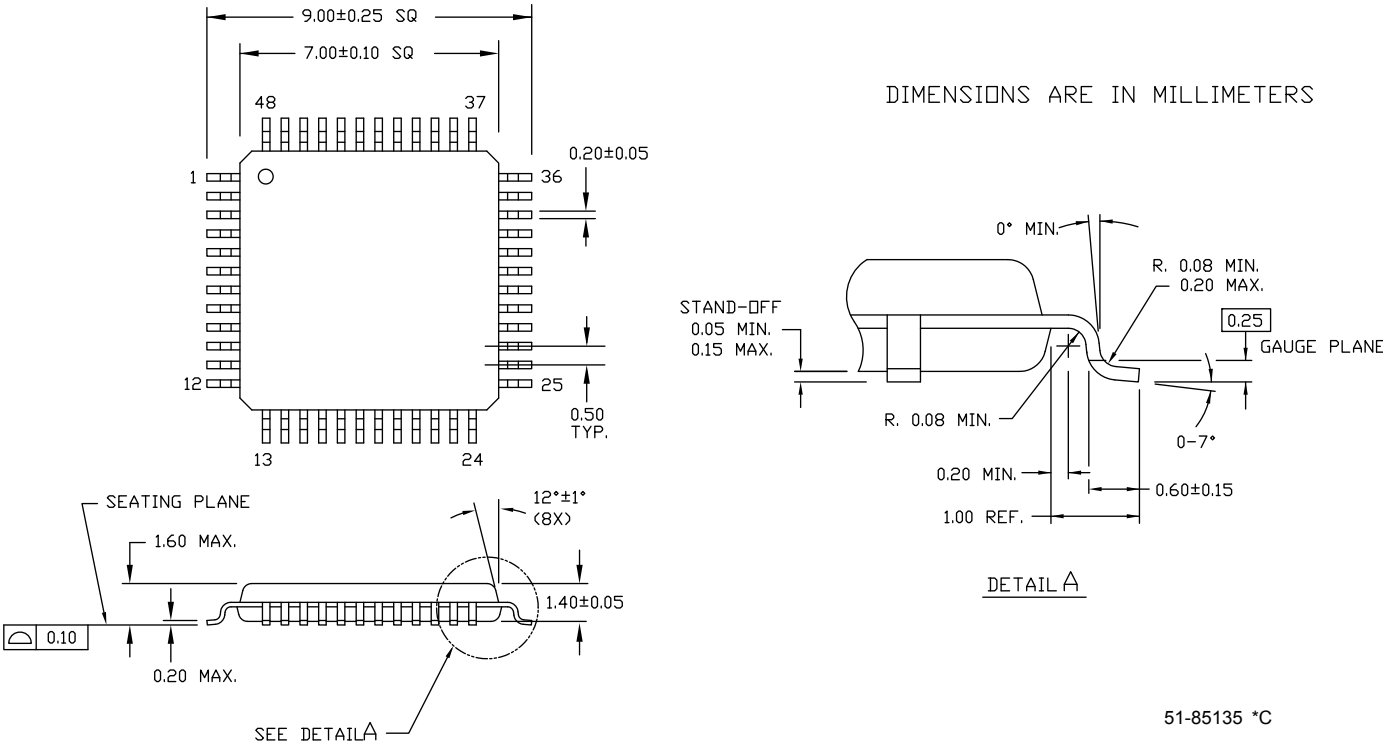


NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 17 ± 2mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-09618 *E

Figure 11. 48-Pin TQFP Package Outline



51-85135 *C

Acronyms

Table 52. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge

Table 52. Acronyms Used in this Document *(continued)*

Acronym	Description
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD

Document Conventions

Units of Measure

Table 53. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt