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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

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Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, LCD, LVD, POR, PWM, SmartSense, WDT
Number of I/O	98
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b SAR; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	124-VFBGA
Supplier Device Package	124-VFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4247bzi-l489

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



# **Functional Definition**

## **CPU and Memory Subsystem**

## CPU

The Cortex-M0 CPU in the PSoC 4200-L is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and execute a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC), which can wake the processor up from the Deep Sleep mode allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a 2-wire form of JTAG; the debug configuration used for PSoC 4200-L has four break-point (address) comparators and two watchpoint (data) comparators.

#### Flash

The PSoC 4200-L has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 2 wait-state (WS) access time at 48 MHz and with 1-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

## SRAM

SRAM memory is retained during Hibernate.

## SROM

A supervisory ROM that contains boot and configuration routines is provided.

## DMA

A DMA engine is provided that can do 32-bit transfers and has chainable ping-pong descriptors.

## System Resources

## Power System

The power system is described in detail in the section Power on page 15. It provides assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (brown-out detect (BOD)) or interrupts (low voltage detect (LVD)). The PSoC 4200-L operates with a single external supply over the range of 1.71 to 5.5 V and has five different power modes, transitions between which are managed by the power system. The PSoC 4200-L provides Sleep, Deep Sleep, Hibernate, and Stop low-power modes.

#### Clock System

The PSoC 4200-L clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that no meta-stable conditions occur.

The clock system for the PSoC 4200-L consists of a crystal oscillator (4 to 33 MHz), a watch crystal oscillator (32 kHz), a phase-locked loop (PLL), the IMO and the ILO internal oscillators, and provision for an external clock.





The clk\_hf signal can be divided down to generate synchronous clocks for the UDBs, and the analog and digital peripherals. There are a total of 16 clock dividers for the PSoC 4200-L, each with 16-bit divide capability; this allows 12 to be used for the fixed-function blocks and four for the UDBs. The analog clock leads the digital clocks to allow analog events to occur before digital clock-related noise is generated. The 16-bit capability allows a lot of flexibility in generating fine-grained frequency values and is fully supported in PSoC Creator.

#### IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 4200-L. It is trimmed during testing to achieve the specified accuracy. Trim values are stored in nonvolatile latches (NVL). Additional trim settings from flash can be used to compensate for changes. The IMO default frequency is 24 MHz and it can be adjusted between 3 to 48 MHz in steps of 1 MHz. IMO tolerance with Cypress-provided calibration settings is ±2%.

#### ILO Clock Source

The ILO is a very low power oscillator, nominally 32 kHz, which is primarily used to generate clocks for peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

## Crystal Oscillators and PLL

The PSoC 4200-L clock subsystem also implements two oscillators: high-frequency (4 to 33 MHz) and low-frequency (32-kHz watch crystal) that can be used for precision timing applications. The PLL can generate a 48-MHz output from the high-frequency oscillator.



#### Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the timeout occurs. The watchdog reset is recorded in the Reset Cause register.

#### Reset

The PSoC 4200-L can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset to avoid complications with configuration and multiple pin functions during power-on or reconfiguration.

#### Voltage Reference

The PSoC 4200-L reference system generates all internally required references. A 1% voltage reference spec is provided for the 12-bit ADC. To allow better signal-to-noise ratios (SNR) and better absolute accuracy, it is possible to add an external bypass capacitor to the internal reference using a GPIO pin or to use an external reference for the SAR.

#### Analog Blocks

#### 12-bit SAR ADC

The 12-bit, 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The block functionality is augmented for the user by adding a reference buffer to it (trimmable to  $\pm 1\%$ ) and by providing the choice (for the PSoC 4200-L case) of three internal voltage refer-

ences:  $V_{DD}$ ,  $V_{DD}/2$ , and  $V_{REF}$  (nominally 1.024 V) as well as an external reference through a GPIO pin. The Sample-and-Hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. The system performance will be 65 dB for true 12-bit precision if appropriate references are used and system noise levels permit. To improve performance in noisy conditions, it is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer (expandable to 16 inputs). The sequencer cycles through selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, the aggregate sampling bandwidth is equal to 1 Msps, whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware-driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. In addition, the signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is able to digitize the output of the on-board temperature sensor for calibration and other temperature-dependent functions. The SAR is not available in Deep Sleep and Hibernate modes as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 to 5.5 V.

#### Figure 4. SAR ADC System Diagram





#### Analog Multiplex Bus

The PSoC4200-L has two concentric analog buses (Analog Mux Bus A and Analog Mux Bus B) that circumnavigate the periphery of the chip. These buses can transport analog signals from any pin to various analog blocks (including the opamps) and to the CapSense blocks allowing, for instance, the ADC to monitor any pin on the chip. These buses are independent and can also be split into three independent sections. This allows one section to be used for CapSense purposes, one for general analog signal processing, and the third for general-purpose digital peripherals and GPIO.

#### Four Opamps (CTBm Blocks)

The PSoC 4200-L has four opamps with Comparator modes, which allow most common analog functions to be performed on-chip eliminating external components; PGAs, voltage buffers, filters, trans-impedance amplifiers, and other functions can be realized with external passives saving power, cost, and space. The on-chip opamps are designed with enough bandwidth to drive the Sample-and-Hold circuit of the ADC without requiring external buffering. The opamps can operate in the Deep Sleep mode at very low power levels. The following diagram shows one of two identical opamp pairs of the opamp subsystem.

## Figure 5. Identical Opamp Pairs in Opamp Subsystem



The ovals in Figure 5 represent analog switches, which may be controlled via user firmware, the SAR sequencer, or user-defined programmable logic. The opamps (OA0 and OA1) are configurable via these switches to perform all standard opamp functions with appropriate feedback components.

The opamps (OA0 and OA1) are programmable and reconfigurable to provide standard opamp functionality via switchable feedback components, unity gain functionality for driving pins directly, or for internal use (such as buffering SAR ADC inputs as indicated in the diagram), or as true comparators.

The opamp inputs provide highly flexible connectivity and can connect directly to dedicated pins or, via the analog mux buses,

The opamps operate in Deep Sleep mode at very low currents allowing analog circuits to remain operational during Deep Sleep.

#### Temperature Sensor

The PSoC 4200-L has one on-chip temperature sensor. This consists of a diode, which is biased by a current source that can be disabled to save power. The temperature sensor is connected to the ADC, which digitizes the reading and produces a temperature value using Cypress-supplied software that includes calibration and linearization.

#### Low-power Comparators

The PSoC 4200-L has a pair of low-power comparators, which can also operate in the Deep Sleep and Hibernate modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid meta-stability unless operating in an asynchronous power mode (Hibernate) where the system wake-up circuit is activated by a comparator switch event.

## **Programmable Digital**

### Universal Digital Blocks (UDBs) and Port Interfaces

The PSoC 4200-L has eight UDBs; the UDB array also provides a switched Digital System Interconnect (DSI) fabric that allows signals from peripherals and ports to be routed to and through the UDBs for communication and control. The UDB array is shown in the following figure.

#### Figure 6. UDB Array





# Pinouts

The following is the pin list for the PSoC 4200-L.

	124-BGA		68-QFN		64-TQFP	48-TQFP		48-TQFP-USB	
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
H13	P0.0	42	P0.0	39	P0.0	28	P0.0	28	P0.0
H12	P0.1	43	P0.1	40	P0.1	29	P0.1	29	P0.1
G13	P0.2	44	P0.2	41	P0.2	30	P0.2	30	P0.2
G12	P0.3	45	P0.3	42	P0.3	31	P0.3	31	P0.3
K10	VSSD								
G11	P0.4	46	P0.4	43	P0.4	32	P0.4	32	P0.4
F13	P0.5	47	P0.5	44	P0.5	33	P0.5	33	P0.5
F12	P0.6	48	P0.6	45	P0.6	34	P0.6	34	P0.6
F11	P0.7	49	P0.7	46	P0.7	35	P0.7	35	P0.7
E13	P8.0								
E12	P8.1								
E11	P8.2								
D13	P8.3								
D12	P8.4								
C13	P8.5								
C12	P8.6								
B12	P8.7								
C11	XRES	50	XRES	47	XRES	36	XRES	36	XRES
A12	VCCD	51	VCCD	48	VCCD	37	VCCD	37	VCCD
D10	VSSD	52	VSSD	49	VSSD	38	VSSD	38	VSSD
B13	VDDD	53	VDDD	50	VDDD	39	VDDD	39	VDDD
A13	VDDD	53	VDDD	50	VDDD	39	VDDD	39	VDDD
A11	P9.0								
B11	P9.1								
A10	P9.2								
B10	P9.3								
C10	P9.4								
A9	P9.5								
B9	P9.6								
C9	P9.7								
						40	VDDA	40	VDDA
C8	P5.0	54	P5.0	51	P5.0				
B8	P5.1	55	P5.1	52	P5.1				
A8	P5.2	56	P5.2	53	P5.2				
A7	P5.3	57	P5.3	54	P5.3				
B7	P5.4	58	P5.4						
C7	P5.5	59	P5.5	55	P5.5				
A6	P5.6								
B6	P5.7								
A2	VDDA	60	VDDA	56	VDDA	40	VDDA	40	VDDA
B2	VDDA	60	VDDA	56	VDDA	40	VDDA	40	VDDA



	124-BGA		68-QFN		64-TQFP	48-TQFP		48-TQFP-USB	
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
M3	P3.3	22	P3.3	21	P3.3	16	P3.3	16	P3.3
N4	P3.4	23	P3.4	22	P3.4	17	P3.4	17	P3.4
M4	P3.5	24	P3.5	23	P3.5	18	P3.5	18	P3.5
N5	P3.6	25	P3.6	24	P3.6	19	P3.6	19	P3.6
M5	P3.7	26	P3.7	25	P3.7	20	P3.7	20	P3.7
M1	VDDIO	27	VDDIO	26	VDDIO	21	VDDIO	21	VDDIO
N1	VDDIO	27	VDDIO	26	VDDIO	21	VDDIO	21	VDDIO
N6	P11.0								
M6	P11.1								
L6	P11.2								
N7	P11.3								
M7	P11.4								
L7	P11.5								
N8	P11.6								
M8	P11.7								
N12	VDDIO	27	VDDIO	26	VDDIO	21	VDDIO	21	VDDIO
N13	VDDIO	27	VDDIO	26	VDDIO	21	VDDIO	21	VDDIO
L8	P4.0	28	P4.0	27	P4.0	22	P4.0	22	P4.0
N9	P4.1	29	P4.1	28	P4.1	23	P4.1		
M9	P4.2	30	P4.2	29	P4.2	24	P4.2		
N10	P4.3	31	P4.3	30	P4.3	25	P4.3		
M10	P4.4	32	P4.4	31	P4.4				
N11	P4.5	33	P4.5	32	P4.5				
M11	P4.6	34	P4.6	33	P4.6				
M12	P4.7	35	P4.7						
L11	VSSD								
L12	D+/P13.0	36	D+/P13.0	34	D+/P13.0			23	D+/P13.0
L13	D-/P13.1	37	D-/P13.1	35	D-/P13.1			24	D-/P13.1
M13	VBUS/P13.2	38	VBUS/P13.2	36	VBUS/P13.2			25	VBUS/P13.2
L9	P7.0	39	P7.0	37	P7.0	26	P7.0	26	P7.0
L10	P7.1	40	P7.1	38	P7.1	27	P7.1	27	P7.1
K13	P7.2	41	P7.2						
K12	P7.3								
K11	P7.4								
J13	P7.5								
J12	P7.6	1						1	
J11	P7.7								

Port 12 (Port pins 12.0 and 12.1) are SIO pins.

Ports 6 (Port pins P6.0..6.5) and 9 (Port pins 9.0..9.7) are overvoltage tolerant (GPIO\_OVT)

Balls C6, D11, H11, H3, L4, and L5 are No Connects (NC) on the 124-BGA package. Pins 11 and 15 are NC on the 48-TQFP packages.



Port/Pin	Analog	PRGIO & USB	Alt. Function 1	Alt. Function 2	Alt. Function 3	Alt. Function 4	Alt. Function 5
P0.0	lpcomp.in_p[0]				can[1].can_rx:0	usb.vbus_valid	scb[0].spi_select1:3
P0.1	lpcomp.in_n[0]				can[1].can_tx:0		scb[0].spi_select2:3
P0.2	lpcomp.in_p[1]						scb[0].spi_select3:3
P0.3	lpcomp.in_n[1]						
P0.4	wco_in			scb[1].uart_rx:0		scb[1].i2c_scl:0	scb[1].spi_mosi:0
P0.5	wco_out			scb[1].uart_tx:0		scb[1].i2c_sda:0	scb[1].spi_miso:0
P0.6			srss.ext_clk:0	scb[1].uart_cts:0			scb[1].spi_clk:0
P0.7				scb[1].uart_rts:0	can[1].can_tx_enb_ n:0	srss.wakeup	scb[1].spi_select0:0
P8.0				scb[3].uart_rx:0		scb[3].i2c_scl:0	scb[3].spi_mosi:0
P8.1				scb[3].uart_tx:0		scb[3].i2c_sda:0	scb[3].spi_miso:0
P8.2				scb[3].uart_cts:0		lpcomp.comp[0]:0	scb[3].spi_clk:0
P8.3				scb[3].uart_rts:0		lpcomp.comp[1]:0	scb[3].spi_select0:0
P8.4							scb[3].spi_select1:0
P8.5							scb[3].spi_select2:0
P8.6							scb[3].spi_select3:0
P8.7							
P9.0			tcpwm.line[0]:2	scb[0].uart_rx:0		scb[0].i2c_scl:0	scb[0].spi_mosi:0
P9.1			tcpwm.line_compl[0]:2	scb[0].uart_tx:0		scb[0].i2c_sda:0	scb[0].spi_miso:0
P9.2			tcpwm.line[1]:2	scb[0].uart_cts:0			scb[0].spi_clk:0
P9.3			tcpwm.line_compl[1]:2	scb[0].uart_rts:0			scb[0].spi_select0:0
P9.4			tcpwm.line[2]:2				scb[0].spi_select1:0
P9.5			tcpwm.line_compl[2]:2				scb[0].spi_select2:0
P9.6			tcpwm.line[3]:2			scb[3].i2c_scl:3	scb[0].spi_select3:0
P9.7			tcpwm.line_compl[3]:2			scb[3].i2c_sda:3	
P5.0	ctb1_pads[0] csd[1].c_mod		tcpwm.line[4]:2	scb[2].uart_rx:0		scb[2].i2c_scl:0	scb[2].spi_mosi:0
P5.1	ctb1_pads[1] csd[1].c_sh_tank		tcpwm.line_compl[4]:2	scb[2].uart_tx:0		scb[2].i2c_sda:0	scb[2].spi_miso:0
P5.2	ctb1_pads[2] ctb1_oa0_out_10x		tcpwm.line[5]:2	scb[2].uart_cts:0		lpcomp.comp[0]:1	scb[2].spi_clk:0
P5.3	ctb1_pads[3] ctb1_oa1_out_10x		tcpwm.line_compl[5]:2	scb[2].uart_rts:0		lpcomp.comp[1]:1	scb[2].spi_select0:0
P5.4	ctb1_pads[4]		tcpwm.line[6]:2				scb[2].spi_select1:0
P5.5	ctb1_pads[5]		tcpwm.line_compl[6]:2				scb[2].spi_select2:0
P5.6	ctb1_pads[6]		tcpwm.line[7]:2				scb[2].spi_select3:0
P5.7	ctb1_pads[7]		tcpwm.line_compl[7]:2				
P1.0	ctb0_pads[0]		tcpwm.line[2]:1	scb[0].uart_rx:1		scb[0].i2c_scl:1	scb[0].spi_mosi:1
P1.1	ctb0_pads[1]		tcpwm.line_compl[2]:1	scb[0].uart_tx:1		scb[0].i2c_sda:1	scb[0].spi_miso:1
P1.2	ctb0_pads[2] ctb0_oa0_out_10x		tcpwm.line[3]:1	scb[0].uart_cts:1			scb[0].spi_clk:1
P1.3	ctb0_pads[3] ctb0_oa1_out_10x		tcpwm.line_compl[3]:1	scb[0].uart_rts:1			scb[0].spi_select0:1
P1.4	ctb0_pads[4]		tcpwm.line[6]:1				scb[0].spi_select1:1

Each of the pins shown in the previous table can have multiple programmable functions as shown in the following table.



Port/Pin	Analog	PRGIO & USB	Alt. Function 1	Alt. Function 2	Alt. Function 3	Alt. Function 4	Alt. Function 5
P1.5	ctb0_pads[5]		tcpwm.line_compl[6]:1				scb[0].spi_select2:1
P1.6	ctb0_pads[6]		tcpwm.line[7]:1				scb[0].spi_select3:1
P1.7	ctb0_pads[7], sar_ext_vref		tcpwm.line_compl[7]:1				
P2.0	sarmux_pads[0]		tcpwm.line[4]:1	scb[1].uart_rx:1		scb[1].i2c_scl:1	scb[1].spi_mosi:1
P2.1	sarmux_pads[1]		tcpwm.line_compl[4]:1	scb[1].uart_tx:1		scb[1].i2c_sda:1	scb[1].spi_miso:1
P2.2	sarmux_pads[2]		tcpwm.line[5]:1	scb[1].uart_cts:1			scb[1].spi_clk:1
P2.3	sarmux_pads[3]		tcpwm.line_compl[5]:1	scb[1].uart_rts:1			scb[1].spi_select0:1
P2.4	sarmux_pads[4]		tcpwm.line[0]:1				scb[1].spi_select1:0
P2.5	sarmux_pads[5]		tcpwm.line_compl[0]:1				scb[1].spi_select2:0
P2.6	sarmux_pads[6]		tcpwm.line[1]:1				scb[1].spi_select3:0
P2.7	sarmux_pads[7]		tcpwm.line_compl[1]:1				
P10.0				scb[2].uart_rx:1		scb[2].i2c_scl:1	scb[2].spi_mosi:1
P10.1				scb[2].uart_tx:1		scb[2].i2c_sda:1	scb[2].spi_miso:1
P10.2				scb[2].uart_cts:1			scb[2].spi_clk:1
P10.3				scb[2].uart_rts:1			scb[2].spi_select0:1
P10.4							scb[2].spi_select1:1
P10.5							scb[2].spi_select2:1
P10.6							scb[2].spi_select3:1
P10.7							
P6.0			tcpwm.line[4]:0	scb[3].uart_rx:1	can[0].can_tx_enb_ n:0	scb[3].i2c_scl:1	scb[3].spi_mosi:1
P6.1			tcpwm.line_compl[4]:0	scb[3].uart_tx:1	can[0].can_rx:0	scb[3].i2c_sda:1	scb[3].spi_miso:1
P6.2			tcpwm.line[5]:0	scb[3].uart_cts:1	can[0].can_tx:0	scb[2].i2c_scl:3	scb[3].spi_clk:1
P6.3			tcpwm.line_compl[5]:0	scb[3].uart_rts:1		scb[2].i2c_sda:3	scb[3].spi_select0:1
P6.4			tcpwm.line[6]:0			scb[0].i2c_scl:3	scb[3].spi_select1:1
P12.0			tcpwm.line[7]:0			scb[1].i2c_scl:3	scb[3].spi_select3:1
P12.1			tcpwm.line_compl[7]:0			scb[1].i2c_sda:3	
P6.5			tcpwm.line_compl[6]:0			scb[0].i2c_sda:3	scb[3].spi_select2:1
P3.0			tcpwm.line[0]:0	scb[1].uart_rx:2		scb[1].i2c_scl:2	scb[1].spi_mosi:2
P3.1			tcpwm.line_compl[0]:0	scb[1].uart_tx:2		scb[1].i2c_sda:2	scb[1].spi_miso:2
P3.2			tcpwm.line[1]:0	scb[1].uart_cts:2		cpuss.swd_data:0	scb[1].spi_clk:2
P3.3			tcpwm.line_compl[1]:0	scb[1].uart_rts:2		cpuss.swd_clk:0	scb[1].spi_select0:2
P3.4			tcpwm.line[2]:0				scb[1].spi_select1:1
P3.5			tcpwm.line_compl[2]:0				scb[1].spi_select2:1
P3.6			tcpwm.line[3]:0				scb[1].spi_select3:1
P3.7			tcpwm.line_compl[3]:0				
P11.0		prgio[0].io[0]	tcpwm.line[4]:3	scb[2].uart_rx:2		scb[2].i2c_scl:2	scb[2].spi_mosi:2
P11.1		prgio[0].io[1]	tcpwm.line_compl[4]:3	scb[2].uart_tx:2		scb[2].i2c_sda:2	scb[2].spi_miso:2
P11.2		prgio[0].io[2]	tcpwm.line[5]:3	scb[2].uart_cts:2		cpuss.swd_data:1	scb[2].spi_clk:2
P11.3		prgio[0].io[3]	tcpwm.line_compl[5]:3	scb[2].uart_rts:2		cpuss.swd_clk:1	scb[2].spi_select0:2
P11.4		prgio[0].io[4]	tcpwm.line[6]:3				scb[2].spi_select1:2
P11.5		prgio[0].io[5]	tcpwm.line_compl[6]:3				scb[2].spi_select2:2
P11.6		prgio[0].io[6]	tcpwm.line[7]:3				scb[2].spi_select3:2
P11.7		prgio[0].io[7]	tcpwm.line_compl[7]:3				
P4.0				scb[0].uart_rx:2	can[0].can_rx:1	scb[0].i2c_scl:2	scb[0].spi_mosi:2
P4.1				scb[0].uart_tx:2	can[0].can_tx:1	scb[0].i2c_sda:2	scb[0].spi_miso:2



# **Development Support**

The PSoC 4200-L family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit www.cypress.com/go/psoc4 to find out more.

### Documentation

A suite of documentation supports the PSoC 4200-L family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

**Software User Guide**: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

**Component Datasheets**: The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

**Application Notes**: PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

**Technical Reference Manual**: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers.

#### Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

#### Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 4200-L family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.



# **Electrical Specifications**

## **Absolute Maximum Ratings**

### Table 1. Absolute Maximum Ratings<sup>[1]</sup>

Spec ID#	Parameter	Description	Min	Тур	Мах	Units	Details/ Conditions
SID1	V <sub>DD_ABS</sub>	Analog or digital supply relative to $V_{SS}$ ( $V_{SSD} = V_{SSA}$ )	-0.5	-	6	V	Absolute maximum
SID2	V <sub>CCD_ABS</sub>	Direct digital core voltage input relative to $V_{SSD}$	-0.5	-	1.95	V	Absolute maximum
SID3	V <sub>GPIO_ABS</sub>	GPIO voltage; V <sub>DDD</sub> or V <sub>DDA</sub>	-0.5	-	V <sub>DD</sub> +0.5	V	Absolute maximum
SID4	I <sub>GPIO_ABS</sub>	Current per GPIO	-25	-	25	mA	Absolute maximum
SID5	I <sub>G-PIO_injection</sub>	GPIO injection current per pin	-0.5	-	0.5	mA	Absolute maximum
BID44	ESD_HBM	Electrostatic discharge human body model	2200	-	-	V	
BID45	ESD_CDM	Electrostatic discharge charged device model	500	-	-	V	
BID46	LU	Pin current for latch-up	-140	-	140	mA	

## **Device Level Specifications**

All specifications are valid for -40 °C  $\leq$  TA  $\leq$  85 °C and TJ  $\leq$  100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

#### Table 2. DC Specifications

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details / Conditions
SID53	V <sub>DDD</sub>	Power Supply Input Voltage ( $V_{DDA} = V_{DDD} = V_{DD}$ )	1.8	-	5.5	V	With regulator enabled
SID255	V <sub>DDD</sub>	Power supply input voltage unregulated	1.71	1.8	1.89	V	Internally unregu- lated Supply
SID54	V <sub>CCD</sub>	Output voltage (for core logic)	-	1.8	-	V	
SID55	C <sub>EFC</sub>	External regulator voltage bypass	1	1.3	1.6	μF	X5R ceramic or better
SID56	C <sub>EXC</sub>	Power supply decoupling capacitor	_	1	-	μF	X5R ceramic or better
Active Mode							·
SID6	I <sub>DD1</sub>	Execute from flash; CPU at 6 MHz	_	2.2	3.1	mA	
SID7	I <sub>DD2</sub>	Execute from flash; CPU at 12 MHz	_	3.7	4.8	mA	
SID8	I <sub>DD3</sub>	Execute from flash; CPU at 24 MHz	_	6.7	8.0	mA	
SID9	I <sub>DD4</sub>	Execute from flash; CPU at 48 MHz	_	12.8	14.5	mA	
Sleep Mode							
SID21	I <sub>DD16</sub>	I <sup>2</sup> C wakeup, WDT, and Comparators on. Regulator Off.	_	1.8	2.2	mA	V <sub>DD</sub> = 1.71 to 1.89, 6 MHz
SID22	I <sub>DD17</sub>	I <sup>2</sup> C wakeup, WDT, and Comparators on.	-	1.7	2.1	mA	V <sub>DD</sub> = 1.8 to 5.5, 6 MHz

Note

Usage above the absolute maximum conditions listed in Table 1 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.



## Table 2. DC Specifications

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details / Conditions
SID23	I <sub>DD18</sub>	I <sup>2</sup> C wakeup, WDT, and Comparators on. Regulator Off.	-	2.4	2.9	mA	V <sub>DD</sub> = 1.71 to 1.89, 12 MHz
SID24	I <sub>DD19</sub>	I <sup>2</sup> C wakeup, WDT, and Comparators on.	_	2.3	2.8	mA	V <sub>DD</sub> = 1.8 to 5.5, 12 MHz
Deep Sleep I	Mode, –40 °C to	+ 60 °C					
SID30	I <sub>DD25</sub>	I <sup>2</sup> C wakeup and WDT on. Regulator Off.	-	-	13.5	μA	V <sub>DD</sub> = 1.71 to 1.89
SID31	I <sub>DD26</sub>	I <sup>2</sup> C wakeup and WDT on.	-	1.3	20.0	μA	V <sub>DD</sub> = 1.8 to 3.6
SID32	I <sub>DD27</sub>	I <sup>2</sup> C wakeup and WDT on.	-	-	20.0	μA	V <sub>DD</sub> = 3.6 to 5.5
Deep Sleep I	Mode, +85 °C						
SID33	I <sub>DD28</sub>	I <sup>2</sup> C wakeup and WDT on. Regulator Off.	-	-	45.0	μA	V <sub>DD</sub> = 1.71 to 1.89
SID34	I <sub>DD29</sub>	I <sup>2</sup> C wakeup and WDT on.	-	15	60.0	μA	V <sub>DD</sub> = 1.8 to 3.6
SID35	I <sub>DD30</sub>	I <sup>2</sup> C wakeup and WDT on.	-	-	45.0	μA	V <sub>DD</sub> = 3.6 to 5.5
Hibernate Mo	ode, -40 °C to +	60 °C					
SID39	I <sub>DD34</sub>	Regulator Off.	-	-	1123	nA	V <sub>DD</sub> = 1.71 to 1.89
SID40	I <sub>DD35</sub>		-	150	1600	nA	V <sub>DD</sub> = 1.8 to 3.6
SID41	I <sub>DD36</sub>		_	-	1600	nA	V <sub>DD</sub> = 3.6 to 5.5
Hibernate Mo	ode, +85 °C						
SID42	I <sub>DD37</sub>	Regulator Off.	-	-	4142	nA	V <sub>DD</sub> = 1.71 to 1.89
SID43	I <sub>DD38</sub>		_	-	9700	nA	V <sub>DD</sub> = 1.8 to 3.6
SID44	I <sub>DD39</sub>		-	-	10,400	nA	V <sub>DD</sub> = 3.6 to 5.5
Stop Mode							
SID304	I <sub>DD43A</sub>	Stop Mode current; V <sub>DD</sub> = 3.6 V	-	20	659	nA	T = -40 °C to +60 °C
SID304A	I <sub>DD43B</sub>	Stop Mode current; V <sub>DD</sub> = 3.6 V	_	-	1810	nA	T = +85 °C
XRES curren	nt	· · · · ·		•	·		
SID307	I <sub>DD_XR</sub>	Supply current while XRES (Active Low) asserted	_	2	5	mA	

## Table 3. AC Specifications

Spec ID#	Parameter	Description	Min	Тур	Мах	Units	Details/ Conditions
SID48	F <sub>CPU</sub>	CPU frequency	DC	-	48	MHz	$1.71 \leq V_{DD} \leq 5.5$
SID49	T <sub>SLEEP</sub>	Wakeup from sleep mode	-	0	-	μs	Guaranteed by characterization
SID50	T <sub>DEEPSLEEP</sub>	Wakeup from Deep Sleep mode	_	_	25	μs	24-MHz IMO. Guaranteed by characterization
SID51	T <sub>HIBERNATE</sub>	Wakeup from Hibernate mode	_	-	0.7	ms	Guaranteed by characterization
SID51A	T <sub>STOP</sub>	Wakeup from Stop mode	_	-	1.9	ms	Guaranteed by characterization
SID52	T <sub>RESETWIDTH</sub>	External reset pulse width	1	-	_	μs	Guaranteed by characterization



## Table 5. GPIO AC Specifications

(Guaranteed by Characterization)<sup>[3]</sup>

Spec ID#	Parameter	Description	Min	Тур	Мах	Units	Details/ Conditions
SID70	T <sub>RISEF</sub>	Rise time in fast strong mode	2	-	12	ns	3.3 V V <sub>DDD</sub> , Cload = 25 pF
SID71	T <sub>FALLF</sub>	Fall time in fast strong mode	2	-	12	ns	3.3 V V <sub>DDD</sub> , Cload = 25 pF
SID72	T <sub>RISES</sub>	Rise time in slow strong mode	10	-	60	ns	3.3 V V <sub>DDD</sub> , Cload = 25 pF
SID73	T <sub>FALLS</sub>	Fall time in slow strong mode	10	-	60	ns	3.3 V V <sub>DDD</sub> , Cload = 25 pF
SID74	F <sub>GPIOUT1</sub>	GPIO Fout;3.3 V $\leq$ V <sub>DDD</sub> $\leq$ 5.5 V. Fast strong mode.	_	-	33	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID75	F <sub>GPIOUT2</sub>	GPIO Fout;1.7 V $\leq$ V <sub>DDD</sub> $\leq$ 3.3 V. Fast strong mode.	_	-	16.7	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID76	F <sub>GPIOUT3</sub>	GPIO Fout;3.3 V $\leq$ V <sub>DDD</sub> $\leq$ 5.5 V. Slow strong mode.	_	-	7	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID245	F <sub>GPIOUT4</sub>	GPIO Fout;1.7 V $\leq$ V <sub>DDD</sub> $\leq$ 3.3 V. Slow strong mode.	_	-	3.5	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID246	F <sub>GPIOIN</sub>	GPIO input operating frequency; 1.71 V $\leq$ V <sub>DDD</sub> $\leq$ 5.5 V	-	-	48	MHz	90/10% V <sub>IO</sub>

## XRES

## Table 6. XRES DC Specifications

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/ Conditions
SID77	V <sub>IH</sub>	Input voltage high threshold	0.7 × V <sub>DDD</sub>	-	-	V	CMOS Input
SID78	V <sub>IL</sub>	Input voltage low threshold	-	-	0.3 × V <sub>DDD</sub>	V	CMOS Input
SID79	R <sub>PULLUP</sub>	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID80	C <sub>IN</sub>	Input capacitance	-	3	-	pF	
SID81	V <sub>HYSXRES</sub>	Input voltage hysteresis	-	100	_	mV	Guaranteed by characterization
SID82	IDIODE	Current through protection diode to $V_{DDD}/V_{SS}$	_	-	100	μA	Guaranteed by characterization

## Table 7. XRES AC Specifications

Spec ID#	Parameter	Description	Min	Тур	Мах	Units	Details/ Conditions
SID83	T <sub>RESETWIDTH</sub>	Reset pulse width	1	_	_	μs	Guaranteed by characterization

Note

Simultaneous switching transitions on many fully-loaded GPIO pins may cause ground perturbations depending on several factors including PCB and decoupling capacitor design. For applications that are very sensitive to ground perturbations, the slower GPIO slew rate setting may be used.



# Table 10. Comparator AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Тур	Max	Units	<b>Details/Conditions</b>
SID91	T <sub>RESP1</sub>	Response time, normal mode	-	38	110	ns	50-mV overdrive
SID258	T <sub>RESP2</sub>	Response time, low power mode	-	70	200	ns	50-mV overdrive
SID92	T <sub>RESP3</sub>	Response time, ultra low power mode	-	2.3	15	μs	200-mV overdrive. $V_{DDD} \ge 2.2 V \text{ for}$ Temp < 0 °C, $V_{DDD} \ge$ 1.8 V for Temp > 0 °C

#### Temperature Sensor

## Table 11. Temperature Sensor Specifications

Spec ID#	Parameter	Description	Min	Тур	Max	Units	<b>Details/Conditions</b>
SID93	T <sub>SENSACC</sub>	Temperature sensor accuracy	-5	±1	+5	°C	–40 to +85 °C

SAR ADC

## Table 12. SAR ADC DC Specifications

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID94	A_RES	Resolution	-	-	12	bits	
SID95	A_CHNIS_S	Number of channels - single ended	-	_	16		8 full speed
SID96	A-CHNKS_D	Number of channels - differential	_	-	8		Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity	_	-	-		Yes. Based on characterization
SID98	A_GAINERR	Gain error	-	-	±0.1	%	With external reference.
SID99	A_OFFSET	Input offset voltage	_	-	2	mV	Measured with 1-V V <sub>REF.</sub>
SID100	A_ISAR	Current consumption	-	-	1	mA	
SID101	A_VINS	Input voltage range - single ended	V <sub>SS</sub>	-	V <sub>DDA</sub>	V	Based on device characterization
SID102	A_VIND	Input voltage range - differential	$V_{SS}$	-	V <sub>DDA</sub>	V	Based on device characterization
SID103	A_INRES	Input resistance	-	-	2.2	KΩ	Based on device characterization
SID104	A_INCAP	Input capacitance	_	-	10	pF	Based on device characterization

## Table 13. SAR ADC AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID106	A_PSRR	Power supply rejection ratio	70	-	-	dB	
SID107	A_CMRR	Common mode rejection ratio	66	-	-	dB	Measured at 1 V
SID108	A_SAMP_1	Sample rate with external reference bypass cap	-	-	1	Msps	
SID108A	A_SAMP_2	Sample rate with no bypass cap. Reference = V <sub>DD</sub>	-	-	500	Ksps	



## LCD Direct Drive

# Table 18. LCD Direct Drive DC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID154	ILCDLOW	Operating current in low power mode	_	5	_	μA	16 × 4 small segment disp. at 50 Hz
SID155	C <sub>LCDCAP</sub>	LCD capacitance per segment/common driver	_	500	5000	pF	Guaranteed by Design
SID156	LCD <sub>OFFSET</sub>	Long-term segment offset	_	20	_	mV	
SID157	I <sub>LCDOP1</sub>	PWM Mode current. 5-V bias. 24-MHz IMO	_	0.6	-	mA	32 × 4 segments. 50 Hz, 25 °C
SID158	I <sub>LCDOP2</sub>	PWM Mode current. 3.3-V bias. 24-MHz IMO.	-	0.5	-	mA	32 × 4 segments. 50 Hz, 25 °C

# Table 19. LCD Direct Drive AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Тур	Max	Units	<b>Details/Conditions</b>
SID159	F <sub>LCD</sub>	LCD frame rate	10	50	150	Hz	

## Table 20. Fixed UART DC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID160	I <sub>UART1</sub>	Block current consumption at 100 Kbits/sec	-	9	55	μA	
SID161	I <sub>UART2</sub>	Block current consumption at 1000 Kbits/sec	-	-	312	μA	

## Table 21. Fixed UART AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID162	F <sub>UART</sub>	Bit rate	_	-	1	Mbps	



# Memory

## Table 26. Flash DC Specifications

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID173	V <sub>PE</sub>	Erase and program voltage	1.71	Ι	5.5	V	

## Table 27. Flash AC Specifications

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID174	T <sub>ROWWRITE</sub>	Row (block) write time (erase and program)	-	_	20	ms	Row (block) = 256 bytes
SID175	T <sub>ROWERASE</sub>	Row erase time	-	_	13	ms	
SID176	T <sub>ROWPROGRAM</sub>	Row program time after erase	-	-	7	ms	
SID178	T <sub>BULKERASE</sub>	Bulk erase time (128 KB)	-	-	35	ms	
SID180	T <sub>DEVPROG</sub>	Total device program time	-	_	15	seconds	Guaranteed by charac- terization
SID181	F <sub>END</sub>	Flash endurance	100 K	_	_	cycles	Guaranteed by charac- terization
SID182	F <sub>RET</sub>	Flash retention. $T_A \le 55 \text{ °C}$ , 100 K P/E cycles	20	_	-	years	Guaranteed by charac- terization
SID182A		Flash retention. $T_A \le 85$ °C, 10 K P/E cycles	10	-	-	years	Guaranteed by charac- terization



## SWD Interface

## Table 32. SWD Interface Specifications

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID213	F_SWDCLK1	$3.3~V \leq V_{DD} \leq 5.5~V$	-	-	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID214	F_SWDCLK2	$1.71~V \leq V_{DD} \leq 3.3~V$	-	-	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID215	T_SWDI_SETUP	T = 1/f SWDCLK	0.25*T	-	-	ns	Guaranteed by characterization
SID216	T_SWDI_HOLD	T = 1/f SWDCLK	0.25*T	-	-	ns	Guaranteed by characterization
SID217	T_SWDO_VALID	T = 1/f SWDCLK	-	-	0.5*T	ns	Guaranteed by characterization
SID217A	T_SWDO_HOLD	T = 1/f SWDCLK	1	-	_	ns	Guaranteed by characterization

Internal Main Oscillator

## Table 33. IMO DC Specifications

(Guaranteed by Design)

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID218	I <sub>IMO1</sub>	IMO operating current at 48 MHz	_	-	1000	μA	
SID219	I <sub>IMO2</sub>	IMO operating current at 24 MHz	-	-	325	μA	
SID220	I <sub>IMO3</sub>	IMO operating current at 12 MHz	_	-	225	μA	
SID221	I <sub>IMO4</sub>	IMO operating current at 6 MHz	-	-	180	μA	
SID222	I <sub>IMO5</sub>	IMO operating current at 3 MHz	_	_	150	μA	

#### Table 34. IMO AC Specifications

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID223	F <sub>IMOTOL1</sub>	Frequency variation from 3 to 48 MHz	-	-	±2	%	
SID226	T <sub>STARTIMO</sub>	IMO startup time	-	-	12	μs	
SID227	T <sub>JITRMSIMO1</sub>	RMS Jitter at 3 MHz	-	156	-	ps	
SID228	T <sub>JITRMSIMO2</sub>	RMS Jitter at 24 MHz	-	145	-	ps	
SID229	T <sub>JITRMSIMO3</sub>	RMS Jitter at 48 MHz	-	139	-	ps	

Internal Low-Speed Oscillator

# Table 35. ILO DC Specifications

(Guaranteed by Design)

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID231	I <sub>ILO1</sub>	ILO operating current at 32 kHz	-	0.3	1.05	μA	Guaranteed by Characterization
SID233	IILOLEAK	ILO leakage current	_	2	15	nA	Guaranteed by Design



## Table 36. ILO AC Specifications

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID234	T <sub>STARTILO1</sub>	ILO startup time	-	-	2	ms	Guaranteed by charac- terization
SID236	T <sub>ILODUTY</sub>	ILO duty cycle	40	50	60	%	Guaranteed by charac- terization
SID237	F <sub>ILOTRIM1</sub>	32 kHz trimmed frequency	15	32	50	kHz	±60% with trim.

#### Table 37. PLL DC Specifications

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID410	IDD_PLL_48	In = 3 MHz, Out = 48 MHz	-	530	610	μΑ	
SID411	IDD_PLL_24	In = 3 MHz, Out = 24 MHz	-	300	405	μΑ	

## Table 38. PLL AC Specifications

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID412	F <sub>PLLIN</sub>	PLL input frequency	1	-	48	MHz	
SID413	F <sub>PLLINT</sub>	PLL intermediate frequency; prescaler out	1	-	3	MHz	
SID414	F <sub>PLLVCO</sub>	VCO output frequency before post-divide	22.5	-	104	MHz	
SID415	D <sub>IVVCO</sub>	VCO Output post-divider range; PLL output frequency is F <sub>PPLVCO</sub> /D <sub>IVVCO</sub>	1	-	8	-	
SID416	PLLlocktime	Lock time at startup	-	-	250	us	
SID417	Jperiod_1	Period jitter for VCO ≥ 67 MHz	-	-	150	ps	Guaranteed By Design
SID416A	Jperiod_2	Period jitter for VCO ≤ 67 MHz	_	_	200	ps	Guaranteed By Design

### Table 39. External Clock Specifications

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID305	ExtClkFreq	External Clock input Frequency	0	-	48	MHz	Guaranteed by characterization
SID306	ExtClkDuty	Duty cycle; Measured at V <sub>DD/2</sub>	45	-	55	%	Guaranteed by characterization

### Table 40. Watch Crystal Oscillator (WCO) Specifications

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details / Conditions	
IMO WCO-	MO WCO-PLL calibrated mode							
SID330	IMOWCO1	Frequency variation with IMO set to 3 MHz	-0.6	_	0.6	%	Does not include WCO tolerance	
SID331	IMOWCO2	Frequency variation with IMO set to 5 MHZ	-0.4	-	0.4	%	Does not include WCO tolerance	
SID332	IMOWCO3	Frequency variation with IMO set to 7 or 9 MHZ	-0.3	-	0.3	%	Does not include WCO tolerance	
SID333	IMOWCO4	All other IMO frequency settings	-0.2	-	0.2	%	Does not include WCO tolerance	



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The nomenciature used in	Ianie 4X is nasen	on the following	nart numnering	convention.
		on the following	part numbering	convention.

Field	Description	Values	Meaning
CY8C	Cypress Prefix		
4	Architecture	4	PSoC 4
A	Family	2	4200 Family
В	CPU Speed	4	48 MHz
С	Flash Capacity	6	64 KB
		7	128 KB
		8	256 KB
DE	Package Code	AX, AZ	TQFP
		LT	QFN
		BU	BGA
		FD	CSP
F	Temperature Range	1	Industrial
S	Silicon Family	N/A	PSoC 4A
		L	PSoC 4A-L
		BL	PSoC 4A-BLE
XYZ	Attributes Code	000-999	Code of feature set in the specific family

## Part Numbering Conventions

The part number fields are defined as follows.





# Acronyms

#### Table 52. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus archi- tecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge

#### Table 52. Acronyms Used in this Document (continued)

Acronym	Description
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I <sup>2</sup> C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD



## Table 52. Acronyms Used in this Document (continued)

Acronym	Description
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC <sup>®</sup>	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I <sup>2</sup> C serial clock
SDA	I <sup>2</sup> C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol

#### Table 52. Acronyms Used in this Document (continued)

Acronym	Description
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
ТΧ	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal



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