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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, LCD, LVD, POR, PWM, SmartSense, WDT
Number of I/O	53
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b SAR; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4248azi-l485

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article KBA86521, How to Design with PSoC 3, PSoC 4, and PSoC 5LP. Following is an abbreviated list for PSoC 4:

- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: PSoC 1, PSoC 3, PSoC 4, PSoC 5LP
  In addition, PSoC Creator includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 4 are:
  - AN79953: Getting Started With PSoC 4
  - AN88619: PSoC 4 Hardware Design Considerations
  - AN86439: Using PSoC 4 GPIO Pins
  - AN57821: Mixed Signal Circuit Board Layout
  - AN81623: Digital Design Best Practices
  - AN73854: Introduction To Bootloaders
  - AN89610: ARM Cortex Code Optimization
- Technical Reference Manual (TRM) is in two documents:
  - Architecture TRM details each PSoC 4 functional block.
  - Registers TRM describes each of the PSoC 4 registers.
- Development Kits:
  - CY8CKIT-042, PSoC 4 Pioneer Kit, is an easy-to-use and inexpensive development platform. This kit includes connectors for Arduino™ compatible shields and Digilent® Pmod™ daughter cards.
  - CY8CKIT-049 is a very low-cost prototyping platform. It is a low-cost alternative to sampling PSoC 4 devices.
  - CY8CKIT-001 is a common development platform for any one of the PSoC 1, PSoC 3, PSoC 4, or PSoC 5LP families of devices.

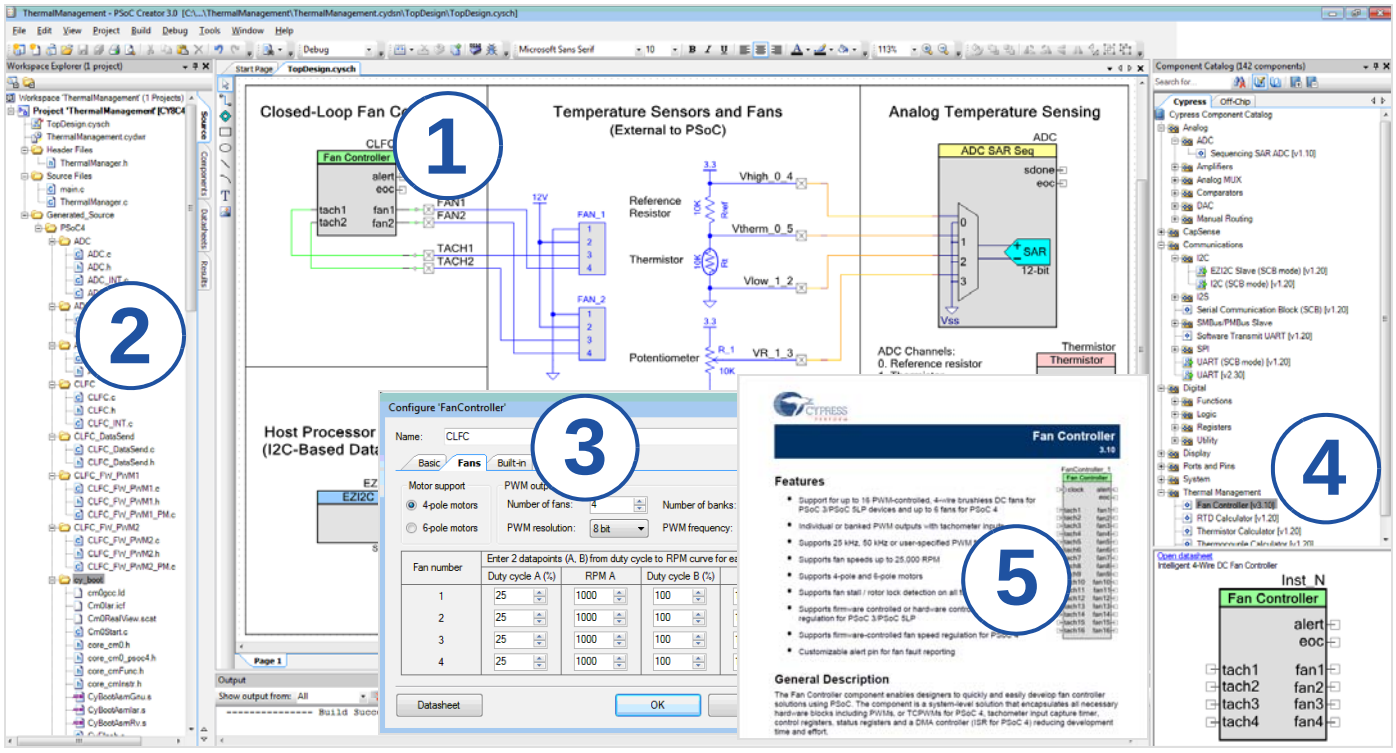
The MiniProg3 device provides an interface for flash programming and debug.

PSoC Creator

PSoC Creator is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the list of component datasheets. With PSoC Creator, you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

Figure 1. Multiple-Sensor Example Project in PSoC Creator Contents

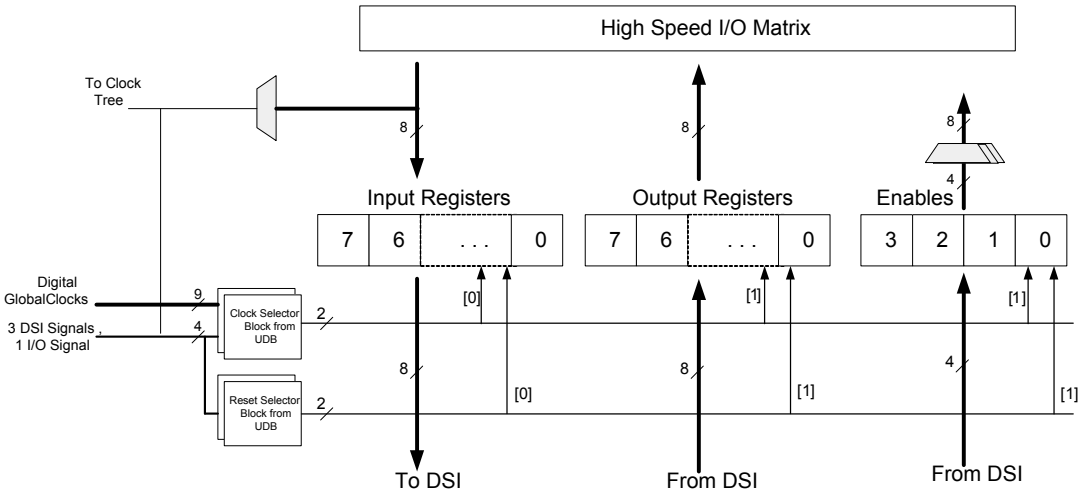


UDBs can be clocked from a clock divider block, from a port interface (required for peripherals such as SPI), and from the DSI network directly or after synchronization.

A port interface is defined, which acts as a register that can be clocked with the same source as the PLDs inside the UDB array. This allows faster operation because the inputs and outputs can be registered at the port interface close to the I/O pins and at the edge of the array. The port interface registers can be clocked by one of the I/Os from the same port. This allows interfaces such as SPI to operate at higher clock speeds by eliminating the delay for the port input to be routed over DSI and used to register other inputs. The port interface is shown in Figure 7.

The UDBs can generate interrupts (one UDB at a time) to the interrupt controller. The UDBs retain the ability to connect to any pin on the chip through the DSI.

Figure 7. Port Interface



Fixed Function Digital

Timer/Counter/PWM (TCPWM) Block

The TCPWM block consists of four 16-bit counters with user-programmable period length. There is a Capture register to record the count value at the time of an event (which may be an I/O event), a period register which is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals, which are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as deadband programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an overcurrent state is indicated and the PWMs driving the FETs need to be shut off immediately with no time for software intervention. The PSoC 4200-L has eight TCPWM blocks.

Serial Communication Blocks (SCB)

The PSoC 4200-L has four SCBs, which can each implement an I^{2}C, UART, or SPI interface.

I^{2}C Mode: The hardware I^{2}C block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EzI2C that creates a mailbox address range in the memory of the PSoC 4200-L and effectively reduces I^{2}C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time. The FIFO mode is available in all channels and is very useful in the absence of DMA.

The I^{2}C peripheral is compatible with the I^{2}C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I^{2}C-bus specification and user manual (UM10204). The I^{2}C bus I/O is implemented with GPIO in open-drain modes.

UART Mode: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

SPI Mode: The SPI mode supports full Motorola SPI, TI SSP (essentially adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO.

USB Device

A Full-speed USB 2.0 device interface is provided. It has a Control endpoint and eight other endpoints. The interface has a USB transceiver and can be operated from the IMO obviating the need for a crystal oscillator.

CAN Blocks

There are two independent CAN 2.0B blocks, which are certified CAN conformant.

GPIO

The PSoC 4200-L has 96 GPIOs. The GPIO block implements the following:

- Eight drive strength modes including strong push-pull, resistive pull-up and pull-down, weak (resistive) pull-up and pull-down, open drain and open source, input only, and disabled
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output disables
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode and Hibernate modes)
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals are also fixed to reduce internal multiplexing complexity (these signals do not go through the DSI network). DSI signals are not affected by this and any pin may be routed to any UDB through the DSI network.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (13 for PSoC 4200-L).

There are 14 GPIO pins that are overvoltage tolerant (V_{IN} can exceed V_{DD}). The overvoltage cells will not sink more than 10 µA when their inputs exceed V_{DDIO} in compliance with I^2C specifications. Meeting the I^2C minimum fall time requirement for FM and FM+ may require the slower slew rate setting depending on bus loading (also applies to all GPIO and SIO pins).

SIO

The Special I/O (SIO) pins have the following features in addition to the GPIO features:

- Overvoltage protection and hot swap capability
- Programmable switching thresholds
- Programmable output pull-up voltage capability

They allow interfacing to buses, such as I^2C with full I^2C compatibility and interfacing to devices operating at different voltage levels. There are two SIO pins on the PSoC4200-L.

Special Function Peripherals

LCD Segment Drive

The PSoC 4200-L has an LCD controller, which can drive up to eight commons and up to 56 segments. Any pin can be either a common or a segment pin. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as digital correlation and PWM.

Digital correlation pertains to modulating the frequency and levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays.

PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep refreshing a small display buffer (4 bits; 1 32-bit register per port).

CapSense

CapSense is supported on all pins in the PSoC 4200-L through two CapSense Sigma-Delta (CSD) blocks that can be connected to any pin through an analog mux bus that any GPIO pin can be connected to via an Analog switch. CapSense function can thus be provided on any pin or group of pins in a system under software control. A component is provided for the CapSense block to make it easy for the user.

Shield voltage can be driven on another Mux Bus to provide water tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input.

Each CapSense block has two IDACs which can be used for general purposes if CapSense is not being used.(both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available). The two CapSense blocks can be used independently.

Pinouts

The following is the pin list for the PSoC 4200-L.

124-BGA		68-QFN		64-TQFP		48-TQFP		48-TQFP-USB	
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
H13	P0.0	42	P0.0	39	P0.0	28	P0.0	28	P0.0
H12	P0.1	43	P0.1	40	P0.1	29	P0.1	29	P0.1
G13	P0.2	44	P0.2	41	P0.2	30	P0.2	30	P0.2
G12	P0.3	45	P0.3	42	P0.3	31	P0.3	31	P0.3
K10	VSSD								
G11	P0.4	46	P0.4	43	P0.4	32	P0.4	32	P0.4
F13	P0.5	47	P0.5	44	P0.5	33	P0.5	33	P0.5
F12	P0.6	48	P0.6	45	P0.6	34	P0.6	34	P0.6
F11	P0.7	49	P0.7	46	P0.7	35	P0.7	35	P0.7
E13	P8.0								
E12	P8.1								
E11	P8.2								
D13	P8.3								
D12	P8.4								
C13	P8.5								
C12	P8.6								
B12	P8.7								
C11	XRES	50	XRES	47	XRES	36	XRES	36	XRES
A12	VCCD	51	VCCD	48	VCCD	37	VCCD	37	VCCD
D10	VSSD	52	VSSD	49	VSSD	38	VSSD	38	VSSD
B13	VDDD	53	VDDD	50	VDDD	39	VDDD	39	VDDD
A13	VDDD	53	VDDD	50	VDDD	39	VDDD	39	VDDD
A11	P9.0								
B11	P9.1								
A10	P9.2								
B10	P9.3								
C10	P9.4								
A9	P9.5								
B9	P9.6								
C9	P9.7								
						40	VDDA	40	VDDA
C8	P5.0	54	P5.0	51	P5.0				
B8	P5.1	55	P5.1	52	P5.1				
A8	P5.2	56	P5.2	53	P5.2				
A7	P5.3	57	P5.3	54	P5.3				
B7	P5.4	58	P5.4						
C7	P5.5	59	P5.5	55	P5.5				
A6	P5.6								
B6	P5.7								
A2	VDDA	60	VDDA	56	VDDA	40	VDDA	40	VDDA
B2	VDDA	60	VDDA	56	VDDA	40	VDDA	40	VDDA

124-BGA		68-QFN		64-TQFP		48-TQFP		48-TQFP-USB	
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
M3	P3.3	22	P3.3	21	P3.3	16	P3.3	16	P3.3
N4	P3.4	23	P3.4	22	P3.4	17	P3.4	17	P3.4
M4	P3.5	24	P3.5	23	P3.5	18	P3.5	18	P3.5
N5	P3.6	25	P3.6	24	P3.6	19	P3.6	19	P3.6
M5	P3.7	26	P3.7	25	P3.7	20	P3.7	20	P3.7
M1	VDDIO	27	VDDIO	26	VDDIO	21	VDDIO	21	VDDIO
N1	VDDIO	27	VDDIO	26	VDDIO	21	VDDIO	21	VDDIO
N6	P11.0								
M6	P11.1								
L6	P11.2								
N7	P11.3								
M7	P11.4								
L7	P11.5								
N8	P11.6								
M8	P11.7								
N12	VDDIO	27	VDDIO	26	VDDIO	21	VDDIO	21	VDDIO
N13	VDDIO	27	VDDIO	26	VDDIO	21	VDDIO	21	VDDIO
L8	P4.0	28	P4.0	27	P4.0	22	P4.0	22	P4.0
N9	P4.1	29	P4.1	28	P4.1	23	P4.1		
M9	P4.2	30	P4.2	29	P4.2	24	P4.2		
N10	P4.3	31	P4.3	30	P4.3	25	P4.3		
M10	P4.4	32	P4.4	31	P4.4				
N11	P4.5	33	P4.5	32	P4.5				
M11	P4.6	34	P4.6	33	P4.6				
M12	P4.7	35	P4.7						
L11	VSSD								
L12	D+/P13.0	36	D+/P13.0	34	D+/P13.0			23	D+/P13.0
L13	D-/P13.1	37	D-/P13.1	35	D-/P13.1			24	D-/P13.1
M13	VBUS/P13.2	38	VBUS/P13.2	36	VBUS/P13.2			25	VBUS/P13.2
L9	P7.0	39	P7.0	37	P7.0	26	P7.0	26	P7.0
L10	P7.1	40	P7.1	38	P7.1	27	P7.1	27	P7.1
K13	P7.2	41	P7.2						
K12	P7.3								
K11	P7.4								
J13	P7.5								
J12	P7.6								
J11	P7.7								

Port 12 (Port pins 12.0 and 12.1) are SIO pins.

Ports 6 (Port pins P6.0..6.5) and 9 (Port pins 9.0..9.7) are overvoltage tolerant (GPIO_OVT)

Balls C6, D11, H11, H3, L4, and L5 are No Connects (NC) on the 124-BGA package. Pins 11 and 15 are NC on the 48-TQFP packages.

Port/Pin	Analog	PRGIO & USB	Alt. Function 1	Alt. Function 2	Alt. Function 3	Alt. Function 4	Alt. Function 5
P1.5	ctb0_pads[5]		tcpwm.line_compl[6]:1				scb[0].spi_select2:1
P1.6	ctb0_pads[6]		tcpwm.line[7]:1				scb[0].spi_select3:1
P1.7	ctb0_pads[7], sar_ext_vref		tcpwm.line_compl[7]:1				
P2.0	sarmux_pads[0]		tcpwm.line[4]:1	scb[1].uart_rx:1		scb[1].i2c_scl:1	scb[1].spi_mosi:1
P2.1	sarmux_pads[1]		tcpwm.line_compl[4]:1	scb[1].uart_tx:1		scb[1].i2c_sda:1	scb[1].spi_miso:1
P2.2	sarmux_pads[2]		tcpwm.line[5]:1	scb[1].uart_cts:1			scb[1].spi_clk:1
P2.3	sarmux_pads[3]		tcpwm.line_compl[5]:1	scb[1].uart_rts:1			scb[1].spi_select0:1
P2.4	sarmux_pads[4]		tcpwm.line[0]:1				scb[1].spi_select1:0
P2.5	sarmux_pads[5]		tcpwm.line_compl[0]:1				scb[1].spi_select2:0
P2.6	sarmux_pads[6]		tcpwm.line[1]:1				scb[1].spi_select3:0
P2.7	sarmux_pads[7]		tcpwm.line_compl[1]:1				
P10.0				scb[2].uart_rx:1		scb[2].i2c_scl:1	scb[2].spi_mosi:1
P10.1				scb[2].uart_tx:1		scb[2].i2c_sda:1	scb[2].spi_miso:1
P10.2				scb[2].uart_cts:1			scb[2].spi_clk:1
P10.3				scb[2].uart_rts:1			scb[2].spi_select0:1
P10.4							scb[2].spi_select1:1
P10.5							scb[2].spi_select2:1
P10.6							scb[2].spi_select3:1
P10.7							
P6.0			tcpwm.line[4]:0	scb[3].uart_rx:1	can[0].can_tx_enb_n:0	scb[3].i2c_scl:1	scb[3].spi_mosi:1
P6.1			tcpwm.line_compl[4]:0	scb[3].uart_tx:1	can[0].can_rx:0	scb[3].i2c_sda:1	scb[3].spi_miso:1
P6.2			tcpwm.line[5]:0	scb[3].uart_cts:1	can[0].can_tx:0	scb[2].i2c_scl:3	scb[3].spi_clk:1
P6.3			tcpwm.line_compl[5]:0	scb[3].uart_rts:1		scb[2].i2c_sda:3	scb[3].spi_select0:1
P6.4			tcpwm.line[6]:0			scb[0].i2c_scl:3	scb[3].spi_select1:1
P12.0			tcpwm.line[7]:0			scb[1].i2c_scl:3	scb[3].spi_select3:1
P12.1			tcpwm.line_compl[7]:0			scb[1].i2c_sda:3	
P6.5			tcpwm.line_compl[6]:0			scb[0].i2c_sda:3	scb[3].spi_select2:1
P3.0			tcpwm.line[0]:0	scb[1].uart_rx:2		scb[1].i2c_scl:2	scb[1].spi_mosi:2
P3.1			tcpwm.line_compl[0]:0	scb[1].uart_tx:2		scb[1].i2c_sda:2	scb[1].spi_miso:2
P3.2			tcpwm.line[1]:0	scb[1].uart_cts:2		cpuss.swd_data:0	scb[1].spi_clk:2
P3.3			tcpwm.line_compl[1]:0	scb[1].uart_rts:2		cpuss.swd_clk:0	scb[1].spi_select0:2
P3.4			tcpwm.line[2]:0				scb[1].spi_select1:1
P3.5			tcpwm.line_compl[2]:0				scb[1].spi_select2:1
P3.6			tcpwm.line[3]:0				scb[1].spi_select3:1
P3.7			tcpwm.line_compl[3]:0				
P11.0		prgio[0].io[0]	tcpwm.line[4]:3	scb[2].uart_rx:2		scb[2].i2c_scl:2	scb[2].spi_mosi:2
P11.1		prgio[0].io[1]	tcpwm.line_compl[4]:3	scb[2].uart_tx:2		scb[2].i2c_sda:2	scb[2].spi_miso:2
P11.2		prgio[0].io[2]	tcpwm.line[5]:3	scb[2].uart_cts:2		cpuss.swd_data:1	scb[2].spi_clk:2
P11.3		prgio[0].io[3]	tcpwm.line_compl[5]:3	scb[2].uart_rts:2		cpuss.swd_clk:1	scb[2].spi_select0:2
P11.4		prgio[0].io[4]	tcpwm.line[6]:3				scb[2].spi_select1:2
P11.5		prgio[0].io[5]	tcpwm.line_compl[6]:3				scb[2].spi_select2:2
P11.6		prgio[0].io[6]	tcpwm.line[7]:3				scb[2].spi_select3:2
P11.7		prgio[0].io[7]	tcpwm.line_compl[7]:3				
P4.0				scb[0].uart_rx:2	can[0].can_rx:1	scb[0].i2c_scl:2	scb[0].spi_mosi:2
P4.1				scb[0].uart_tx:2	can[0].can_tx:1	scb[0].i2c_sda:2	scb[0].spi_miso:2

Port/Pin	Analog	PRGIO & USB	Alt. Function 1	Alt. Function 2	Alt. Function 3	Alt. Function 4	Alt. Function 5
P4.2	csd[0].c_mod			scb[0].uart_cts:2	can[0].can_tx_enb_n:1	lpcomp.comp[0]:2	scb[0].spi_clk:2
P4.3	csd[0].c_sh_tank			scb[0].uart_rts:2		lpcomp.comp[1]:2	scb[0].spi_select0:2
P4.4					can[1].can_tx_enb_n:1		scb[0].spi_select1:2
P4.5					can[1].can_rx:1		scb[0].spi_select2:2
P4.6					can[1].can_tx:1		scb[0].spi_select3:2
P4.7							
P13.0		USBDP					
P13.1		USBDM					
P13.2		VBUS					
P7.0	srss.eco_in		tcpwm.line[0]:3	scb[3].uart_rx:2		scb[3].i2c_scl:2	scb[3].spi_mosi:2
P7.1	srss.eco_out		tcpwm.line_compl[0]:3	scb[3].uart_tx:2		scb[3].i2c_sda:2	scb[3].spi_miso:2
P7.2			tcpwm.line[1]:3	scb[3].uart_cts:2			scb[3].spi_clk:2
P7.3			tcpwm.line_compl[1]:3	scb[3].uart_rts:2			scb[3].spi_select0:2
P7.4			tcpwm.line[2]:3				scb[3].spi_select1:2
P7.5			tcpwm.line_compl[2]:3				scb[3].spi_select2:2
P7.6			tcpwm.line[3]:3				scb[3].spi_select3:2
P7.7			tcpwm.line_compl[3]:3				

Descriptions of the power pin functions are as follows:

VDDD: Power supply for both analog and digital sections (where there is no V_{DDA} pin)

VDDA: Analog V_{DD} pin where package pins allow; shorted to V_{DDD} otherwise

VDDIO: I/O pin power domain

VSSA: Analog ground pin where package pins allow; shorted to VSS otherwise

VSS: Ground pin

VCCD: Regulated digital supply (1.8 V ±5%)

GPIO and GPIO_OVT pins can be used as CSD sense and shield pins (a total of 94). Up to 64 of the pins can be used for LCD drive.

The following packages are supported: 124-ball BGA, 64-pin TQFP, 68-pin QFN, and 48-pin TQFP.

Power

The supply voltage range is 1.71 V to 5.5 V with all functions and circuits operating over that range.

The PSoC 4200-L family allows two distinct modes of power supply operation: Unregulated External Supply and Regulated External Supply modes.

Unregulated External Supply

In this mode, the PSoC 4200-L is powered by an External Power Supply that can be anywhere in the range of 1.8 V to 5.5 V. This range is also designed for battery-powered operation, for instance, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of the PSoC 4200-L supplies the internal logic and the VCCD output of the PSoC 4200-L must be bypassed to ground via an external Capacitor (in the range of 1 to 1.6 µF; X5R ceramic or better).

VDDA and VDDD must be shorted together on the PC board; the grounds, VSSA and VSS must also be shorted together. Bypass capacitors must be used from VDDD and VDDA to ground, typical practice for systems in this frequency range is to use a capacitor in the 1 µF range in parallel with a smaller capacitor (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

Power Supply	Bypass Capacitors
VDDD–VSS and VDDIO-VSS	0.1 µF ceramic at each pin plus bulk capacitor 1 to 10 µF.
VDDA–VSSA	0.1 µF ceramic at pin. Additional 1 µF to 10 µF bulk capacitor
VCCD–VSS	1 µF ceramic capacitor at the VCCD pin
VREF–VSSA (optional)	The internal bandgap may be bypassed with a 1 µF to 10 µF capacitor for better ADC performance.

Regulated External Supply

In this mode, the PSoC 4200-L is powered by an external power supply that must be within the range of 1.71 V to 1.89 V (1.8 ±5%); note that this range needs to include power supply ripple. In this mode, the VCCD and VDDD pins are shorted together and bypassed. The internal regulator is disabled in firmware.

Development Support

The PSoC 4200-L family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit www.cypress.com/go/psoc4 to find out more.

Documentation

A suite of documentation supports the PSoC 4200-L family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

Component Datasheets: The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

Application Notes: PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

Technical Reference Manual: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers.

Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 4200-L family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

Table 2. DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID23	I_{DD18}	I^2C wakeup, WDT, and Comparators on. Regulator Off.	–	2.4	2.9	mA	V_{DD} = 1.71 to 1.89, 12 MHz
SID24	I_{DD19}	I^2C wakeup, WDT, and Comparators on.	–	2.3	2.8	mA	V_{DD} = 1.8 to 5.5, 12 MHz
Deep Sleep Mode, –40 °C to + 60 °C							
SID30	I_{DD25}	I^2C wakeup and WDT on. Regulator Off.	–	–	13.5	µA	V_{DD} = 1.71 to 1.89
SID31	I_{DD26}	I^2C wakeup and WDT on.	–	1.3	20.0	µA	V_{DD} = 1.8 to 3.6
SID32	I_{DD27}	I^2C wakeup and WDT on.	–	–	20.0	µA	V_{DD} = 3.6 to 5.5
Deep Sleep Mode, +85 °C							
SID33	I_{DD28}	I^2C wakeup and WDT on. Regulator Off.	–	–	45.0	µA	V_{DD} = 1.71 to 1.89
SID34	I_{DD29}	I^2C wakeup and WDT on.	–	15	60.0	µA	V_{DD} = 1.8 to 3.6
SID35	I_{DD30}	I^2C wakeup and WDT on.	–	–	45.0	µA	V_{DD} = 3.6 to 5.5
Hibernate Mode, –40 °C to + 60 °C							
SID39	I_{DD34}	Regulator Off.	–	–	1123	nA	V_{DD} = 1.71 to 1.89
SID40	I_{DD35}		–	150	1600	nA	V_{DD} = 1.8 to 3.6
SID41	I_{DD36}		–	–	1600	nA	V_{DD} = 3.6 to 5.5
Hibernate Mode, +85 °C							
SID42	I_{DD37}	Regulator Off.	–	–	4142	nA	V_{DD} = 1.71 to 1.89
SID43	I_{DD38}		–	–	9700	nA	V_{DD} = 1.8 to 3.6
SID44	I_{DD39}		–	–	10,400	nA	V_{DD} = 3.6 to 5.5
Stop Mode							
SID304	I_{DD43A}	Stop Mode current; V_{DD} = 3.6 V	–	20	659	nA	T = –40 °C to +60 °C
SID304A	I_{DD43B}	Stop Mode current; V_{DD} = 3.6 V	–	–	1810	nA	T = +85 °C
XRES current							
SID307	I_{DD_XR}	Supply current while XRES (Active Low) asserted	–	2	5	mA	

Table 3. AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID48	F_{CPU}	CPU frequency	DC	–	48	MHz	$1.71 \le V_{DD} \le 5.5$
SID49	T_{SLEEP}	Wakeup from sleep mode	–	0	–	µs	Guaranteed by characterization
SID50	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	–	25	µs	24-MHz IMO. Guaranteed by characterization
SID51	$T_{HIBERNATE}$	Wakeup from Hibernate mode	–	–	0.7	ms	Guaranteed by characterization
SID51A	T_{STOP}	Wakeup from Stop mode	–	–	1.9	ms	Guaranteed by characterization
SID52	$T_{RESETWIDTH}$	External reset pulse width	1	–	–	µs	Guaranteed by characterization

GPIO

Table 4. GPIO DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID57	V_{IH}[2]	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS Input
SID57A	I_{IHS}	Input current when Pad > V_{DDIO} for OVT inputs	–	–	10	µA	Per I^2C Spec
SID58	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}	V	CMOS Input
SID241	V_{IH}[2]	LVTTL input, V_{DDD} < 2.7 V	0.7× V_{DDD}	–	–	V	
SID242	V_{IL}	LVTTL input, V_{DDD} < 2.7 V	–	–	0.3 × V_{DDD}	V	
SID243	V_{IH}[2]	LVTTL input, $V_{DDD} \geq 2.7$ V	2.0	–	–	V	
SID244	V_{IL}	LVTTL input, $V_{DDD} \geq 2.7$ V	–	–	0.8	V	
SID59	V_{OH}	Output voltage high level	V_{DDD} –0.6	–	–	V	I_{OH} = 4 mA at 3 V V_{DDD}
SID60	V_{OH}	Output voltage high level	V_{DDD} –0.5	–	–	V	I_{OH} = 1 mA at 1.8 V V_{DDD}
SID61	V_{OL}	Output voltage low level	–	–	0.6	V	I_{OL} = 4 mA at 1.8 V V_{DDD}
SID62	V_{OL}	Output voltage low level	–	–	0.6	V	I_{OL} = 8 mA at 3 V V_{DDD}
SID62A	V_{OL}	Output voltage low level	–	–	0.4	V	I_{OL} = 3 mA at 3 V V_{DDD}
SID63	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	
SID65	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DDD} = 3.0 V
SID65A	I_{IL_CTBM}	Input leakage current (absolute value) for CTBM pins	–	–	4	nA	
SID66	C_{IN}	Input capacitance	–	–	7	pF	Not applicable for P6.4, P6.5, P12.0, P12.1, and for USB pins.
SID67	V_{HYSTTL}	Input hysteresis LVTTL	25	40	–	mV	$V_{DDD} \geq 2.7$ V
SID68	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DDD}	–	–	mV	
SID69	I_{DIODE}	Current through protection diode to V_{DD}/Vss	–	–	100	µA	Guaranteed by characterization
SID69A	I_{TOT_GPIO}	Maximum Total Source or Sink Chip Current	–	–	200	mA	Guaranteed by characterization

Note
2. V_{IH} must not exceed V_{DDD} + 0.2 V.

Table 5. GPIO AC Specifications

(Guaranteed by Characterization)[3]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID70	T_{RISEF}	Rise time in fast strong mode	2	–	12	ns	3.3 V V_{DDD}, Cload = 25 pF
SID71	T_{FALLF}	Fall time in fast strong mode	2	–	12	ns	3.3 V V_{DDD}, Cload = 25 pF
SID72	T_{RISES}	Rise time in slow strong mode	10	–	60	ns	3.3 V V_{DDD}, Cload = 25 pF
SID73	T_{FALLS}	Fall time in slow strong mode	10	–	60	ns	3.3 V V_{DDD}, Cload = 25 pF
SID74	$F_{GPIOUT1}$	GPIO Fout;3.3 V ≤ V_{DDD} ≤ 5.5 V. Fast strong mode.	–	–	33	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO Fout;1.7 V≤ V_{DDD}≤ 3.3 V. Fast strong mode.	–	–	16.7	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID76	$F_{GPIOUT3}$	GPIO Fout;3.3 V ≤ V_{DDD} ≤ 5.5 V. Slow strong mode.	–	–	7	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID245	$F_{GPIOUT4}$	GPIO Fout;1.7 V ≤ V_{DDD} ≤ 3.3 V. Slow strong mode.	–	–	3.5	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID246	F_{GPIOIN}	GPIO input operating frequency; 1.71 V ≤ V_{DDD} ≤ 5.5 V	–	–	48	MHz	90/10% V_{IO}

XRES

Table 6. XRES DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID77	V_{IH}	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS Input
SID78	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}	V	CMOS Input
SID79	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID80	C_{IN}	Input capacitance	–	3	–	pF	
SID81	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	Guaranteed by characterization
SID82	I_{DIODE}	Current through protection diode to V_{DDD}/V_{SS}	–	–	100	µA	Guaranteed by characterization

Table 7. XRES AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID83	$T_{RESETWIDTH}$	Reset pulse width	1	–	–	µs	Guaranteed by characterization

Note

3. Simultaneous switching transitions on many fully-loaded GPIO pins may cause ground perturbations depending on several factors including PCB and decoupling capacitor design. For applications that are very sensitive to ground perturbations, the slower GPIO slew rate setting may be used.

Table 8. Opamp Specifications

(Guaranteed by Characterization) *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID295	V_{N3}	Input referred, 10kHz, power = high	–	28	–	nV/rtHz	
SID296	V_{N4}	Input referred, 100kHz, power = high	–	15	–	nV/rtHz	
SID297	Cload	Stable up to maximum load. Performance specs at 50 pF.	–	–	125	pF	
SID298	Slew_rate	Cload = 50 pF, Power = High, $V_{DDA} \geq 2.7$ V	6	–	–	V/µs	
SID299	T_op_wake	From disable to enable, no external RC dominating	–	25	–	µs	
SID299A	OL_GAIN	Open Loop Gain	–	90	–	dB	
	Comp_mode	Comparator mode; 50 mV drive, $T_{rise} = T_{fall}$ (approx.)	–	–	–		
SID300	T_{PD1}	Response time; power = high	–	150	–	ns	
SID301	T_{PD2}	Response time; power = medium	–	400	–	ns	
SID302	T_{PD3}	Response time; power = low	–	2000	–	ns	
SID303	Vhyst_op	Hysteresis	–	10	–	mV	
Deep Sleep Mode		Mode 2 is lowest current range. Mode 1 has higher GBW.					Deep Sleep mode $V_{DDA} \geq 2.7$ V.
SID_DS_1	IDD_HI_M1	Mode 1, High current	–	1400	–	µA	25 °C
SID_DS_2	IDD_MED_M1	Mode 1, Medium current	–	700	–	µA	25 °C
SID_DS_3	IDD_LOW_M1	Mode 1, Low current	–	200	–	µA	25 °C
SID_DS_4	IDD_HI_M2	Mode 2, High current	–	120	–	µA	25 °C
SID_DS_5	IDD_MED_M2	Mode 2, Medium current	–	60	–	µA	25 °C
SID_DS_6	IDD_LOW_M2	Mode 2, Low current	–	15	–	µA	25 °C
SID_DS_7	GBW_HI_M1	Mode 1, High current	–	4	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA}-1.5 V
SID_DS_8	GBW_MED_M1	Mode 1, Medium current	–	2	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA}-1.5 V
SID_DS_9	GBW_LOW_M1	Mode 1, Low current	–	0.5	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA}-1.5 V
SID_DS_10	GBW_HI_M2	Mode 2, High current	–	0.5	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA}-1.5 V
SID_DS_11	GBW_MED_M2	Mode 2, Medium current	–	0.2	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA}-1.5 V
SID_DS_12	GBW_LOW_M2	Mode 2, Low current	–	0.1	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA}-1.5 V
SID_DS_13	VOS_HI_M1	Mode 1, High current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA}-1.5 V
SID_DS_14	VOS_MED_M1	Mode 1, Medium current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA}-1.5 V
SID_DS_15	VOS_LOW_M2	Mode 1, Low current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA}-1.5 V
SID_DS_16	VOS_HI_M2	Mode 2, High current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA}-1.5 V
SID_DS_17	VOS_MED_M2	Mode 2, Medium current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA}-1.5 V

Table 8. Opamp Specifications

(Guaranteed by Characterization) *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID_DS_18	VOS_LOW_M2	Mode 2, Low current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA}-1.5 V
SID_DS_19	IOUT_HI_M!	Mode 1, High current	–	10	–	mA	Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_20	IOUT_MED_M1	Mode 1, Medium current	–	10	–	mA	Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_21	IOUT_LOW_M1	Mode 1, Low current	–	4	–	mA	Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_22	IOUT_HI_M2	Mode 2, High current	–	1	–	mA	Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_23	IOU_MED_M2	Mode 2, Medium current	–	1	–	mA	Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_24	IOU_LOW_M2	Mode 2, Low current	–	0.5	–	mA	Output is 0.5 V to V_{DDA}-0.5 V

Comparator

Table 9. Comparator DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID85	$V_{OFFSET2}$	Input offset voltage. Custom trim. Common mode voltage range from 0 to V_{DD}-1.	–	–	±4	mV	
SID85A	$V_{OFFSET3}$	Input offset voltage. Ultra low-power mode.	–	±12	–	mV	V_{DDD} ≥ 2.2 V for Temp < 0 °C, V_{DDD} ≥ 1.8 V for Temp > 0 °C
SID86	V_{HYST}	Hysteresis when enabled. Common mode voltage range from 0 to V_{DD} -1.	–	10	35	mV	Guaranteed by characterization
SID87	V_{ICM1}	Input common mode voltage in normal mode	0	–	V_{DDD} – 0.2	V	Modes 1 and 2.
SID247	V_{ICM2}	Input common mode voltage in low power mode	0	–	V_{DDD}	V	
SID247A	V_{ICM2}	Input common mode voltage in ultra low power mode	0	–	V_{DDD} – 1.15	V	V_{DDD} ≥ 2.2 V for Temp < 0 °C, V_{DDD} ≥ 1.8 V for Temp > 0 °C
SID88	CMRR	Common mode rejection ratio	50	–	–	dB	V_{DDD} ≥ 2.7 V. Guaranteed by characterization
SID88A	CMRR	Common mode rejection ratio	42	–	–	dB	V_{DDD} < 2.7 V. Guaranteed by characterization
SID89	I_{CMP1}	Block current, normal mode	–	280	400	µA	Guaranteed by characterization
SID248	I_{CMP2}	Block current, low power mode	–	50	100	µA	Guaranteed by characterization
SID259	I_{CMP3}	Block current, ultra low power mode	–	6	28	µA	Guaranteed by characterization, V_{DDD} ≥ 2.2 V for Temp < 0 °C, V_{DDD} ≥ 1.8 V for Temp > 0 °
SID90	Z_{CMP}	DC input impedance of comparator	35	–	–	MΩ	Guaranteed by characterization

Table 10. Comparator AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID91	T_{RESP1}	Response time, normal mode	–	38	110	ns	50-mV overdrive
SID258	T_{RESP2}	Response time, low power mode	–	70	200	ns	50-mV overdrive
SID92	T_{RESP3}	Response time, ultra low power mode	–	2.3	15	µs	200-mV overdrive. $V_{DDD} \geq 2.2$ V for Temp < 0 °C, $V_{DDD} \geq 1.8$ V for Temp > 0 °C

Temperature Sensor

Table 11. Temperature Sensor Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID93	$T_{SENSACC}$	Temperature sensor accuracy	–5	±1	+5	°C	–40 to +85 °C

SAR ADC

Table 12. SAR ADC DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID94	A_RES	Resolution	–	–	12	bits	
SID95	A_CHNIS_S	Number of channels - single ended	–	–	16		8 full speed
SID96	A-CHNKS_D	Number of channels - differential	–	–	8		Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity	–	–	–		Yes. Based on characterization
SID98	A_GAINERR	Gain error	–	–	±0.1	%	With external reference.
SID99	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V V_{REF}.
SID100	A_ISAR	Current consumption	–	–	1	mA	
SID101	A_VINS	Input voltage range - single ended	V_{SS}	–	V_{DDA}	V	Based on device characterization
SID102	A_VIND	Input voltage range - differential	V_{SS}	–	V_{DDA}	V	Based on device characterization
SID103	A_INRES	Input resistance	–	–	2.2	KΩ	Based on device characterization
SID104	A_INCAP	Input capacitance	–	–	10	pF	Based on device characterization

Table 13. SAR ADC AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID106	A_PSRR	Power supply rejection ratio	70	–	–	dB	
SID107	A_CMRR	Common mode rejection ratio	66	–	–	dB	Measured at 1 V
SID108	A_SAMP_1	Sample rate with external reference bypass cap	–	–	1	Msps	
SID108A	A_SAMP_2	Sample rate with no bypass cap. Reference = V_{DD}	–	–	500	Ksps	

SWD Interface

Table 32. SWD Interface Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID213	F_SWDCLK1	3.3 V ≤ V_{DD} ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID214	F_SWDCLK2	1.71 V ≤ V_{DD} ≤ 3.3 V	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID215	T_SWDI_SETUP	T = 1/f SWDCLK	0.25*T	–	–	ns	Guaranteed by characterization
SID216	T_SWDI_HOLD	T = 1/f SWDCLK	0.25*T	–	–	ns	Guaranteed by characterization
SID217	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5*T	ns	Guaranteed by characterization
SID217A	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	Guaranteed by characterization

Internal Main Oscillator

Table 33. IMO DC Specifications

(Guaranteed by Design)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I_{IMO1}	IMO operating current at 48 MHz	–	–	1000	µA	
SID219	I_{IMO2}	IMO operating current at 24 MHz	–	–	325	µA	
SID220	I_{IMO3}	IMO operating current at 12 MHz	–	–	225	µA	
SID221	I_{IMO4}	IMO operating current at 6 MHz	–	–	180	µA	
SID222	I_{IMO5}	IMO operating current at 3 MHz	–	–	150	µA	

Table 34. IMO AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	$F_{IMOTOL1}$	Frequency variation from 3 to 48 MHz	–	–	±2	%	
SID226	$T_{STARTIMO}$	IMO startup time	–	–	12	µs	
SID227	$T_{JITRMSIMO1}$	RMS Jitter at 3 MHz	–	156	–	ps	
SID228	$T_{JITRMSIMO2}$	RMS Jitter at 24 MHz	–	145	–	ps	
SID229	$T_{JITRMSIMO3}$	RMS Jitter at 48 MHz	–	139	–	ps	

Internal Low-Speed Oscillator

Table 35. ILO DC Specifications

(Guaranteed by Design)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	I_{ILO1}	ILO operating current at 32 kHz	–	0.3	1.05	µA	Guaranteed by Characterization
SID233	$I_{ILOLEAK}$	ILO leakage current	–	2	15	nA	Guaranteed by Design

Table 43. Block Specs

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID256	T_{WS48}	Number of wait states at 48 MHz	2	–	–		CPU execution from Flash. Guaranteed by characterization
SID257	T_{WS24}	Number of wait states at 24 MHz	1	–	–		CPU execution from Flash. Guaranteed by characterization
SID260	V_{REFSAR}	Trimmed internal reference to SAR	–1	–	+1	%	Percentage of Vbg (1.024 V). Guaranteed by characterization
SID261	$F_{SARINTREF}$	SAR operating speed without external reference bypass	–	500	–	ksps	12-bit resolution. Guaranteed by characterization
SID262	$T_{CLKSWITCH}$	Clock switching from clk1 to clk2 in clk1 periods	3	–	4	Periods	Guaranteed by design
* Tws48 and Tws24 are guaranteed by Design							

Table 44. UDB Port Adaptor Specifications

(Based on LPC Component Specs; all specs except TLCLKDO are guaranteed by design -10-pF load, 3-V V_{DDIO} and V_{DDD})

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID263	T_{LCLKDO}	LCLK to output delay	–	–	18	ns	
SID264	$T_{DINLCLK}$	Input setup time to LCLCK rising edge	–	–	7	ns	
SID265	$T_{DINLCLKHLD}$	Input hold time from LCLK rising edge	0	–	–	ns	
SID266	$T_{LCLKHIZ}$	LCLK to output tristated	–	–	28	ns	
SID267	T_{FLCLK}	LCLK frequency	–	–	33	MHz	
SID268	$T_{LCLKDUTY}$	LCLK duty cycle (percentage high)	40	–	60	%	

Table 45. USB Device Block Specifications (USB only)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID321	Vusb_5	Device supply for USB operation	4.5	–	5.5	V	USB Configured, USB Reg. enabled
SID322	Vusb_3.3	Device supply for USB operation	3.15	–	3.6	V	USB Configured, USB Reg. bypassed
SID323	Vusb_3.3	Device supply for USB operation (Functional operation only)	2.85	–	3.6	V	USB Configured, USB Reg. bypassed
SID324	Iusb_config	Device supply current in Active mode, IMO = 24 MHz	–	10	–	mA	V_{DDD} = 5 V
SID325	Iusb_config	Device supply current in Active mode, IMO = 24 MHz	–	8	–	mA	V_{DDD} = 3.3 V
SID326	Isub_suspend	Device supply current in Sleep mode	–	0.5	–	mA	V_{DDD} = 5 V, PICU wakeup
SID327	Isub_suspend	Device supply current in Sleep mode	–	0.3	–	mA	V_{DDD} = 5 V, Device disconnected
SID328	Isub_suspend	Device supply current in Sleep mode	–	0.5	–	mA	V_{DDD} = 3.3 V, PICU wakeup
SID329	Isub_suspend	Device supply current in Sleep mode	–	0.3	–	mA	V_{DDD} = 3.3 V, Device disconnected

Ordering Information

The PSoC 4200-L family part numbers and features are listed in the following table.

Table 48. PSoC 4200-L Ordering Information

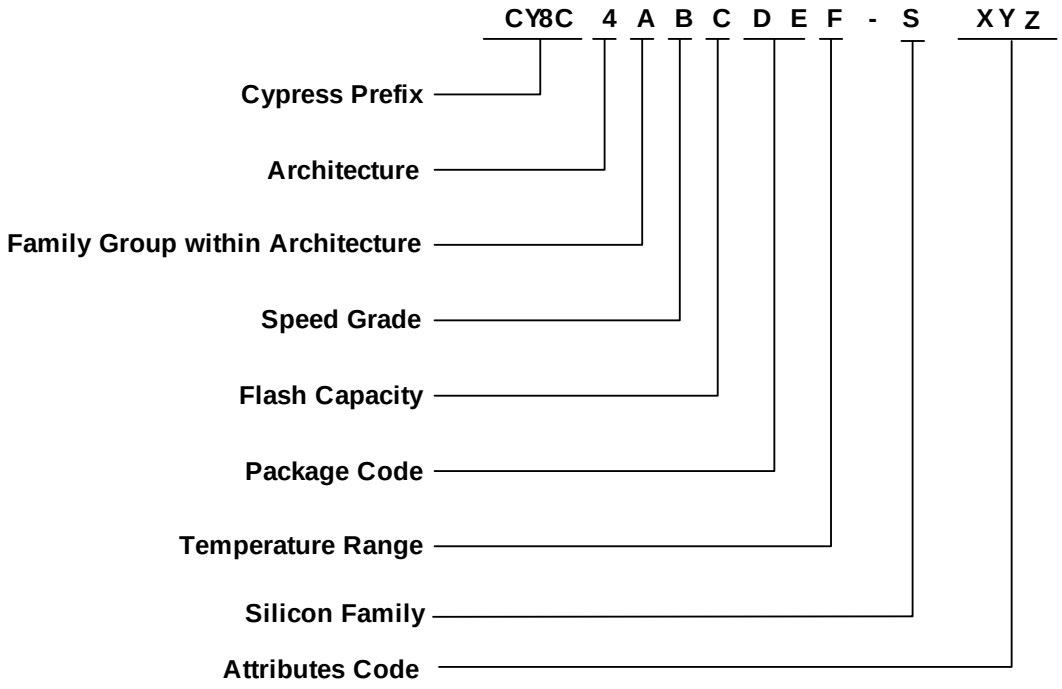
Category	MPN	Features														Package			
		Max CPU Speed (MHz)	Flash (KB)	SRAM (KB)	UDB	Op-amp (CTBm)	CSD	Direct LCD Drive	12-bit SAR ADC	LP Comparators	TCPWM Blocks	SCB Blocks	USB Full Speed	CAN	GPIO	48-TQFP	64-TQFP	68-QFN	124-VFBGA
4246	CY8C4246AZI-L423	48	64	8	8	2	1	✔	1000 ksps	2	8	3	–	–	38	✔	–	–	–
	CY8C4246AZI-L433	48	64	8	8	2	–	–	1000 ksps	2	8	3	✔	–	38	✔	–	–	–
	CY8C4246AZI-L435	48	64	8	8	2	–	–	1000 ksps	2	8	4	✔	–	53	–	✔	–	–
	CY8C4246AZI-L445	48	64	8	8	2	2	✔	1000 ksps	2	8	4	✔	–	53	–	✔	–	–
	CY8C4246LTI-L445	48	64	8	8	2	2	✔	1000 ksps	2	8	4	✔	–	57	–	–	✔	–
4247	CY8C4247AZI-L423	48	128	16	8	2	1	✔	1000 ksps	2	8	3	–	–	38	✔	–	–	–
	CY8C4247AZI-L433	48	128	16	8	2	–	–	1000 ksps	2	8	3	✔	–	38	✔	–	–	–
	CY8C4247AZI-L445	48	128	16	8	2	2	✔	1000 ksps	2	8	4	✔	–	53	–	✔	–	–
	CY8C4247LTI-L445	48	128	16	8	2	2	✔	1000 ksps	2	8	4	✔	–	57	–	–	✔	–
	CY8C4247AZI-L475	48	128	16	8	4	2	–	1000 ksps	2	8	4	✔	–	53	–	✔	–	–
	CY8C4247LTI-L475	48	128	16	8	4	2	–	1000 ksps	2	8	4	✔	–	57	–	–	✔	–
	CY8C4247BZI-L479	48	128	16	8	4	2	–	1000 ksps	2	8	4	✔	–	98	–	–	–	✔
	CY8C4247AZI-L485	48	128	16	8	4	2	✔	1000 ksps	2	8	4	✔	✔	53	–	✔	–	–
	CY8C4247LTI-L485	48	128	16	8	4	2	✔	1000 ksps	2	8	4	✔	✔	57	–	–	✔	–
	CY8C4247BZI-L489	48	128	16	8	4	2	✔	1000 ksps	2	8	4	✔	✔	98	–	–	–	✔
4248	CY8C4248BZI-L469	48	256	32	8	4	–	–	1000 ksps	2	8	4	–	–	96	–	–	–	✔
	CY8C4248AZI-L475	48	256	32	8	4	2	–	1000 ksps	2	8	4	✔	–	53	–	✔	–	–
	CY8C4248LTI-L475	48	256	32	8	4	2	–	1000 ksps	2	8	4	✔	–	57	–	–	✔	–
	CY8C4248BZI-L479	48	256	32	8	4	2	–	1000 ksps	2	8	4	✔	–	98	–	–	–	✔
	CY8C4248AZI-L485	48	256	32	8	4	2	✔	1000 ksps	2	8	4	✔	✔	53	–	✔	–	–
	CY8C4248LTI-L485	48	256	32	8	4	2	✔	1000 ksps	2	8	4	✔	✔	57	–	–	✔	–
	CY8C4248BZI-L489	48	256	32	8	4	2	✔	1000 ksps	2	8	4	✔	✔	98	–	–	–	✔

The nomenclature used in Table 48 is based on the following part numbering convention:

Field	Description	Values	Meaning
CY8C	Cypress Prefix		
4	Architecture	4	PSoC 4
A	Family	2	4200 Family
B	CPU Speed	4	48 MHz
C	Flash Capacity	6	64 KB
		7	128 KB
		8	256 KB
DE	Package Code	AX, AZ	TQFP
		LT	QFN
		BU	BGA
		FD	CSP
F	Temperature Range	I	Industrial
S	Silicon Family	N/A	PSoC 4A
		L	PSoC 4A-L
		BL	PSoC 4A-BLE
XYZ	Attributes Code	000-999	Code of feature set in the specific family

Part Numbering Conventions

The part number fields are defined as follows.



Packaging

The description of the PSoC4200-L package dimensions follows.

SPEC ID#	Package	Description	Package DWG #
PKG_1	124-ball VFBGA	124-ball, 9 mm x 9 mm x 1.0 mm height with 0.65 mm ball pitch	001-97718
PKG_2	64-pin TQFP	64-pin TQFP, 10 mm x10 mm x 1,4 mm height with 0.5 mm pitch	51-85051
PKG_3	68-pin QFN	68-pin QFN, 8 mm x 8 mm x 1.0 mm height with 0.4 mm pitch	001-09618
PKG_4	48-pin TQFP	48-pin TQFP, 7 mm x 7 mm x 1.4 mm height with 0.5 mm pitch	51-85135

Table 49. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature		–40	25.00	85	°C
T_J	Operating junction temperature		–40	–	100	°C
T_{JA}	Package θ_{JA} (124-ball VFBGA)		–	35	–	°C/Watt
T_{JA}	Package θ_{JA} (64-pin TQFP)		–	54	–	°C/Watt
T_{JA}	Package θ_{JA} (68-pin QFN)		–	17	–	°C/Watt
T_{JA}	Package θ_{JA} (48-pin TQFP)		–	67	–	°C/Watt

Table 50. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
All packages	260 °C	30 seconds

Table 51. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
All packages	MSL 3

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