Infineon Technologies - CY8C4248BZI-L489 Datasheet

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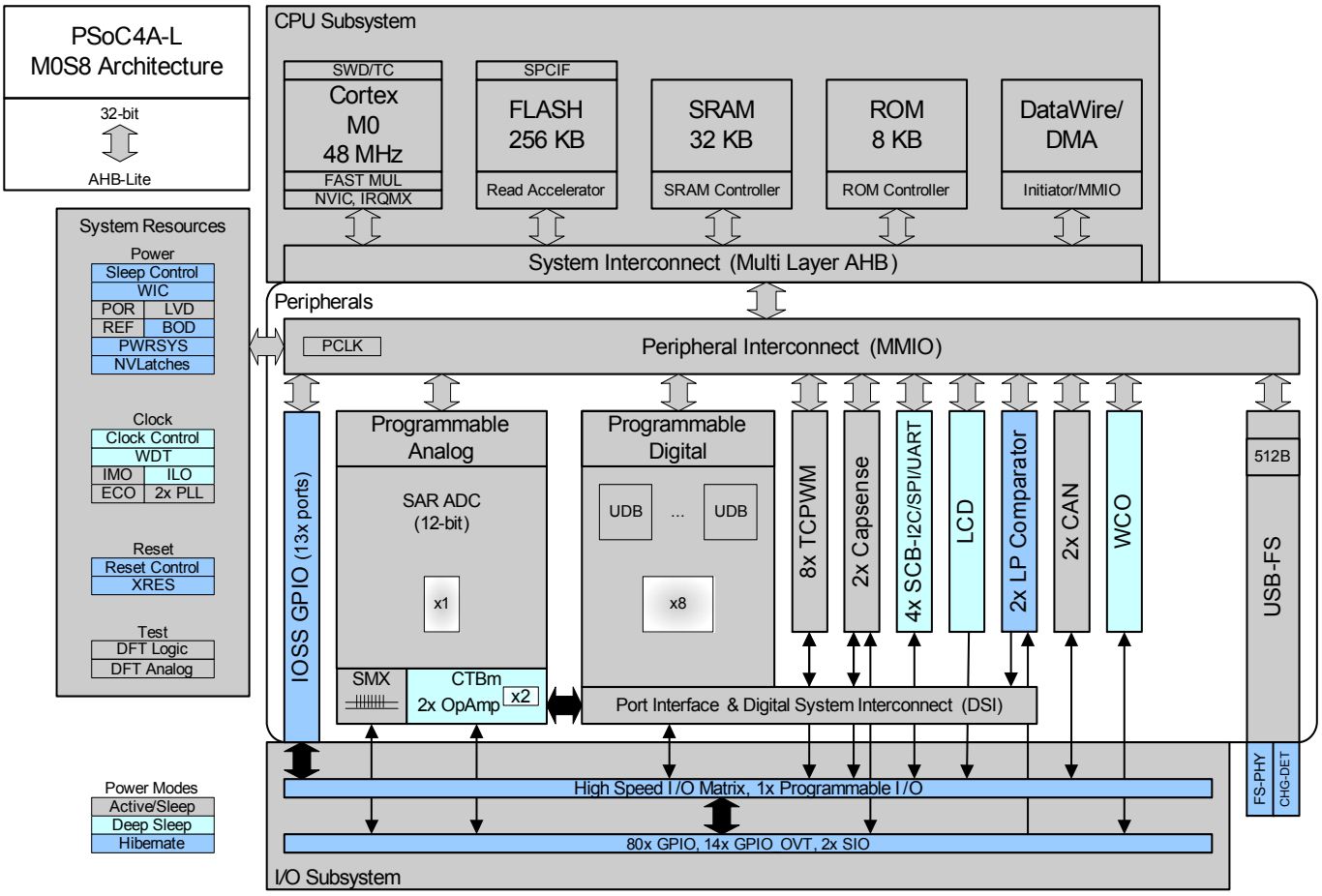
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, I²C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, LCD, LVD, POR, PWM, SmartSense, WDT
Number of I/O	98
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b SAR; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	124-VFBGA
Supplier Device Package	124-VFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4248bzi-l489

Figure 2. Block Diagram



PSoC 4200-L Block Diagram

The PSoC 4200-L devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM Serial_Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator Integrated Development Environment (IDE) provides fully integrated programming and debug support for PSoC 4200-L devices. The SWD interface is fully compatible with industry-standard third-party tools. The PSoC 4200-L family provides a level of security not possible with multi-chip application solutions or with microcontrollers. This is due to its ability to disable debug features, robust flash protection, and because it allows customer-proprietary functionality to be implemented in on-chip programmable blocks.

The debug circuits are enabled by default and can only be disabled in firmware. If not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. Because all programming, debug, and test interfaces are disabled when maximum device security is enabled, PSoC 4200-L with device security enabled may not be returned for failure analysis. This is a trade-off the PSoC 4200-L allows the customer to make.

Functional Definition

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in the PSoC 4200-L is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and execute a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC), which can wake the processor up from the Deep Sleep mode allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a 2-wire form of JTAG; the debug configuration used for PSoC 4200-L has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The PSoC 4200-L has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 2 wait-state (WS) access time at 48 MHz and with 1-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

SRAM

SRAM memory is retained during Hibernate.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

DMA

A DMA engine is provided that can do 32-bit transfers and has chainable ping-pong descriptors.

System Resources

Power System

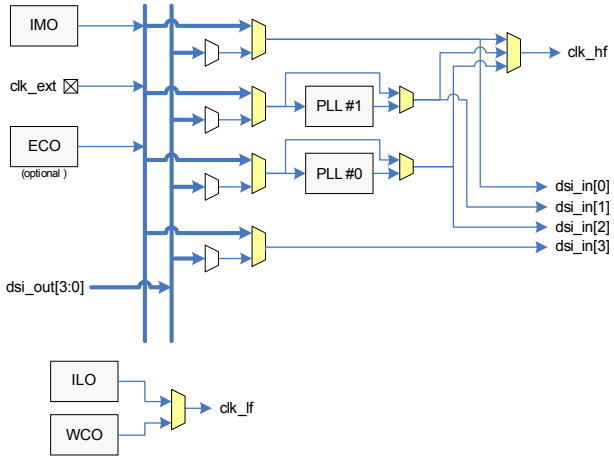
The power system is described in detail in the section Power on page 15. It provides assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (brown-out detect (BOD)) or interrupts (low voltage detect (LVD)). The PSoC 4200-L operates with a single external supply over the range of 1.71 to 5.5 V and has five different power modes, transitions between which are managed by the power system. The PSoC 4200-L provides Sleep, Deep Sleep, Hibernate, and Stop low-power modes.

Clock System

The PSoC 4200-L clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that no meta-stable conditions occur.

The clock system for the PSoC 4200-L consists of a crystal oscillator (4 to 33 MHz), a watch crystal oscillator (32 kHz), a phase-locked loop (PLL), the IMO and the ILO internal oscillators, and provision for an external clock.

Figure 3. PSoC 4200-L MCU Clocking Architecture



The clk_hf signal can be divided down to generate synchronous clocks for the UDBs, and the analog and digital peripherals. There are a total of 16 clock dividers for the PSoC 4200-L, each with 16-bit divide capability; this allows 12 to be used for the fixed-function blocks and four for the UDBs. The analog clock leads the digital clocks to allow analog events to occur before digital clock-related noise is generated. The 16-bit capability allows a lot of flexibility in generating fine-grained frequency values and is fully supported in PSoC Creator.

IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 4200-L. It is trimmed during testing to achieve the specified accuracy. Trim values are stored in nonvolatile latches (NVL). Additional trim settings from flash can be used to compensate for changes. The IMO default frequency is 24 MHz and it can be adjusted between 3 to 48 MHz in steps of 1 MHz. IMO tolerance with Cypress-provided calibration settings is ±2%.

ILO Clock Source

The ILO is a very low power oscillator, nominally 32 kHz, which is primarily used to generate clocks for peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

Crystal Oscillators and PLL

The PSoC 4200-L clock subsystem also implements two oscillators: high-frequency (4 to 33 MHz) and low-frequency (32-kHz watch crystal) that can be used for precision timing applications. The PLL can generate a 48-MHz output from the high-frequency oscillator.

Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the timeout occurs. The watchdog reset is recorded in the Reset Cause register.

Reset

The PSoC 4200-L can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset to avoid complications with configuration and multiple pin functions during power-on or reconfiguration.

Voltage Reference

The PSoC 4200-L reference system generates all internally required references. A 1% voltage reference spec is provided for the 12-bit ADC. To allow better signal-to-noise ratios (SNR) and better absolute accuracy, it is possible to add an external bypass capacitor to the internal reference using a GPIO pin or to use an external reference for the SAR.

Analog Blocks

12-bit SAR ADC

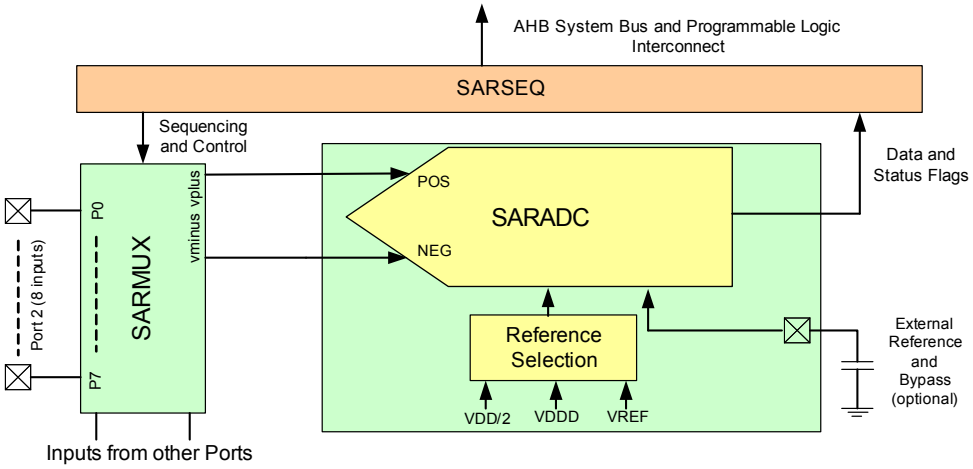
The 12-bit, 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The block functionality is augmented for the user by adding a reference buffer to it (trimmable to ±1%) and by providing the choice (for the PSoC 4200-L case) of three internal voltage references: V_{DD}, $V_{DD}/2$, and V_{REF} (nominally 1.024 V) as well as an external reference through a GPIO pin. The Sample-and-Hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. The system performance will be 65 dB for true 12-bit precision if appropriate references are used and system noise levels permit. To improve performance in noisy conditions, it is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer (expandable to 16 inputs). The sequencer cycles through selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, the aggregate sampling bandwidth is equal to 1 Msps, whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware-driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. In addition, the signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is able to digitize the output of the on-board temperature sensor for calibration and other temperature-dependent functions. The SAR is not available in Deep Sleep and Hibernate modes as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 to 5.5 V.

Figure 4. SAR ADC System Diagram



CAN Blocks

There are two independent CAN 2.0B blocks, which are certified CAN conformant.

GPIO

The PSoC 4200-L has 96 GPIOs. The GPIO block implements the following:

- Eight drive strength modes including strong push-pull, resistive pull-up and pull-down, weak (resistive) pull-up and pull-down, open drain and open source, input only, and disabled
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output disables
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode and Hibernate modes)
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals are also fixed to reduce internal multiplexing complexity (these signals do not go through the DSI network). DSI signals are not affected by this and any pin may be routed to any UDB through the DSI network.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (13 for PSoC 4200-L).

There are 14 GPIO pins that are overvoltage tolerant (V_{IN} can exceed V_{DD}). The overvoltage cells will not sink more than 10 µA when their inputs exceed V_{DDIO} in compliance with I^2C specifications. Meeting the I^2C minimum fall time requirement for FM and FM+ may require the slower slew rate setting depending on bus loading (also applies to all GPIO and SIO pins).

SIO

The Special I/O (SIO) pins have the following features in addition to the GPIO features:

- Overvoltage protection and hot swap capability
- Programmable switching thresholds
- Programmable output pull-up voltage capability

They allow interfacing to buses, such as I^2C with full I^2C compatibility and interfacing to devices operating at different voltage levels. There are two SIO pins on the PSoC4200-L.

Special Function Peripherals

LCD Segment Drive

The PSoC 4200-L has an LCD controller, which can drive up to eight commons and up to 56 segments. Any pin can be either a common or a segment pin. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as digital correlation and PWM.

Digital correlation pertains to modulating the frequency and levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays.

PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep refreshing a small display buffer (4 bits; 1 32-bit register per port).

CapSense

CapSense is supported on all pins in the PSoC 4200-L through two CapSense Sigma-Delta (CSD) blocks that can be connected to any pin through an analog mux bus that any GPIO pin can be connected to via an Analog switch. CapSense function can thus be provided on any pin or group of pins in a system under software control. A component is provided for the CapSense block to make it easy for the user.

Shield voltage can be driven on another Mux Bus to provide water tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input.

Each CapSense block has two IDACs which can be used for general purposes if CapSense is not being used.(both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available). The two CapSense blocks can be used independently.

Pinouts

The following is the pin list for the PSoC 4200-L.

124-BGA		68-QFN		64-TQFP		48-TQFP		48-TQFP-USB	
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
H13	P0.0	42	P0.0	39	P0.0	28	P0.0	28	P0.0
H12	P0.1	43	P0.1	40	P0.1	29	P0.1	29	P0.1
G13	P0.2	44	P0.2	41	P0.2	30	P0.2	30	P0.2
G12	P0.3	45	P0.3	42	P0.3	31	P0.3	31	P0.3
K10	VSSD								
G11	P0.4	46	P0.4	43	P0.4	32	P0.4	32	P0.4
F13	P0.5	47	P0.5	44	P0.5	33	P0.5	33	P0.5
F12	P0.6	48	P0.6	45	P0.6	34	P0.6	34	P0.6
F11	P0.7	49	P0.7	46	P0.7	35	P0.7	35	P0.7
E13	P8.0								
E12	P8.1								
E11	P8.2								
D13	P8.3								
D12	P8.4								
C13	P8.5								
C12	P8.6								
B12	P8.7								
C11	XRES	50	XRES	47	XRES	36	XRES	36	XRES
A12	VCCD	51	VCCD	48	VCCD	37	VCCD	37	VCCD
D10	VSSD	52	VSSD	49	VSSD	38	VSSD	38	VSSD
B13	VDDD	53	VDDD	50	VDDD	39	VDDD	39	VDDD
A13	VDDD	53	VDDD	50	VDDD	39	VDDD	39	VDDD
A11	P9.0								
B11	P9.1								
A10	P9.2								
B10	P9.3								
C10	P9.4								
A9	P9.5								
B9	P9.6								
C9	P9.7								
						40	VDDA	40	VDDA
C8	P5.0	54	P5.0	51	P5.0				
B8	P5.1	55	P5.1	52	P5.1				
A8	P5.2	56	P5.2	53	P5.2				
A7	P5.3	57	P5.3	54	P5.3				
B7	P5.4	58	P5.4						
C7	P5.5	59	P5.5	55	P5.5				
A6	P5.6								
B6	P5.7								
A2	VDDA	60	VDDA	56	VDDA	40	VDDA	40	VDDA
B2	VDDA	60	VDDA	56	VDDA	40	VDDA	40	VDDA

124-BGA		68-QFN		64-TQFP		48-TQFP		48-TQFP-USB	
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
M3	P3.3	22	P3.3	21	P3.3	16	P3.3	16	P3.3
N4	P3.4	23	P3.4	22	P3.4	17	P3.4	17	P3.4
M4	P3.5	24	P3.5	23	P3.5	18	P3.5	18	P3.5
N5	P3.6	25	P3.6	24	P3.6	19	P3.6	19	P3.6
M5	P3.7	26	P3.7	25	P3.7	20	P3.7	20	P3.7
M1	VDDIO	27	VDDIO	26	VDDIO	21	VDDIO	21	VDDIO
N1	VDDIO	27	VDDIO	26	VDDIO	21	VDDIO	21	VDDIO
N6	P11.0								
M6	P11.1								
L6	P11.2								
N7	P11.3								
M7	P11.4								
L7	P11.5								
N8	P11.6								
M8	P11.7								
N12	VDDIO	27	VDDIO	26	VDDIO	21	VDDIO	21	VDDIO
N13	VDDIO	27	VDDIO	26	VDDIO	21	VDDIO	21	VDDIO
L8	P4.0	28	P4.0	27	P4.0	22	P4.0	22	P4.0
N9	P4.1	29	P4.1	28	P4.1	23	P4.1		
M9	P4.2	30	P4.2	29	P4.2	24	P4.2		
N10	P4.3	31	P4.3	30	P4.3	25	P4.3		
M10	P4.4	32	P4.4	31	P4.4				
N11	P4.5	33	P4.5	32	P4.5				
M11	P4.6	34	P4.6	33	P4.6				
M12	P4.7	35	P4.7						
L11	VSSD								
L12	D+/P13.0	36	D+/P13.0	34	D+/P13.0			23	D+/P13.0
L13	D-/P13.1	37	D-/P13.1	35	D-/P13.1			24	D-/P13.1
M13	VBUS/P13.2	38	VBUS/P13.2	36	VBUS/P13.2			25	VBUS/P13.2
L9	P7.0	39	P7.0	37	P7.0	26	P7.0	26	P7.0
L10	P7.1	40	P7.1	38	P7.1	27	P7.1	27	P7.1
K13	P7.2	41	P7.2						
K12	P7.3								
K11	P7.4								
J13	P7.5								
J12	P7.6								
J11	P7.7								

Port 12 (Port pins 12.0 and 12.1) are SIO pins.

Ports 6 (Port pins P6.0..6.5) and 9 (Port pins 9.0..9.7) are overvoltage tolerant (GPIO_OVT)

Balls C6, D11, H11, H3, L4, and L5 are No Connects (NC) on the 124-BGA package. Pins 11 and 15 are NC on the 48-TQFP packages.

Each of the pins shown in the previous table can have multiple programmable functions as shown in the following table.

Port/Pin	Analog	PRGIO & USB	Alt. Function 1	Alt. Function 2	Alt. Function 3	Alt. Function 4	Alt. Function 5
P0.0	lpcomp.in_p[0]				can[1].can_rx:0	usb.vbus_valid	scb[0].spi_select1:3
P0.1	lpcomp.in_n[0]				can[1].can_tx:0		scb[0].spi_select2:3
P0.2	lpcomp.in_p[1]						scb[0].spi_select3:3
P0.3	lpcomp.in_n[1]						
P0.4	wco_in			scb[1].uart_rx:0		scb[1].i2c_scl:0	scb[1].spi_mosi:0
P0.5	wco_out			scb[1].uart_tx:0		scb[1].i2c_sda:0	scb[1].spi_miso:0
P0.6			srss.ext_clk:0	scb[1].uart_cts:0			scb[1].spi_clk:0
P0.7				scb[1].uart_rts:0	can[1].can_tx_enb_n:0	srss.wakeup	scb[1].spi_select0:0
P8.0				scb[3].uart_rx:0		scb[3].i2c_scl:0	scb[3].spi_mosi:0
P8.1				scb[3].uart_tx:0		scb[3].i2c_sda:0	scb[3].spi_miso:0
P8.2				scb[3].uart_cts:0		lpcomp.comp[0]:0	scb[3].spi_clk:0
P8.3				scb[3].uart_rts:0		lpcomp.comp[1]:0	scb[3].spi_select0:0
P8.4							scb[3].spi_select1:0
P8.5							scb[3].spi_select2:0
P8.6							scb[3].spi_select3:0
P8.7							
P9.0			tcpwm.line[0]:2	scb[0].uart_rx:0		scb[0].i2c_scl:0	scb[0].spi_mosi:0
P9.1			tcpwm.line_compl[0]:2	scb[0].uart_tx:0		scb[0].i2c_sda:0	scb[0].spi_miso:0
P9.2			tcpwm.line[1]:2	scb[0].uart_cts:0			scb[0].spi_clk:0
P9.3			tcpwm.line_compl[1]:2	scb[0].uart_rts:0			scb[0].spi_select0:0
P9.4			tcpwm.line[2]:2				scb[0].spi_select1:0
P9.5			tcpwm.line_compl[2]:2				scb[0].spi_select2:0
P9.6			tcpwm.line[3]:2			scb[3].i2c_scl:3	scb[0].spi_select3:0
P9.7			tcpwm.line_compl[3]:2			scb[3].i2c_sda:3	
P5.0	ctb1_pads[0] csd[1].c_mod		tcpwm.line[4]:2	scb[2].uart_rx:0		scb[2].i2c_scl:0	scb[2].spi_mosi:0
P5.1	ctb1_pads[1] csd[1].c_sh_tank		tcpwm.line_compl[4]:2	scb[2].uart_tx:0		scb[2].i2c_sda:0	scb[2].spi_miso:0
P5.2	ctb1_pads[2] ctb1_oa0_out_10x		tcpwm.line[5]:2	scb[2].uart_cts:0		lpcomp.comp[0]:1	scb[2].spi_clk:0
P5.3	ctb1_pads[3] ctb1_oa1_out_10x		tcpwm.line_compl[5]:2	scb[2].uart_rts:0		lpcomp.comp[1]:1	scb[2].spi_select0:0
P5.4	ctb1_pads[4]		tcpwm.line[6]:2				scb[2].spi_select1:0
P5.5	ctb1_pads[5]		tcpwm.line_compl[6]:2				scb[2].spi_select2:0
P5.6	ctb1_pads[6]		tcpwm.line[7]:2				scb[2].spi_select3:0
P5.7	ctb1_pads[7]		tcpwm.line_compl[7]:2				
P1.0	ctb0_pads[0]		tcpwm.line[2]:1	scb[0].uart_rx:1		scb[0].i2c_scl:1	scb[0].spi_mosi:1
P1.1	ctb0_pads[1]		tcpwm.line_compl[2]:1	scb[0].uart_tx:1		scb[0].i2c_sda:1	scb[0].spi_miso:1
P1.2	ctb0_pads[2] ctb0_oa0_out_10x		tcpwm.line[3]:1	scb[0].uart_cts:1			scb[0].spi_clk:1
P1.3	ctb0_pads[3] ctb0_oa1_out_10x		tcpwm.line_compl[3]:1	scb[0].uart_rts:1			scb[0].spi_select0:1
P1.4	ctb0_pads[4]		tcpwm.line[6]:1				scb[0].spi_select1:1

Port/Pin	Analog	PRGIO & USB	Alt. Function 1	Alt. Function 2	Alt. Function 3	Alt. Function 4	Alt. Function 5
P1.5	ctb0_pads[5]		tcpwm.line_compl[6]:1				scb[0].spi_select2:1
P1.6	ctb0_pads[6]		tcpwm.line[7]:1				scb[0].spi_select3:1
P1.7	ctb0_pads[7], sar_ext_vref		tcpwm.line_compl[7]:1				
P2.0	sarmux_pads[0]		tcpwm.line[4]:1	scb[1].uart_rx:1		scb[1].i2c_scl:1	scb[1].spi_mosi:1
P2.1	sarmux_pads[1]		tcpwm.line_compl[4]:1	scb[1].uart_tx:1		scb[1].i2c_sda:1	scb[1].spi_miso:1
P2.2	sarmux_pads[2]		tcpwm.line[5]:1	scb[1].uart_cts:1			scb[1].spi_clk:1
P2.3	sarmux_pads[3]		tcpwm.line_compl[5]:1	scb[1].uart_rts:1			scb[1].spi_select0:1
P2.4	sarmux_pads[4]		tcpwm.line[0]:1				scb[1].spi_select1:0
P2.5	sarmux_pads[5]		tcpwm.line_compl[0]:1				scb[1].spi_select2:0
P2.6	sarmux_pads[6]		tcpwm.line[1]:1				scb[1].spi_select3:0
P2.7	sarmux_pads[7]		tcpwm.line_compl[1]:1				
P10.0				scb[2].uart_rx:1		scb[2].i2c_scl:1	scb[2].spi_mosi:1
P10.1				scb[2].uart_tx:1		scb[2].i2c_sda:1	scb[2].spi_miso:1
P10.2				scb[2].uart_cts:1			scb[2].spi_clk:1
P10.3				scb[2].uart_rts:1			scb[2].spi_select0:1
P10.4							scb[2].spi_select1:1
P10.5							scb[2].spi_select2:1
P10.6							scb[2].spi_select3:1
P10.7							
P6.0			tcpwm.line[4]:0	scb[3].uart_rx:1	can[0].can_tx_enb_n:0	scb[3].i2c_scl:1	scb[3].spi_mosi:1
P6.1			tcpwm.line_compl[4]:0	scb[3].uart_tx:1	can[0].can_rx:0	scb[3].i2c_sda:1	scb[3].spi_miso:1
P6.2			tcpwm.line[5]:0	scb[3].uart_cts:1	can[0].can_tx:0	scb[2].i2c_scl:3	scb[3].spi_clk:1
P6.3			tcpwm.line_compl[5]:0	scb[3].uart_rts:1		scb[2].i2c_sda:3	scb[3].spi_select0:1
P6.4			tcpwm.line[6]:0			scb[0].i2c_scl:3	scb[3].spi_select1:1
P12.0			tcpwm.line[7]:0			scb[1].i2c_scl:3	scb[3].spi_select3:1
P12.1			tcpwm.line_compl[7]:0			scb[1].i2c_sda:3	
P6.5			tcpwm.line_compl[6]:0			scb[0].i2c_sda:3	scb[3].spi_select2:1
P3.0			tcpwm.line[0]:0	scb[1].uart_rx:2		scb[1].i2c_scl:2	scb[1].spi_mosi:2
P3.1			tcpwm.line_compl[0]:0	scb[1].uart_tx:2		scb[1].i2c_sda:2	scb[1].spi_miso:2
P3.2			tcpwm.line[1]:0	scb[1].uart_cts:2		cpuss.swd_data:0	scb[1].spi_clk:2
P3.3			tcpwm.line_compl[1]:0	scb[1].uart_rts:2		cpuss.swd_clk:0	scb[1].spi_select0:2
P3.4			tcpwm.line[2]:0				scb[1].spi_select1:1
P3.5			tcpwm.line_compl[2]:0				scb[1].spi_select2:1
P3.6			tcpwm.line[3]:0				scb[1].spi_select3:1
P3.7			tcpwm.line_compl[3]:0				
P11.0		prgio[0].io[0]	tcpwm.line[4]:3	scb[2].uart_rx:2		scb[2].i2c_scl:2	scb[2].spi_mosi:2
P11.1		prgio[0].io[1]	tcpwm.line_compl[4]:3	scb[2].uart_tx:2		scb[2].i2c_sda:2	scb[2].spi_miso:2
P11.2		prgio[0].io[2]	tcpwm.line[5]:3	scb[2].uart_cts:2		cpuss.swd_data:1	scb[2].spi_clk:2
P11.3		prgio[0].io[3]	tcpwm.line_compl[5]:3	scb[2].uart_rts:2		cpuss.swd_clk:1	scb[2].spi_select0:2
P11.4		prgio[0].io[4]	tcpwm.line[6]:3				scb[2].spi_select1:2
P11.5		prgio[0].io[5]	tcpwm.line_compl[6]:3				scb[2].spi_select2:2
P11.6		prgio[0].io[6]	tcpwm.line[7]:3				scb[2].spi_select3:2
P11.7		prgio[0].io[7]	tcpwm.line_compl[7]:3				
P4.0				scb[0].uart_rx:2	can[0].can_rx:1	scb[0].i2c_scl:2	scb[0].spi_mosi:2
P4.1				scb[0].uart_tx:2	can[0].can_tx:1	scb[0].i2c_sda:2	scb[0].spi_miso:2

Port/Pin	Analog	PRGIO & USB	Alt. Function 1	Alt. Function 2	Alt. Function 3	Alt. Function 4	Alt. Function 5
P4.2	csd[0].c_mod			scb[0].uart_cts:2	can[0].can_tx_enb_n:1	lpcomp.comp[0]:2	scb[0].spi_clk:2
P4.3	csd[0].c_sh_tank			scb[0].uart_rts:2		lpcomp.comp[1]:2	scb[0].spi_select0:2
P4.4					can[1].can_tx_enb_n:1		scb[0].spi_select1:2
P4.5					can[1].can_rx:1		scb[0].spi_select2:2
P4.6					can[1].can_tx:1		scb[0].spi_select3:2
P4.7							
P13.0		USBDP					
P13.1		USBDM					
P13.2		VBUS					
P7.0	srss.eco_in		tcpwm.line[0]:3	scb[3].uart_rx:2		scb[3].i2c_scl:2	scb[3].spi_mosi:2
P7.1	srss.eco_out		tcpwm.line_compl[0]:3	scb[3].uart_tx:2		scb[3].i2c_sda:2	scb[3].spi_miso:2
P7.2			tcpwm.line[1]:3	scb[3].uart_cts:2			scb[3].spi_clk:2
P7.3			tcpwm.line_compl[1]:3	scb[3].uart_rts:2			scb[3].spi_select0:2
P7.4			tcpwm.line[2]:3				scb[3].spi_select1:2
P7.5			tcpwm.line_compl[2]:3				scb[3].spi_select2:2
P7.6			tcpwm.line[3]:3				scb[3].spi_select3:2
P7.7			tcpwm.line_compl[3]:3				

Descriptions of the power pin functions are as follows:

VDDD: Power supply for both analog and digital sections (where there is no V_{DDA} pin)

VDDA: Analog V_{DD} pin where package pins allow; shorted to V_{DDD} otherwise

VDDIO: I/O pin power domain

VSSA: Analog ground pin where package pins allow; shorted to VSS otherwise

VSS: Ground pin

VCCD: Regulated digital supply (1.8 V ±5%)

GPIO and GPIO_OVT pins can be used as CSD sense and shield pins (a total of 94). Up to 64 of the pins can be used for LCD drive.

The following packages are supported: 124-ball BGA, 64-pin TQFP, 68-pin QFN, and 48-pin TQFP.

Power

The supply voltage range is 1.71 V to 5.5 V with all functions and circuits operating over that range.

The PSoC 4200-L family allows two distinct modes of power supply operation: Unregulated External Supply and Regulated External Supply modes.

Unregulated External Supply

In this mode, the PSoC 4200-L is powered by an External Power Supply that can be anywhere in the range of 1.8 V to 5.5 V. This range is also designed for battery-powered operation, for instance, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of the PSoC 4200-L supplies the internal logic and the VCCD output of the PSoC 4200-L must be bypassed to ground via an external Capacitor (in the range of 1 to 1.6 µF; X5R ceramic or better).

VDDA and VDDD must be shorted together on the PC board; the grounds, VSSA and VSS must also be shorted together. Bypass capacitors must be used from VDDD and VDDA to ground, typical practice for systems in this frequency range is to use a capacitor in the 1 µF range in parallel with a smaller capacitor (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

Power Supply	Bypass Capacitors
VDDD–VSS and VDDIO-VSS	0.1 µF ceramic at each pin plus bulk capacitor 1 to 10 µF.
VDDA–VSSA	0.1 µF ceramic at pin. Additional 1 µF to 10 µF bulk capacitor
VCCD–VSS	1 µF ceramic capacitor at the VCCD pin
VREF–VSSA (optional)	The internal bandgap may be bypassed with a 1 µF to 10 µF capacitor for better ADC performance.

Regulated External Supply

In this mode, the PSoC 4200-L is powered by an external power supply that must be within the range of 1.71 V to 1.89 V (1.8 ±5%); note that this range needs to include power supply ripple. In this mode, the VCCD and VDDD pins are shorted together and bypassed. The internal regulator is disabled in firmware.

Development Support

The PSoC 4200-L family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit www.cypress.com/go/psoc4 to find out more.

Documentation

A suite of documentation supports the PSoC 4200-L family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

Component Datasheets: The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

Application Notes: PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

Technical Reference Manual: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers.

Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 4200-L family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

Table 5. GPIO AC Specifications

(Guaranteed by Characterization)[3]

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID70	T_{RISEF}	Rise time in fast strong mode	2	–	12	ns	3.3 V V_{DDD}, Cload = 25 pF
SID71	T_{FALLF}	Fall time in fast strong mode	2	–	12	ns	3.3 V V_{DDD}, Cload = 25 pF
SID72	T_{RISES}	Rise time in slow strong mode	10	–	60	ns	3.3 V V_{DDD}, Cload = 25 pF
SID73	T_{FALLS}	Fall time in slow strong mode	10	–	60	ns	3.3 V V_{DDD}, Cload = 25 pF
SID74	$F_{GPIOUT1}$	GPIO Fout;3.3 V ≤ V_{DDD} ≤ 5.5 V. Fast strong mode.	–	–	33	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO Fout;1.7 V≤ V_{DDD}≤ 3.3 V. Fast strong mode.	–	–	16.7	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID76	$F_{GPIOUT3}$	GPIO Fout;3.3 V ≤ V_{DDD} ≤ 5.5 V. Slow strong mode.	–	–	7	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID245	$F_{GPIOUT4}$	GPIO Fout;1.7 V ≤ V_{DDD} ≤ 3.3 V. Slow strong mode.	–	–	3.5	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID246	F_{GPIOIN}	GPIO input operating frequency; 1.71 V ≤ V_{DDD} ≤ 5.5 V	–	–	48	MHz	90/10% V_{IO}

XRES

Table 6. XRES DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID77	V_{IH}	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS Input
SID78	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}	V	CMOS Input
SID79	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID80	C_{IN}	Input capacitance	–	3	–	pF	
SID81	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	Guaranteed by characterization
SID82	I_{DIODE}	Current through protection diode to V_{DDD}/V_{SS}	–	–	100	µA	Guaranteed by characterization

Table 7. XRES AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID83	$T_{RESETWIDTH}$	Reset pulse width	1	–	–	µs	Guaranteed by characterization

Note

3. Simultaneous switching transitions on many fully-loaded GPIO pins may cause ground perturbations depending on several factors including PCB and decoupling capacitor design. For applications that are very sensitive to ground perturbations, the slower GPIO slew rate setting may be used.

Analog Peripherals

Opamp

Table 8. Opamp Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
	I_{DD}	Opamp block current. No load.	–	–	–	–	
SID269	I_{DD_HI}	Power = high	–	1100	1850	µA	
SID270	I_{DD_MED}	Power = medium	–	550	950	µA	
SID271	I_{DD_LOW}	Power = low	–	150	350	µA	
	GBW	Load = 20 pF, 0.1 mA. V_{DDA} = 2.7 V	–	–	–	–	
SID272	GBW_HI	Power = high	6	–	–	MHz	
SID273	GBW_MED	Power = medium	4	–	–	MHz	
SID274	GBW_LO	Power = low	–	1	–	MHz	
	I_{OUT_MAX}	$V_{DDA} \geq 2.7$ V, 500 mV from rail	–	–	–	–	
SID275	$I_{OUT\_MAX\_HI}$	Power = high	10	–	–	mA	
SID276	$I_{OUT\_MAX\_MID}$	Power = medium	10	–	–	mA	
SID277	$I_{OUT\_MAX\_LO}$	Power = low	–	5	–	mA	
	I_{OUT}	V_{DDA} = 1.71 V, 500 mV from rail	–	–	–	–	
SID278	$I_{OUT\_MAX\_HI}$	Power = high	4	–	–	mA	
SID279	$I_{OUT\_MAX\_MID}$	Power = medium	4	–	–	mA	
SID280	$I_{OUT\_MAX\_LO}$	Power = low	–	2	–	mA	
SID281	V_{IN}	Input voltage range	–0.05	–	V_{DDA}– 0.2	V	Charge-pump on, $V_{DDA} \geq$ 2.7 V
SID282	V_{CM}	Input common mode voltage	–0.05	–	VDDA – 0.2	V	Charge-pump on, $V_{DDA} \geq$ 2.7 V
	V_{OUT}	$V_{DDA} \geq 2.7$ V	–	–	–		
SID283	V_{OUT_1}	Power = high, I_{load}=10 mA	0.5	–	VDDA – 0.5	V	
SID284	V_{OUT_2}	Power = high, I_{load}=1 mA	0.2	–	VDDA – 0.2	V	
SID285	V_{OUT_3}	Power = medium, I_{load}=1 mA	0.2	–	VDDA – 0.2	V	
SID286	V_{OUT_4}	Power = low, I_{load}=0.1mA	0.2	–	VDDA – 0.2	V	
SID288	V_{OS_TR}	Offset voltage, trimmed	1	±0.5	1	mV	High mode
SID288A	V_{OS_TR}	Offset voltage, trimmed	–	±1	–	mV	Medium mode
SID288B	V_{OS_TR}	Offset voltage, trimmed	–	±2	–	mV	Low mode
SID290	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–10	±3	10	µV/°C	High mode
SID290A	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/°C	Medium mode
SID290B	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/°C	Low mode
SID291	CMRR	DC	60	70	–	dB	V_{DDD} = 3.6 V
SID292	PSRR	At 1 kHz, 100 mV ripple	70	85	–	dB	VDDD = 3.6 V
	Noise		–	–	–	–	
SID293	V_{N1}	Input referred, 1 Hz - 1GHz, power = high	–	94	–	µVrms	
SID294	V_{N2}	Input referred, 1 kHz, power = high	–	72	–	nV/rtHz	

Table 10. Comparator AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID91	T_{RESP1}	Response time, normal mode	–	38	110	ns	50-mV overdrive
SID258	T_{RESP2}	Response time, low power mode	–	70	200	ns	50-mV overdrive
SID92	T_{RESP3}	Response time, ultra low power mode	–	2.3	15	µs	200-mV overdrive. $V_{DDD} \geq 2.2$ V for Temp < 0 °C, $V_{DDD} \geq 1.8$ V for Temp > 0 °C

Temperature Sensor

Table 11. Temperature Sensor Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID93	$T_{SENSACC}$	Temperature sensor accuracy	–5	±1	+5	°C	–40 to +85 °C

SAR ADC

Table 12. SAR ADC DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID94	A_RES	Resolution	–	–	12	bits	
SID95	A_CHNIS_S	Number of channels - single ended	–	–	16		8 full speed
SID96	A-CHNKS_D	Number of channels - differential	–	–	8		Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity	–	–	–		Yes. Based on characterization
SID98	A_GAINERR	Gain error	–	–	±0.1	%	With external reference.
SID99	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V V_{REF}.
SID100	A_ISAR	Current consumption	–	–	1	mA	
SID101	A_VINS	Input voltage range - single ended	V_{SS}	–	V_{DDA}	V	Based on device characterization
SID102	A_VIND	Input voltage range - differential	V_{SS}	–	V_{DDA}	V	Based on device characterization
SID103	A_INRES	Input resistance	–	–	2.2	KΩ	Based on device characterization
SID104	A_INCAP	Input capacitance	–	–	10	pF	Based on device characterization

Table 13. SAR ADC AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID106	A_PSRR	Power supply rejection ratio	70	–	–	dB	
SID107	A_CMRR	Common mode rejection ratio	66	–	–	dB	Measured at 1 V
SID108	A_SAMP_1	Sample rate with external reference bypass cap	–	–	1	Msps	
SID108A	A_SAMP_2	Sample rate with no bypass cap. Reference = V_{DD}	–	–	500	Ksps	

Memory

Table 26. Flash DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID173	V_{PE}	Erase and program voltage	1.71	–	5.5	V	

Table 27. Flash AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID174	$T_{ROWWRITE}$	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 256 bytes
SID175	$T_{ROWERASE}$	Row erase time	–	–	13	ms	
SID176	$T_{ROWPROGRAM}$	Row program time after erase	–	–	7	ms	
SID178	$T_{BULKERASE}$	Bulk erase time (128 KB)	–	–	35	ms	
SID180	$T_{DEVPROG}$	Total device program time	–	–	15	seconds	Guaranteed by characterization
SID181	F_{END}	Flash endurance	100 K	–	–	cycles	Guaranteed by characterization
SID182	F_{RET}	Flash retention. $T_A \leq 55$ °C, 100 K P/E cycles	20	–	–	years	Guaranteed by characterization
SID182A		Flash retention. $T_A \leq 85$ °C, 10 K P/E cycles	10	–	–	years	Guaranteed by characterization

Table 40. Watch Crystal Oscillator (WCO) Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
WCO Specifications							
SID398	FWCO	Crystal frequency	–	32.768	–	kHz	
SID399	FTOL	Frequency tolerance	–	50	250	ppm	With 20-ppm crystal.
SID400	ESR	Equivalent series resistance	–	50	–	kΩ	
SID401	PD	Drive Level	–	–	1	µW	
SID402	TSTART	Startup time	–	–	500	ms	
SID403	CL	Crystal load capacitance	6	–	12.5	pF	
SID404	C0	Crystal shunt capacitance	–	1.35	–	pF	
SID405	IWCO1	Operating current (high power mode)	–	–	8	uA	

Table 41. External Crystal Oscillator (ECO) Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID316	IECO1	Block operating current	–	–	1.5	mA	
SID317	FECO	Crystal frequency range	4	–	33	MHz	

Table 42. UDB AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Datapath performance							
SID249	$F_{MAX-TIMER}$	Max frequency of 16-bit timer in a UDB pair	–	–	48	MHz	
SID250	$F_{MAX-ADDER}$	Max frequency of 16-bit adder in a UDB pair	–	–	48	MHz	
SID251	F_{MAX_CRC}	Max frequency of 16-bit CRC/PRS in a UDB pair	–	–	48	MHz	
PLD Performance in UDB							
SID252	F_{MAX_PLD}	Max frequency of 2-pass PLD function in a UDB pair	–	–	48	MHz	
Clock to Output Performance							
SID253	$T_{CLK\_OUT\_UDB1}$	Prop. delay for clock in to data out at 25 °C, Typ.	–	15	–	ns	
SID254	$T_{CLK\_OUT\_UDB2}$	Prop. delay for clock in to data out, Worst case.	–	25	–	ns	

Table 46. SIO Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID358	F_{SIOUT3}	SIO Fout; Unregulated, Slow Strong mode.	–	–	5	MHz	3.3 V ≤ V_{DD} ≤ 5.5 V, 25 pF
SID359	F_{SIOUT4}	SIO Fout, Unregulated, Slow Strong mode.	–	–	3.5	MHz	1.71 V ≤ V_{DD} ≤ 3.3 V, 25 pF
SID360	F_{SIOUT5}	SIO Fout, Regulated, Slow Strong mode.	–	–	2.5	MHz	1.7 V ≤ V_{DD} ≤ 5.5 V, 25 pF
SID361	F_{GPIOIN}	GPIO input operating frequency;1.71 V ≤ V_{DD} ≤ 5.5 V	–	–	48	MHz	1.71 V ≤ V_{DD} ≤ 5.5 V

Table 47. CAN Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / Conditions
SID420	IDD_CAN	Block current consumption	–	–	200	uA	
SID421	CAN_bits	CAN Bit rate (Min 8-MHz clock)	–	–	1	Mbps	

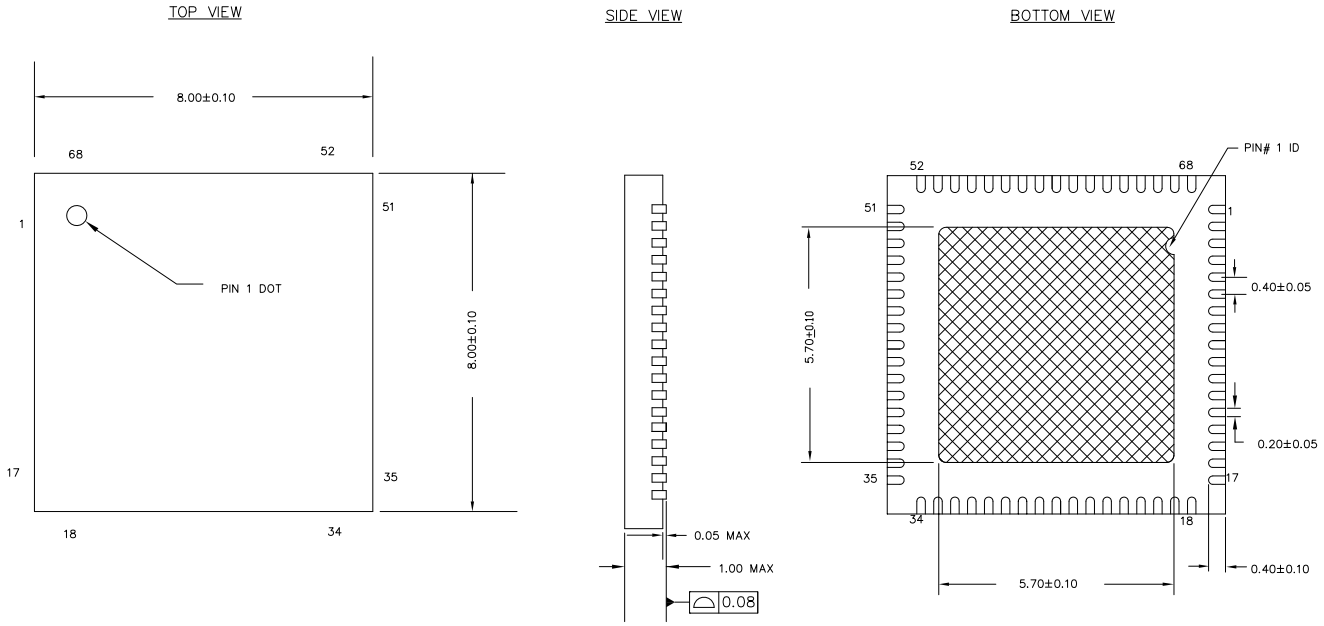
Ordering Information

The PSoC 4200-L family part numbers and features are listed in the following table.

Table 48. PSoC 4200-L Ordering Information

Category	MPN	Features														Package			
		Max CPU Speed (MHz)	Flash (KB)	SRAM (KB)	UDB	Op-amp (CTBm)	CSD	Direct LCD Drive	12-bit SAR ADC	LP Comparators	TCPWM Blocks	SCB Blocks	USB Full Speed	CAN	GPIO	48-TQFP	64-TQFP	68-QFN	124-VFBGA
4246	CY8C4246AZI-L423	48	64	8	8	2	1	✔	1000 ksps	2	8	3	–	–	38	✔	–	–	–
	CY8C4246AZI-L433	48	64	8	8	2	–	–	1000 ksps	2	8	3	✔	–	38	✔	–	–	–
	CY8C4246AZI-L435	48	64	8	8	2	–	–	1000 ksps	2	8	4	✔	–	53	–	✔	–	–
	CY8C4246AZI-L445	48	64	8	8	2	2	✔	1000 ksps	2	8	4	✔	–	53	–	✔	–	–
	CY8C4246LTI-L445	48	64	8	8	2	2	✔	1000 ksps	2	8	4	✔	–	57	–	–	✔	–
4247	CY8C4247AZI-L423	48	128	16	8	2	1	✔	1000 ksps	2	8	3	–	–	38	✔	–	–	–
	CY8C4247AZI-L433	48	128	16	8	2	–	–	1000 ksps	2	8	3	✔	–	38	✔	–	–	–
	CY8C4247AZI-L445	48	128	16	8	2	2	✔	1000 ksps	2	8	4	✔	–	53	–	✔	–	–
	CY8C4247LTI-L445	48	128	16	8	2	2	✔	1000 ksps	2	8	4	✔	–	57	–	–	✔	–
	CY8C4247AZI-L475	48	128	16	8	4	2	–	1000 ksps	2	8	4	✔	–	53	–	✔	–	–
	CY8C4247LTI-L475	48	128	16	8	4	2	–	1000 ksps	2	8	4	✔	–	57	–	–	✔	–
	CY8C4247BZI-L479	48	128	16	8	4	2	–	1000 ksps	2	8	4	✔	–	98	–	–	–	✔
	CY8C4247AZI-L485	48	128	16	8	4	2	✔	1000 ksps	2	8	4	✔	✔	53	–	✔	–	–
	CY8C4247LTI-L485	48	128	16	8	4	2	✔	1000 ksps	2	8	4	✔	✔	57	–	–	✔	–
	CY8C4247BZI-L489	48	128	16	8	4	2	✔	1000 ksps	2	8	4	✔	✔	98	–	–	–	✔
4248	CY8C4248BZI-L469	48	256	32	8	4	–	–	1000 ksps	2	8	4	–	–	96	–	–	–	✔
	CY8C4248AZI-L475	48	256	32	8	4	2	–	1000 ksps	2	8	4	✔	–	53	–	✔	–	–
	CY8C4248LTI-L475	48	256	32	8	4	2	–	1000 ksps	2	8	4	✔	–	57	–	–	✔	–
	CY8C4248BZI-L479	48	256	32	8	4	2	–	1000 ksps	2	8	4	✔	–	98	–	–	–	✔
	CY8C4248AZI-L485	48	256	32	8	4	2	✔	1000 ksps	2	8	4	✔	✔	53	–	✔	–	–
	CY8C4248LTI-L485	48	256	32	8	4	2	✔	1000 ksps	2	8	4	✔	✔	57	–	–	✔	–
	CY8C4248BZI-L489	48	256	32	8	4	2	✔	1000 ksps	2	8	4	✔	✔	98	–	–	–	✔

Figure 10. 68-Pin QFN Package Outline

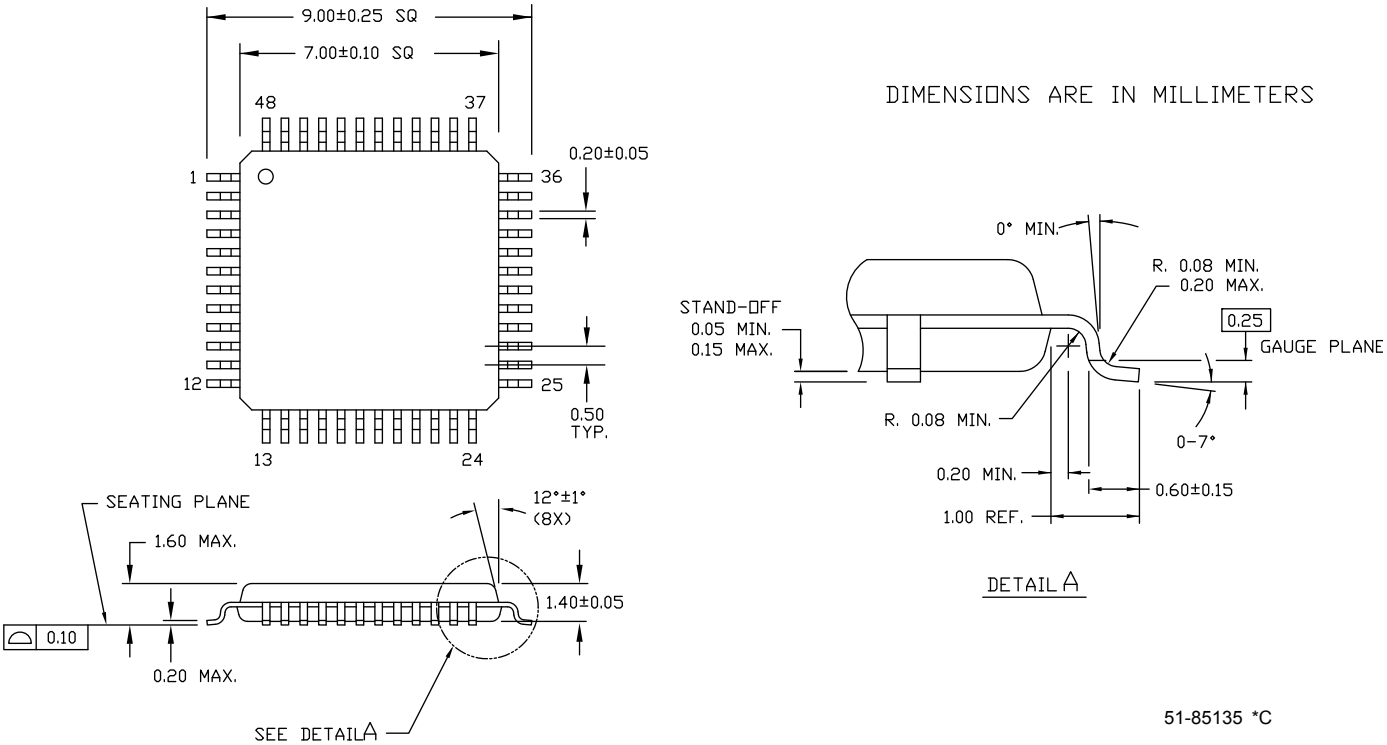


NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 17 ± 2mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-09618 *E

Figure 11. 48-Pin TQFP Package Outline



51-85135 *C

Table 52. Acronyms Used in this Document *(continued)*

Acronym	Description
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol

Table 52. Acronyms Used in this Document *(continued)*

Acronym	Description
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

Revision History

Description Title: PSoC® 4: PSoC 4200-L Family Datasheet Programmable System-on-Chip (PSoC®) Document Number: 001-91686				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	4414601	WKA	02/06/2015	New datasheet for new device family.
*A	4774497	WKA	05/22/2015	Updated Pin List. Added a footnote explaining ground perturbations in GPIO AC Specifications. Updated values for SID269, SID270, SID271, and SID291. Added Conditions for Deep Sleep Mode in Opamp Specifications. Updated Conditions for SID_DS_10 through SID_DS_18. Added Conditions for SID_DS_22 through SID_DS_24. Updated description for SID85 and SID85A. Updated values for SID89, SID248, SID259, SID91, SID258, and SID92. Updated max value for SID.TCPWM.2A. Updated typ and max values for SID149. Added PLL DC Specifications and PLL AC Specifications. Updated Watch Crystal Oscillator (WCO) Specifications. Added CAN Specifications. Changed µFBGA package to VFBGA package.
*B	4867142	WKA	08/03/2015	Changed datasheet status to Preliminary. Updated Pinouts. Removed typ value for SID43. Updated Conditions for SID_DS_7, SID_DS_8, and SID_DS_9. Updated max value for SID87. Removed SID179. Added External Crystal Oscillator (ECO) Specifications. Updated max value for SID321, SID353, and SID359. Added “Guaranteed by Design” note for SID354. Updated Ordering Information.
*C	5034067	WKA	12/03/2015	Updated Conditions for SID85A, SID247A, SID259, SID92, SID417, SID416A Updated typ and max values for SID410. Updated description for SID323. Added “Guaranteed by Characterization” note for SIO AC Specs. Updated Ordering Information.
*D	5170871	WKA	03/11/2016	Removed VDDA and VDDIO pins in Regulated External Supply section. Updated values for Deep Sleep Mode, Hibernate Mode and Stop Mode in DC Specifications. Added SID299A. Added a note in UDB Port Adaptor Specifications that all specs except TLCLKDO are guaranteed by design. Updated T_{JA} value for the 124-VFBGA package.
*E	5281150	WKA	05/23/2016	Changed datasheet status to Final. Updated max values for SID6, SID7, SID8, SID9, SID31, SID32, SID34, SID35, SID40, SID41, SID43, and SID44. Updated the template.
*F	5516529	WKA	11/15/2016	Added CY8C4248BZI-L469 in Ordering Information.
*G	5559970	WKA	11/20/2016	Updated max values for SID33, SID34, and SID35. Updated SID171.