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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	CSIO, EBI/EMI, I²C, LINbus, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	83
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/rochester-electronics/mb9bf314npmc-g-jne2

Real-time clock (RTC)

The Real-time clock can count Year/Month/Day/Hour/Minute/Second/A day of the week from 01 to 99.

- Interrupt function with specifying date and time (Year/Month/Day/Hour/Minute/Second/A day of the week.) is available. This function is also available by specifying only Year, Month, Day, Hour or Minute.
- Timer interrupt function after set time or each set time.
- Capable of rewriting the time with continuing the time count.
- Leap year automatic count is available.

Quadrature Position/Revolution Counter (QPRC) (Max three channels)

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. Moreover, it is possible to use up/down counter.

- The detection edge of the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

Dual Timer (32-/16-bit Down Counter)

The Dual Timer consists of two programmable 32-/16-bit down counters.
Operation mode is selectable from the followings for each channel.

- Free-running
- Periodic (=Reload)
- One-shot

Watch Counter

The Watch counter is used for wake up from power consumption mode.

- Interval timer: up to 64 s (Max) @ Sub Clock : 32.768 kHz

External Interrupt Controller Unit

- Up to 16 external interrupt input pin
- Include one non-maskable interrupt (NMI)

Watchdog Timer (Two channels)

A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a "Hardware" watchdog and a "Software" watchdog.

"Hardware" watchdog timer is clocked by low-speed internal CR oscillator. Therefore, "Hardware" watchdog is active in any power consumption mode except Stop mode.

CRC (Cyclic Redundancy Check) Accelerator

The CRC accelerator helps a verify data transmission or storage integrity.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 Generator Polynomial: 0x1021
- IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

Clock and Reset

- Clocks

Five clock sources (2 external oscillators, 2 internal CR oscillator, and Main PLL) that are dynamically selectable.

  - Main Clock: 4 MHz to 48 MHz
  - Sub Clock: 32.768 kHz
  - High-speed internal CR Clock: 4 MHz
  - Low-speed internal CR Clock: 100 kHz

- Resets
  - Reset requests from INITX pin
  - Power on reset
  - Software reset
  - Watchdog timers reset
  - Low-voltage detector reset
  - Clock supervisor reset

Clock Super Visor (CSV)

Clocks generated by internal CR oscillators are used to supervise abnormality of the external clocks.

- External OSC clock failure (clock stop) is detected, reset is asserted.
- External OSC frequency anomaly is detected, interrupt or reset is asserted.

Low-Voltage Detector (LVD)

This Series include 2-stage monitoring of voltage on the VCC pins. When the voltage falls below the voltage has been set, Low-Voltage Detector generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

Low-Power Consumption Mode

Three power consumption modes supported.

- Sleep
- Timer
- Stop

Debug

- Serial Wire JTAG Debug Port (SWJ-DP)
- Embedded Trace Macrocells (ETM) provide comprehensive debug and trace facilities.

Power Supply

- Two Power Supplies
  - Wide range voltage:
    VCC = 2.7 V to 5.5 V
  - USB for USB I/O voltage:
    USBVCC = 3.0 V to 3.6 V (when USB is used)
    = 2.7 V to 5.5 V (when GPIO is used)

Table of Contents

Note:

- *All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the General I/O port according to your function use. See "12 Electrical Characteristics 12.4 AC Characteristics 12.4.3 Internal CR Oscillation Characteristics" for accuracy of built-in CR.*

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-100	FBGA-112	LQFP-120	QFP-100			
56	H9	66	34	P14 AN04 SIN0_1 INT03_1 IC02_2 MAD12_0	F	L
57	H7	67	35	P15 AN05 SOT0_1 (SDA0_1) IC03_2 MAD13_0	F	K
58	G10	68	36	P16 AN06 SCK0_1 (SCL0_1) MAD14_0	F	K
59	G9	69	37	P17 AN07 SIN2_2 INT04_1 MAD15_0	F	L
60	H11	70	38	AVCC	-	
61	F11	71	39	AVRH	-	
62	G11	72	40	AVSS	-	
63	G8	73	41	P18 AN08 SOT2_2 (SDA2_2) MAD16_0	F	K
64	F10	74	42	P19 AN09 SCK2_2 (SCL2_2) MAD17_0	F	K
65	F9	75	43	P1A AN10 SIN4_1 INT05_1 IC00_1 MAD18_0	F	L
-	H8	-	-	VSS	-	
66	E11	76	44	P1B AN11 SOT4_1 (SDA4_1) IC01_1 MAD19_0	F	K
67	E10	77	45	P1C AN12 SCK4_1 (SCL4_1) IC02_1 MAD20_0	F	K

Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-100	FBGA-112	LQFP-120	QFP-100			
74	C10	89	52	P20 INT05_0 CROUT_0 AIN1_1 MAD24_0	E	H
75	A11	90	53	VSS	-	
76	A10	91	54	VCC	-	
77	A9	92	55	P00 TRSTX MCSX7_0	E	E
78	B9	93	56	P01 TCK SWCLK	E	E
79	B11	94	57	P02 TDI MCSX6_0	E	E
80	A8	95	58	P03 TMS SWDIO	E	E
81	B8	96	59	P04 TDO SWO	E	E
82	C8	97	60	P05 TRACED0 TIOA5_2 SIN4_2 INT00_1 MCSX5_0	E	F
-	D8	-	-	VSS	-	
83	D9	98	61	P06 TRACED1 TIOB5_2 SOT4_2 (SDA4_2) INT01_1 AIN2_1 MCSX4_0	E	F
84	A7	99	62	P07 TRACED2 ADTG_0 SCK4_2 (SCL4_2) BIN2_1 MCLKOUT_0	E	G
85	B7	100	63	P08 TRACED3 TIOA0_2 CTS4_2 ZIN2_1 MCSX3_0	E	G
86	C7	101	64	P09 TRACECLK TIOB0_2 RTS4_2 RTO20_1 (PPG20_1) MCSX2_0	E	G

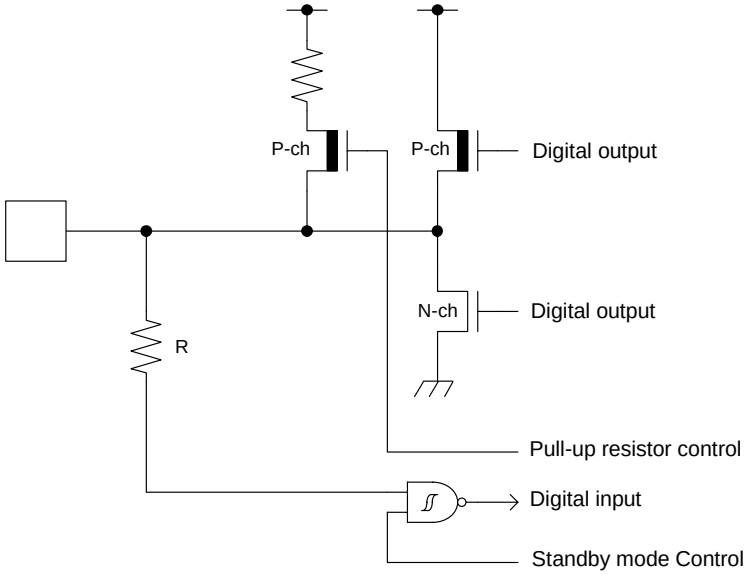
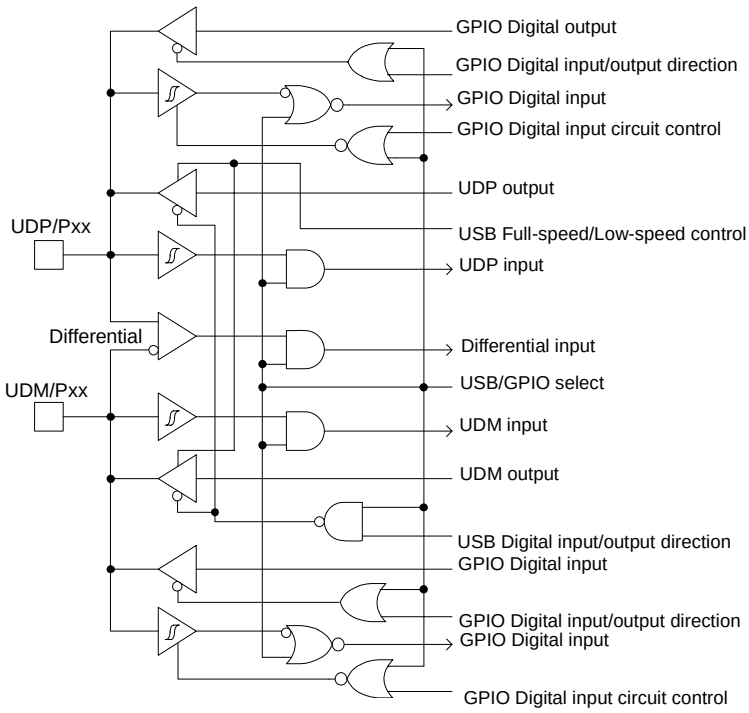
Pin No				Pin Name	I/O circuit type	Pin state type
LQFP-100	FBGA-112	LQFP-120	QFP-100			
95	B4	115	73	P61 SOT5_0 (SDA5_0) TIOB2_2 UHCONX	E	I
96	C4	116	74	P60 SIN5_0 TIOA2_2 INT15_1 MRDY_0	I*	H
97	A4	117	75	USBVCC	-	
98	A3	118	76	P80 UDM0	H	O
99	A2	119	77	P81 UDP0	H	O
100	A1	120	78	VSS	-	

*: 5 V tolerant I/O

Module	Pin name	Function	Pin No			
			LQFP-100	FBGA-112	LQFP-120	QFP-100
Clock	X0	Main clock (oscillation) input pin	48	L9	58	26
	X0A	Sub clock (oscillation) input pin	36	L3	41	14
	X1	Main clock (oscillation) I/O pin	49	L10	59	27
	X1A	Sub clock (oscillation) I/O pin	37	K3	42	15
	CROUT_0	Built-in high-speed CR-osc clock output port	74	C10	89	52
	CROUT_1		92	B5	107	70
Analog Power	AVCC	A/D converter analog power pin	60	H11	70	38
	AVRH	A/D converter analog reference voltage input pin	61	F11	71	39
Analog GND	AVSS	A/D converter GND pin	62	G11	72	40
C pin	C	Power stabilization capacity pin	33	L2	38	11

Note:

- *While this device contains a Test Access Port (TAP) based on the IEEE 1149.1-2001 JTAG standard, it is not fully compliant to all requirements of that standard. This device may contain a 32-bit device ID that is the same as the 32-bit device ID in other devices with different functionality. The TAP pins may also be configurable for purposes other than access to the TAP controller.*

Type	Circuit	Remarks
G		– CMOS level output – CMOS level hysteresis input – With pull-up resistor control – With standby mode control – Pull-up resistor: Approximately 50 kΩ – I_{OH}= -12 mA, I_{OL}= 12 mA – +B input is available
H		It is possible to select the USB I/O / GPIO function. When the USB I/O is selected – Full-speed, Low-speed control When the GPIO is selected. – CMOS level output – CMOS level hysteresis input – With standby mode control – I_{OH}= -20.5 mA, I_{OL}= 18.5 mA

12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1, *2	V_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Power supply voltage (for USB)*1, *3	$USBV_{CC}$	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog power supply voltage*1, *4	AV_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog reference voltage*1, *4	AVRH	V_{SS} - 0.5	V_{SS} + 6.5	V	
Input voltage*1	V_I	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	Except for USB pin
		V_{SS} - 0.5	$USBV_{CC}$ + 0.5 (≤ 6.5 V)	V	USB pin
		V_{SS} - 0.5	V_{SS} + 6.5	V	5 V tolerant
Analog pin input voltage*1	V_{IA}	V_{SS} - 0.5	AV_{CC} + 0.5 (≤ 6.5 V)	V	
Output voltage*1	V_O	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	
Clamp maximum current	I_{CLAMP}	-2	+2	mA	*8
Clamp total maximum current	$\Sigma[I_{CLAMP}]$		+20	mA	*8
L level maximum output current*5	I_{OL}	-	10	mA	4 mA type
			20	mA	12 mA type
			39	mA	P80, P81
L level average output current*6	I_{OLAV}	-	4	mA	4 mA type
			12	mA	12 mA type
			18.5	mA	P80, P81
L level total maximum output current	$\sum I_{OL}$	-	100	mA	
L level total average output current*7	$\sum I_{OLAV}$	-	50	mA	
H level maximum output current*5	I_{OH}	-	- 10	mA	4 mA type
			- 20	mA	12 mA type
			- 39	mA	P80, P81
H level average output current*6	I_{OHAV}	-	- 4	mA	4 mA type
			- 12	mA	12 mA type
			- 20.5	mA	P80, P81
H level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
H level total average output current*7	$\sum I_{OHAV}$	-	- 50	mA	
Power consumption	P_D	-	1000	mW	
Storage temperature	T_{STG}	- 55	+ 150	°C	

*1: These parameters are based on the condition that $V_{SS} = AV_{SS} = 0.0$ V.

*2: V_{CC} must not drop below V_{SS} - 0.5 V.

*3: $USBV_{CC}$ must not drop below V_{SS} - 0.5 V.

*4: Ensure that the voltage does not to exceed V_{CC} + 0.5 V, for example, when the power is turned on.

*5: The maximum output current is the peak value for a single pin.

*6: The average output is the average current for a single pin over a period of 100 ms.

*7: The total average output current is the average current for all pins over a period of 100 ms.

12.2 Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0V)

Parameter		Symbol	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply voltage		V_{CC}	-	2.7	5.5	V	
Power supply voltage for USB ch.0		$USBV_{CC}$	-	3.0	3.6 (≤ V_{CC})	V	*1
				2.7	5.5 (≤ V_{CC})		*2
Analog power supply voltage		AV_{CC}	-	2.7	5.5	V	AV_{CC} = V_{CC}
Analog reference voltage		AVRH	-	2.7	AV_{CC}	V	
Smoothing capacitor		C_S	-	1	10	µF	For built-in 1.2 V regulator*3
Operating temperature	LQI100-02 LQM120-02	T_A	When mounted on four-layer PCB	- 40	+ 85	°C	
	PQH100 LBC112	T_A	-	- 40	+ 85	°C	

*1: When P81/UDP0 and P80/UDM0 pin are used as USB (UDP0, UDM0).

*2: When P81/UDP0 and P80/UDM0 pin are used as GPIO (P81, P80).

*3: See "C Pin" in "7 Handling Devices" for the connection of the smoothing capacitor.

*4: In between less than the minimum power supply voltage and low voltage reset/interrupt detection voltage or more, instruction execution and low voltage detection function by built-in High-speed CR(including Main PLL is used) or built-in Low-speed CR is possible to operate only.

WARNING:

- *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.*
- *Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.*

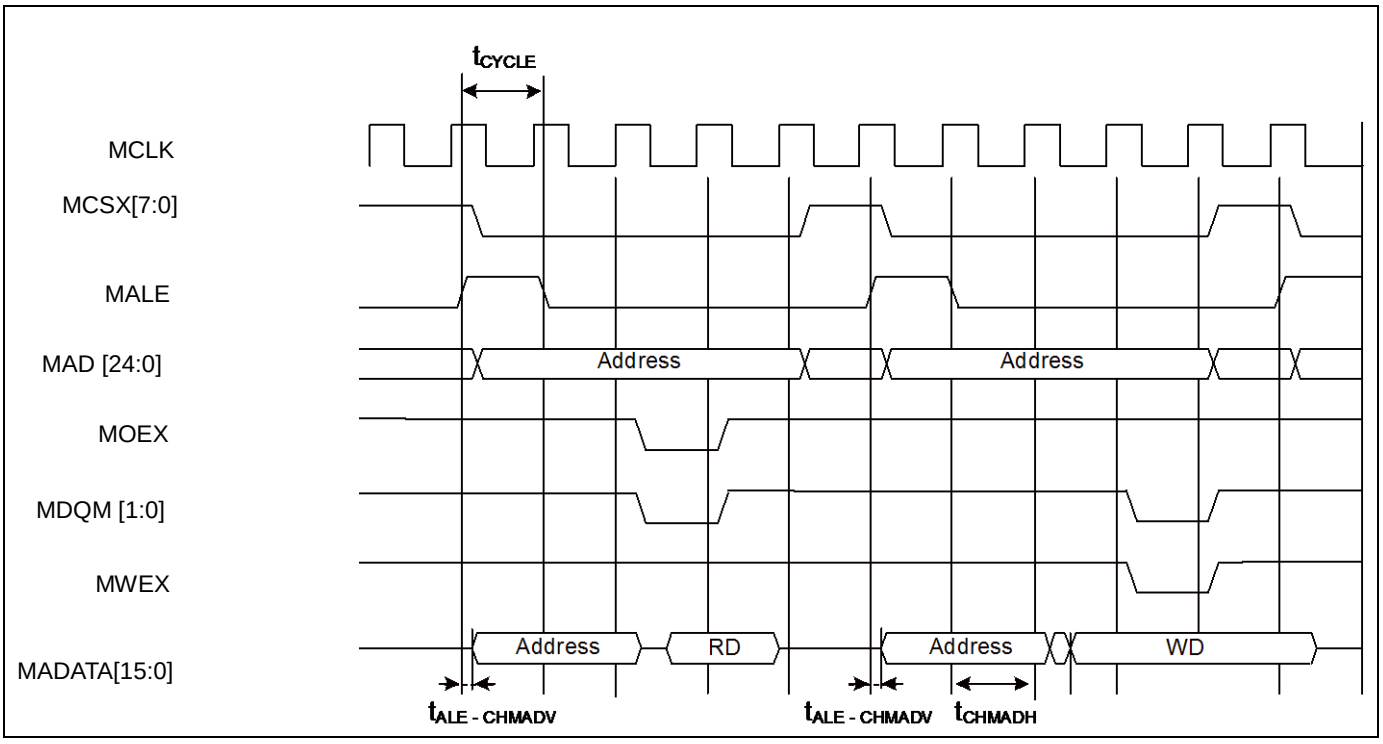
Multiplexed Bus Access Asynchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Multiplexed address delay time	$t_{ALE-CHMADV}$	MALE MADATA[15:0]	$V_{CC} \geq 4.5$ V	0	10	ns
			$V_{CC} < 4.5$ V		20	
Multiplexed address hold time	t_{CHMADH}		$V_{CC} \geq 4.5$ V	MCLK×n+0	MCLK×n+10	ns
			$V_{CC} < 4.5$ V	MCLK×n+0	MCLK×n+20	

Note:

- *When the external load capacitance = 30 pF. (m = 0 to 15, n = 1 to 16)*



NAND Flash Mode

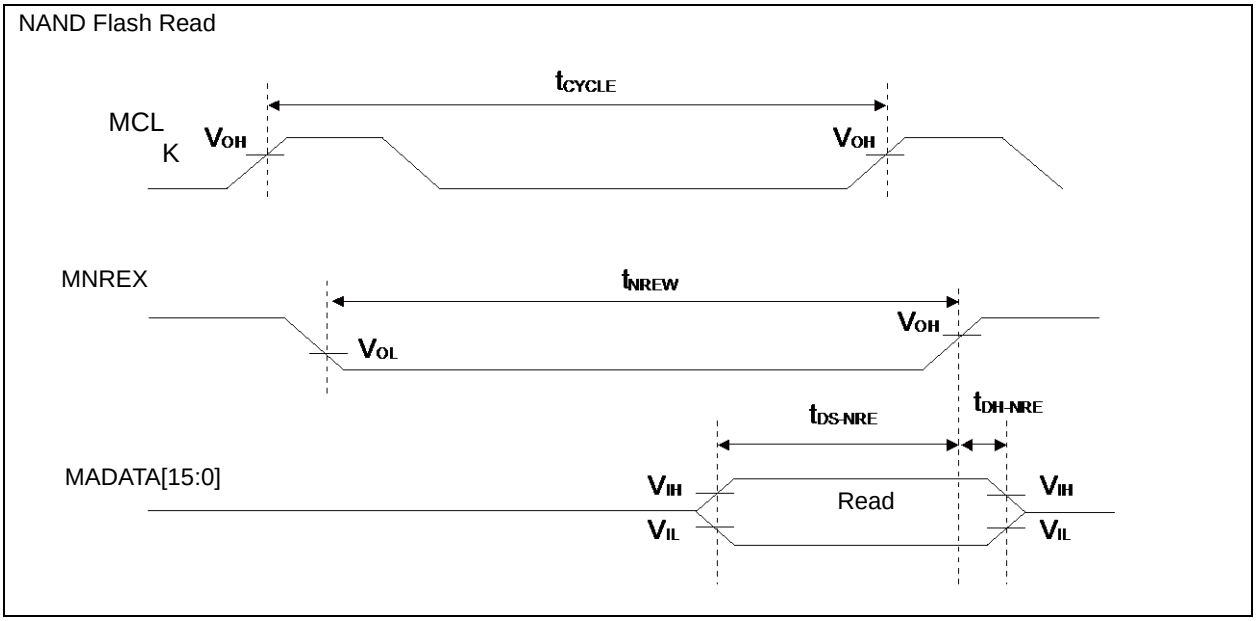
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V, T_A = -40°C to +85°C)

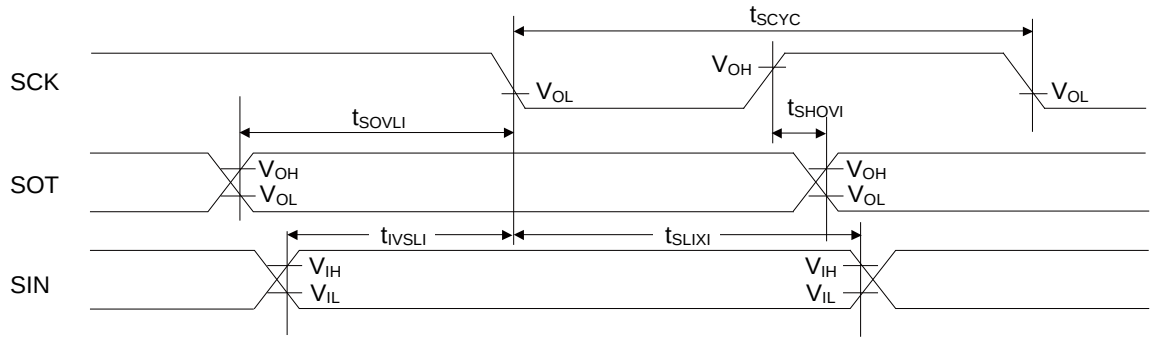
Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
MNREX Min pulse width	t_{NREW}	MNREX	$V_{CC} \geq 4.5$ V	MCLK×n-3	-	ns
			$V_{CC} < 4.5$ V			
Data setup → MNREX ↑ time	t_{DS-NRE}	MNREX MADATA[15:0]	$V_{CC} \geq 4.5$ V	20	-	ns
			$V_{CC} < 4.5$ V	38	-	
MNREX ↑ → Data hold time	t_{DH-NRE}	MNREX MADATA[15:0]	$V_{CC} \geq 4.5$ V	0	-	ns
			$V_{CC} < 4.5$ V			
MNALE ↑ → MNWEX delay time	$t_{ALEH-NWEL}$	MNALE MNWEX	$V_{CC} \geq 4.5$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 4.5$ V	MCLK×m-12	MCLK×m+12	
MNALE ↓ → MNWEX delay time	$t_{ALEL-NWEL}$	MNALE MNWEX	$V_{CC} \geq 4.5$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 4.5$ V	MCLK×m-12	MCLK×m+12	
MNCLE ↑ → MNWEX delay time	$t_{CLEH-NWEL}$	MNCLE MNWEX	$V_{CC} \geq 4.5$ V	MCLK×m-9	MCLK×m+9	ns
			$V_{CC} < 4.5$ V	MCLK×m-12	MCLK×m+12	
MNWEX ↑ → MNCLE delay time	$t_{NWEH-CLEL}$	MNCLE MNWEX	$V_{CC} \geq 4.5$ V	0	MCLK×m+9	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	
MNWEX Min pulse width	t_{NWEW}	MNWEX	$V_{CC} \geq 4.5$ V	MCLK×n-3	-	ns
			$V_{CC} < 4.5$ V			
MNWEX ↓ → Data delay time	$t_{NWEL-DV}$	MNWEX MADATA[15:0]	$V_{CC} \geq 4.5$ V	- 9	+ 9	ns
			$V_{CC} < 4.5$ V	-12	+12	
MNWEX ↑ → Data hold time	$t_{NWEH-DX}$	MNWEX MADATA[15:0]	$V_{CC} \geq 4.5$ V	0	MCLK×m+9	ns
			$V_{CC} < 4.5$ V		MCLK×m+12	

Note:

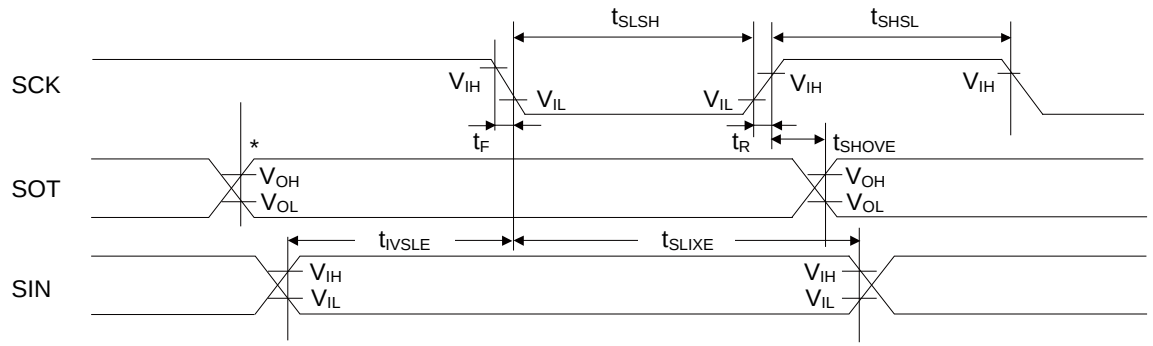
- *When the external load capacitance = 30 pF. (m=0 to 15, n=1 to 16)*

NAND Flash Read





Master mode



Slave mode

*: Changes when writing to TDR register

12.5 12-bit A/D Converter

Electrical Characteristics for the A/D Converter

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral Nonlinearity	-	-	-	± 4.0	± 4.5	LSB	AVRH = 2.7 V to 5.5 V
Differential Nonlinearity	-	-	-	± 2.3	± 2.5	LSB	
Zero transition voltage	V_{ZT}	ANxx	-	± 10	± 15	mV	
Full-scale transition voltage	V_{FST}	ANxx	-	AVRH ± 10	AVRH ± 15	mV	
Conversion time	-	-	1.0*1	-	-	µs	AV_{CC} ≥ 4.5 V
			1.2*1	-	-		AV_{CC} < 4.5 V
Sampling time	t_S	-	*2	-	-	ns	AV_{CC} ≥ 4.5 V
			*2	-	-		AV_{CC} < 4.5 V
Compare clock cycle*3	t_{CCK}	-	50	-	2000	ns	AV_{CC} ≥ 4.5 V
							AV_{CC} < 4.5 V
State transition time to operation permission	t_{STT}	-	-	-	1.0	µs	
Analog input capacity	C_{AIN}	-	-	-	12.9	pF	
Analog input resistance	R_{AIN}	-	-	-	2	kΩ	AV_{CC} ≥ 4.5 V
					3.8		AV_{CC} < 4.5 V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	ANxx	-	-	5	µA	
Analog input voltage	-	ANxx	AV_{SS}	-	AVRH	V	
Reference voltage	-	AVRH	2.7	-	AV_{CC}	V	

*1: Conversion time is the value of sampling time (t_S) + compare time (t_C).

The condition of the minimum conversion time is the following.

AV_{CC} ≥ 4.5 V, HCLK=120 Hz sampling time: 300 ns, compare time: 700 ns

AV_{CC} < 4.5 V, HCLK=120 Hz sampling time: 500 ns, compare time: 700 ns

Ensure that it satisfies the value of sampling time (t_S) and compare clock cycle (t_{CCK}).

For setting*4 of sampling time and compare clock cycle, see CHAPTER 1-1: 12-bit A/D Converter in FM3 Family PERIPHERAL MANUAL Analog Macro Part.

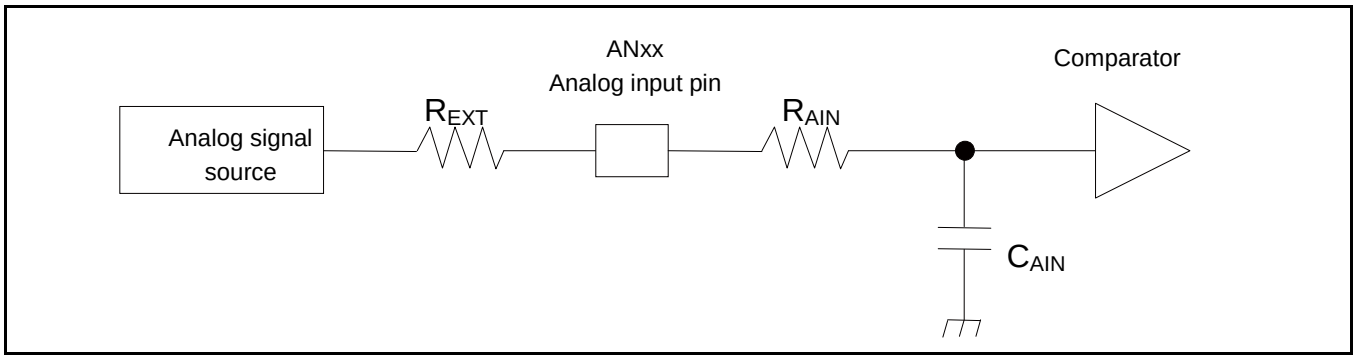
A/D Converter register is set at APB bus clock timing. Sampling and compare clock is set at Base clock (HCLK).

About the APB bus number which the A/D Converter is connected to, see 8 Block Diagram in this data sheet.

*2: A necessary sampling time changes by external impedance.

Ensure that it set the sampling time to satisfy (Equation 1).

*3: Compare time (t_C) is the value of (Equation 2).



(Equation 1) $t_S \geq (R_{AIN} + R_{EXT}) \times C_{AIN} \times 9$

t_S:	Sampling time
R_{AIN}:	input resistance of A/D = 2 kΩ at 4.5 V < AV_{CC} < 5.5 V
	input resistance of A/D = 3.8 kΩ at 2.7 V < AV_{CC} < 4.5 V
C_{AIN}:	input capacity of A/D = 12.9 pF at 2.7 V < AV_{CC} < 5.5 V
R_{EXT}:	Output impedance of external circuit

(Equation 2) $t_C = t_{CCK} \times 14$

t_C:	Compare time
t_{CCK}:	Compare clock cycle

12.10.2 Return Factor: Reset

The return time from Low-Power consumption mode is indicated as follows. It is from releasing reset to starting the program operation.

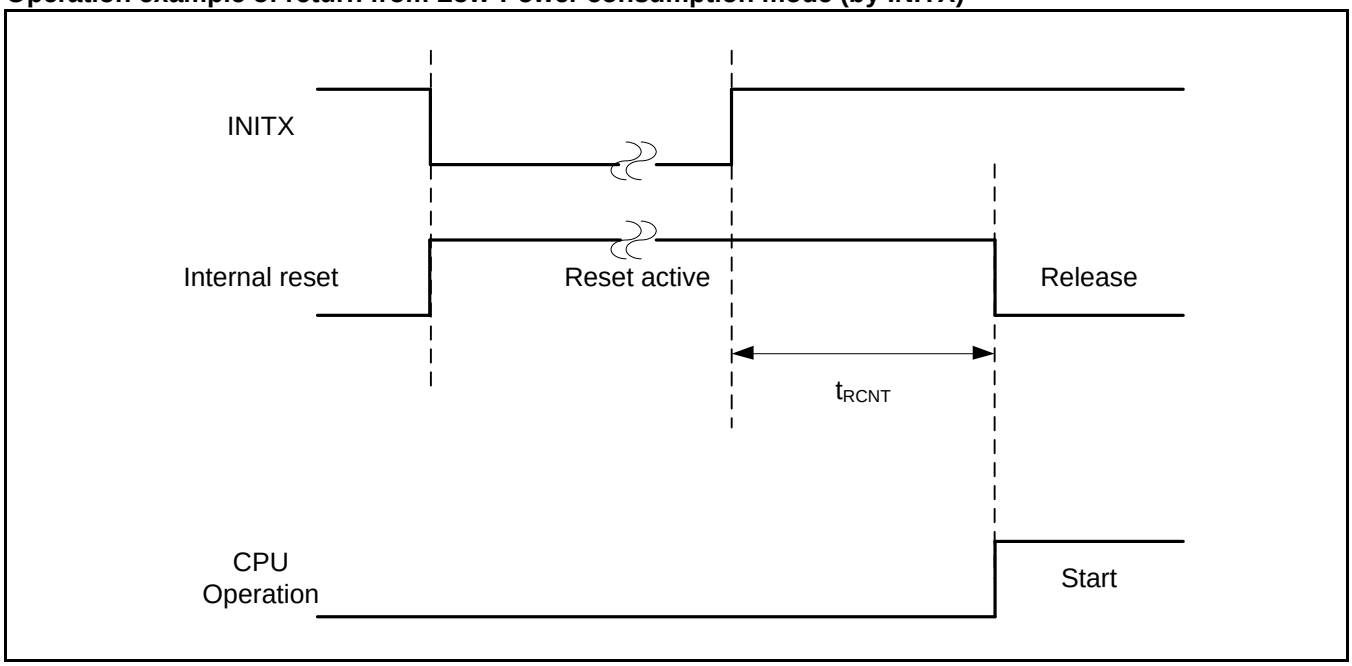
Return Count Time

(V_{CC} = 2.7V to 5.5V, T_A = - 40°C to + 85°C)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t_{RCNT}	321	461	µs	
High-speed CR Timer mode, Main Timer mode, PLL Timer mode		321	461	µs	
Low-speed CR Timer mode		441	701	µs	
Sub Timer mode		441	701	µs	
Stop mode		441	701	µs	

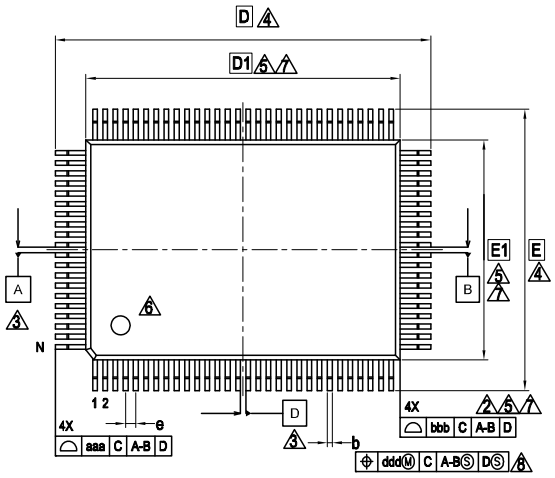
*: The maximum value depends on the accuracy of built-in CR.

Operation example of return from Low-Power consumption mode (by INITX)

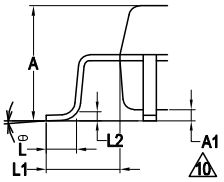


Package Type	Package Code
QFP 100	PQH100

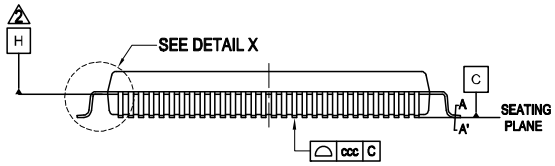
PQH100 , 100 Lead Plastic Quad Flat Package



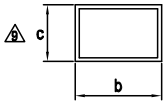
TOP VIEW



DETAIL X



SIDE VIEW



SECTION A-A'

PACKAGE	PQH100		
SYMBOL	MIN.	NOM.	MAX.
A	—	—	3.35
A1	0.05	—	0.45
b	0.27	0.32	0.37
c	0.11	—	0.23
D	23.90 BSC		
D1	20.00 BSC		
e	0.65 BSC		
E	17.90 BSC		
E1	14.00 BSC		
θ	0°		8°
L	0.73	0.88	1.03
L1	1.95 REF		
L2	0.25 BSC		

SYMBOL	TOLERANCES OF FORM AND POSITION
N	100
aaa	0.40
bbb	0.20
ccc	0.10
ddd	0.13

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev.0A

15. Major Changes

Spansion Publication Number: DS706-00027

Page	Section	Change Results
Revision 1.0		
-	-	Initial release
Revision 2.0		
6	■ FEATURES ● External Interrupt Controller Unit	Corrected the external interrupt input pin.
102	■ ELECTRICAL CHARACTERISTICS 5. 12-bit A/D Converter ● Electrical Characteristics for the A/D Converter	Corrected the value of "Compare clock cycle". Max: 10000 → 2000
111	■ ORDERING INFORMATION	Corrected the part number.
Revision 2.1		
-	-	Company name and layout design change
Revision 3.0		
2	■Features ●External Bus Interface	Added the description of Maximum area size
3	■Features ●USB Interface	Added the description of PLL for USB
10	■Packages	Deleted the description of ES
28, 29	■List of Pin Functions · List of pin numbers	Modified I/O circuit type of P63 to P68
48, 50	■I/O Circuit Type	Added the description of I2C to the type of E, F and I
48, 49	■I/O Circuit Type	Added about +B input
55	■Handling Devices	Added "□Stabilizing power supply voltage"
55	■Handling Devices ●Crystal oscillator circuit	Added the following description "Evaluate oscillation of your using crystal oscillator by your mount board."
56	■Handling Devices ●C Pin	Changed the description
57	■Block Diagram	Modified the block diagram
58	■Memory Map · Memory map(1)	Modified the area of "Extarnal Device Area"
59, 60	■Memory Map · Memory map(2)(3)	Added the summary of Flash memory sector and the note
67, 68	■Electrical Characteristics 1. Absolute Maximum Ratings	· Added the Clamp maximum current · Added the output current of P80 and P81 · Added about +B input
69	■Electrical Characteristics 2. Recommended Operation Conditions	· Modified the minimum value of Analog reference voltage · Added Smoothing capacitor · Added the note about less than the minimum power supply voltage
70, 71	■Electrical Characteristics 3. DC Characteristics (1) Current rating	· Changed the table format · Added Main TIMER mode current · Added Flash Memory Current · Moved A/D Converter Current · Modified the unit of low voltage detection circuit (LVD) power supply current
74	■Electrical Characteristics 4. AC Characteristics (1) Main Clock Input Characteristics	Added Master clock at Ingernal operating clock frequency
75	■Electrical Characteristics 4. AC Characteristics (3) Built-in CR Oscillation Characteristics	Added Frequency stability time at Built-in high-speed CR

Page	Section	Change Results
76	■Electrical Characteristics 4. AC Characteristics (4-1) Operating Conditions of Main and USB PLL (4-2) Operating Conditions of Main PLL	· Added Main PLL clock frequency · Added USB clock frequency · Added the figure of Main PLL connection and USB PLL connection
77	■Electrical Characteristics 4. AC Characteristics (6) Power-on Reset Timing	· Added Time until releasing Power-on reset · Changed the figure of timing
79-81	■Electrical Characteristics 4. AC Characteristics (7) External Bus Timing	Modified Data output time
89-96	■Electrical Characteristics 4. AC Characteristics (8) CSIO/UART Timing	· Modified from UART Timing to CSIO/UART Timing · Changed from Internal shift clock operation to Master mode · Changed from External shift clock operation to Slave mode
103	■Electrical Characteristics 5. 12bit A/D Converter	· Added the typical value of Integral Nonlinearity, Differential Nonlinearity, Zero transition voltage and Full-scale transition voltage · Modified Stage transition time to operation permission · Modified the minimum value of Reference voltage
110	■Electrical Characteristics 7. Low-voltage Detection Characteristics (2) Interrupt of Low-voltage Detection	Modified LVD stabilization wait time
111	■Electrical Characteristics 9. WorkFlash Memory Write/Erase Characteristics (1) Write / Erase time	· Modified sector erase time · Modified half word(16-bit) write time
112-115	■Electrical Characteristics 9. Return Time from Low-Power Consumption Mode	Added Return Time from Low-Power Consumption Mode
116	■Ordering Information	Change to full part number
117-120	■Package Dimensions	Deleted FPT-100P-M20 and FPT-120P-M21

NOTE: Please see “Document History” about later revised information.