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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HCS08
Core Size	8-Bit
Speed	48MHz
Connectivity	FIFO, I²C, SCI, SPI, USB
Peripherals	LVD, POR, PWM, WDT
Number of I/O	46
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x12b SAR
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc9s08je128clk

Contents

Related Documentation

Find the most current versions of all documents at: http://www.freescale.com.

Reference Manual —MC9S08JE128RM

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

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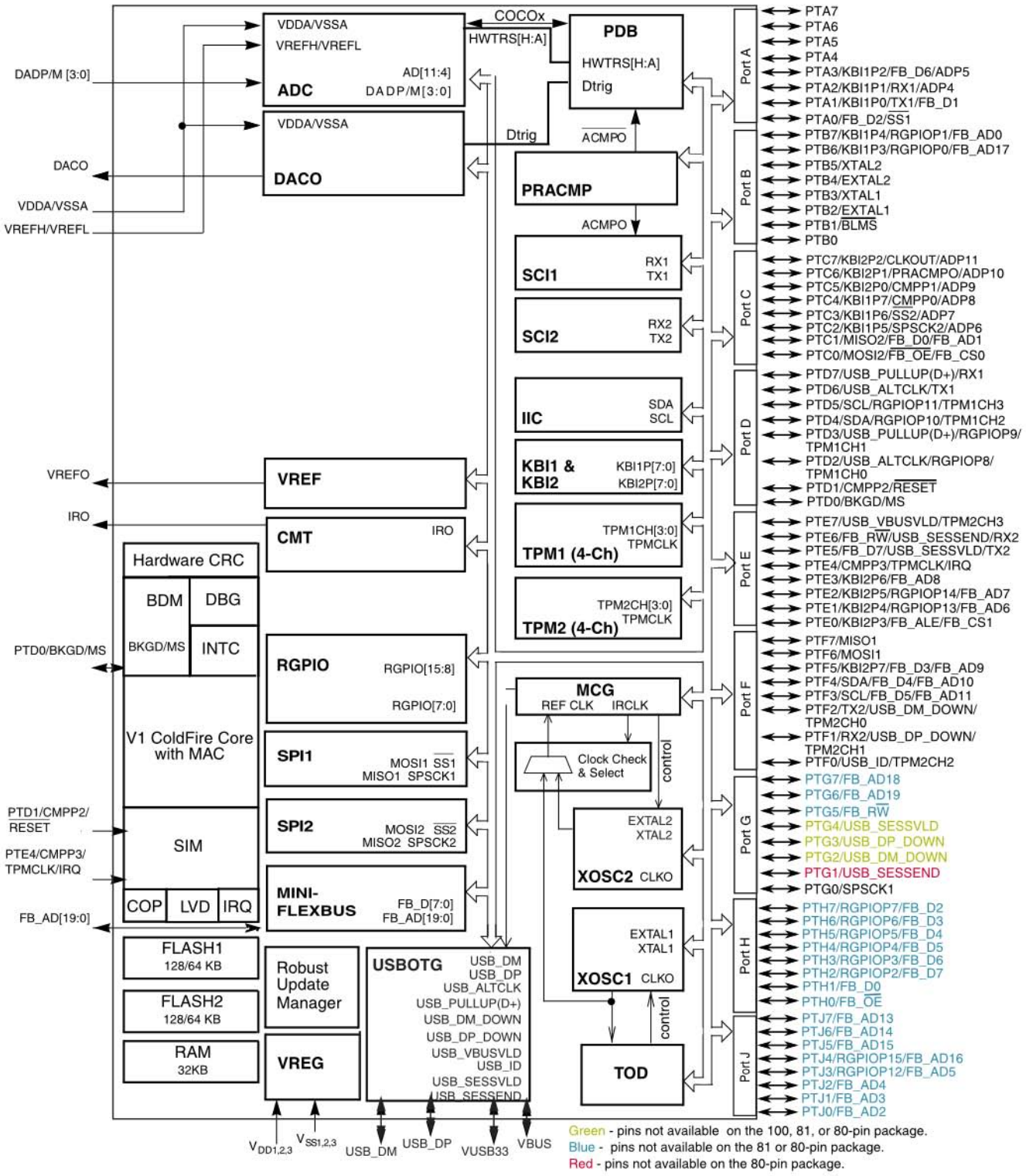

Figure 1. MC9S08JE128 series Block Diagram

1.1 Pin Assignments

This section shows the pin assignments for the MC9S08JE128 series devices.

1.1.1 64-Pin LQFP

The following two figures show the 64-pin LQFP pinout configuration.

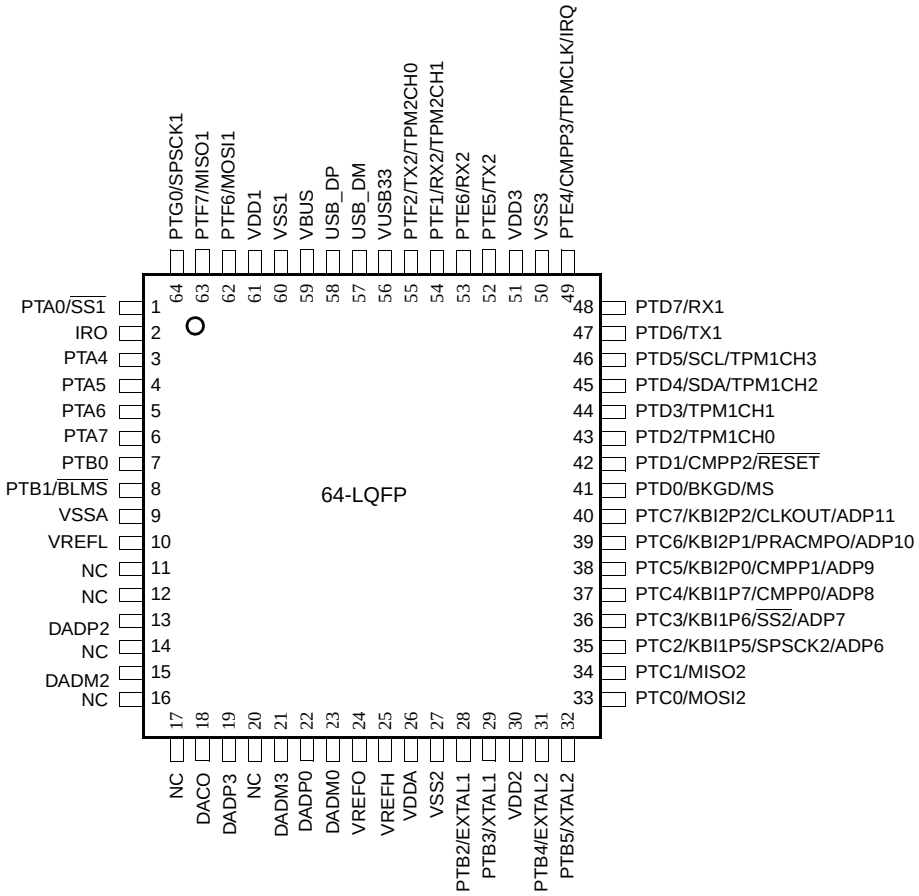

Figure 2. 64-Pin LQFP

1.2 Pin Assignments by Packages

Table 3. Package Pin Assignments

Package			Default Function	ALT1	ALT2	ALT3	Composite Pin Name
81 MAPBGA	80 LQFP	64 LQFP					
B2	1	1	PTA0	$\overline{SS1}$	—	—	PTA0/$\overline{SS1}$
A1	2	2	IRO	—	—	—	IRO
C4	3	—	PTA1	KBI1P0	TX1	—	PTA1/KBI1P0/TX1
D5	4	—	PTA2	KBI1P1	RX1	ADP4	PTA2/KBI1P1/RX1/ADP4
D6	5	—	PTA3	KBI1P2	ADP5	—	PTA3/KBI1P2/ADP5
C1	6	3	PTA4	—	—	—	PTA4
C2	7	4	PTA5	—	—	—	PTA5
C3	8	5	PTA6	—	—	—	PTA6
D2	9	6	PTA7	—	—	—	PTA7
D3	10	7	PTB0	—	—	—	PTB0
D4	11	8	PTB1	$\overline{BLMS}$	—	—	PTB1/$\overline{BLMS}$
J1	12	9	VSSA	—	—	—	VSSA
J2	13	10	VREFL	—	—	—	VREFL
D1	14	11	NC	—	—	—	NC
E1	15	12	NC	—	—	—	NC
F2	16	13	DADP2	—	—	—	DADP2
F1	17	14	NC	—	—	—	NC
E2	18	15	DADM2	—	—	—	DADM2
F3	19	16	NC	—	—	—	NC
E3	20	17	NC	—	—	—	NC
G2	21	18	DACO	—	—	—	DACO
G3	22	19	DADP3	—	—	—	DADP3
H4	23	20	NC	—	—	—	NC
G4	24	21	DADM3	—	—	—	DADM3
G1	25	22	DADP0	—	—	—	DADP0
H1	26	23	DADM0	—	—	—	DADM0
G5	27	24	VREFO	—	—	—	VREFO
H3	28	—	DADP1	—	—	—	DADP1
H2	29	—	DADM1	—	—	—	DADM1

2.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 6. Thermal Characteristics

#	Symbol	Rating	Value	Unit
1	T_A	Operating temperature range (packaged):		°C
		MC9S08JE128	–40 to 105	
		MC9S08JE64	–40 to 105	
2	T_{JMAX}	Maximum junction temperature	135	°C
3	θ_{JA}	Thermal resistance[1,2,3,4] Single-layer board — 1s		°C/W
		81-pin MBGA	77	
		80-pin LQFP	55	
		64-pin LQFP	68	
4	θ_{JA}	Thermal resistance[1, 2, 3, 4] Four-layer board — 2s2p		°C/W
		81-pin MBGA	47	
		80-pin LQFP	40	
		64-pin LQFP	49	

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Junction to Ambient Natural Convection

3 1s — Single layer board, one signal layer

4 2s2p — Four layer board, 2 signal and 2 power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power

$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \qquad \textit{Eqn. 2}$$

Table 9. DC Characteristics (Continued)

Num	Symbol	Characteristic	Condition	Min	Typ[1]	Max	Unit	C
7	V_{IL}	Input low voltage all digital inputs						
			all digital inputs, $V_{DD} > 2.7$ V	—	—	0.35 x V_{DD}	V	P
			all digital inputs, $2.7 > V_{DD} \geq 1.8$ V	—	—	0.30 x V_{DD}	V	P
8	V_{hys}	Input hysteresis all digital inputs	—	0.06 x V_{DD}	—	—	mV	C
9	$\|I_{In}\|$	Input leakage current all input only pins (Per pin)	$V_{In} = V_{DD}$ or V_{SS}	—	—	0.25 (TBD)	µA	P
10	$\|I_{OZ}\|$	Hi-Z (off-state) leakage current all input/output (per pin)	$V_{In} = V_{DD}$ or V_{SS}	—	—	1(TBD)	µA	P
11	$\|I_{OZ}\|$	Leakage current for analog output pins (DACO, VREFO) all input/output (per pin)	$V_{In} = V_{DD}$ or V_{SS}	—	—	(TBD)	µA	P
12	$\|I_{InT}\|$	Total Leakage Current[3] For all pins		—	—	2	µA	D
13	R_{PU}	Pull-up resistors	—	17.5	—	52.5	kΩ	P
14	R_{PD}	Internal pull-down resistors[4]	—	17.5	—	52.5	kΩ	P
15	I_{IC}	DC injection current [5, 6, 7] Single pin limit						
			$V_{SS} > V_{IN} > V_{DD}$	–0.2	—	0.2	mA	D
		Total MCU limit, includes sum of all stressed pins						
			$V_{SS} > V_{IN} > V_{DD}$	–5	—	5	mA	D
16	C_{In}	Input Capacitance, all pins	—	—	—	8	pF	C
17	V_{RAM}	RAM retention voltage	—	—	0.6	1.0	V	C
18	V_{POR}	POR re-arm voltage[8]	—	0.9	1.4	1.79	V	C
19	t_{POR}	POR re-arm time	—	10	—	—	µs	D

Table 9. DC Characteristics (Continued)

Num	Symbol	Characteristic	Condition	Min	Typ[1]	Max	Unit	C
20	V_{LVDH}[9]	Low-voltage detection threshold — high range	V_{DD} falling					
			—	2.11	2.16	2.22	V	P
			V_{DD} rising					
			—	2.16	2.23	2.27	V	P
21	V_{LVDL}	Low-voltage detection threshold — low range[9]	V_{DD} falling					
			—	1.80	1.84	1.88	V	P
			V_{DD} rising					
			—	1.88	1.93	1.96	V	P
22	V_{LVWH}	Low-voltage warning threshold — high range[9]	V_{DD} falling					
			—	2.36	2.46	2.56	V	P
			V_{DD} rising					
			—	2.36	2.46	2.56	V	P
23	V_{LVWL}	Low-voltage warning threshold — low range[9]	V_{DD} falling					
			—	2.11	2.16	2.22	V	P
			V_{DD} rising					
			—	2.16	2.23	2.27	V	P
24	V_{hys}	Low-voltage inhibit reset/recover hysteresis[10]	—	—	50	—	mV	C
25	V_{BG}	Bandgap Voltage Reference[11]	—	1.15	1.17	1.18	V	P

1 Typical values are measured at 25°C. Characterized, not tested

2 As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above V_{LVDL}.

3 Total Leakage current is the sum value for all GPIO pins; this leakage current is not distributed evenly across all pins but characterization data shows that individual pin leakage current maximums are less than 250 nA.

4 Measured with $V_{In} = V_{DD}$.

5 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

6 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

[7] Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

[8] Maximum is highest voltage that POR is guaranteed.

[9] Run at 1 MHz bus frequency

[10] Low voltage detection and warning limits measured at 1 MHz bus frequency.

[11] Factory trimmed at V_{DD} = 3.0 V, Temp = 25°C

2.6 Supply Current Characteristics

Table 10. Supply Current Characteristics

#	Symbol	Parameter	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)	C
1	RI_{DD}	Run supply current FEI mode All modules ON							
			24 MHz	3	20	24	mA	–40 to 25	P
			24 MHz	3	20	TBD	mA	105	P
			20 MHz	3	18	—	mA	–40 to 105	T
			8 MHz	3	8	—	mA	–40 to 105	T
			1 MHz	3	1.8	—	mA	–40 to 105	T
2	RI_{DD}	Run supply current FEI mode; All modules OFF							
			24 MHz	3	12.3	TBD	mA	–40 to 105	C
			20 MHz	3	10.5	—	mA	–40 to 105	T
			8 MHz	3	4.8	—	mA	–40 to 105	T
			1 MHz	3	1.3	—	mA	–40 to 105	T
3	RI_{DD}	Run supply current LPS=0; All modules OFF							
			16 kHz FBILP	3	TBD	—	µA	–40 to 105	T
			16 kHz FBELP	3	TBD	—	µA	–40 to 105	T
4	RI_{DD}	Run supply current LPS=1, all modules OFF							
			16 kHz FBELP	3	TBD	—	µA	0 to 70	T
			16 kHz FBELP	3	TBD	—	µA	–40 to 105	T

Table 11. Typical Stop Mode Adders

#	Parameter	Condition	Temperature (°C)					Units	C
			-40	25	70	85	105		
1	LPO	—	50	75	100	150	250	nA	D
2	EREFSTEN	RANGE = HGO = 0	600 (TBD)	650 (TBD)	750 (TBD)	850 (TBD)	1000 (TBD)	nA	D
3	IREFSTEN[1]	—	68	70	77	86	120	µA	T
4	TOD	Does not include clock source current	50	75	100	150	250	nA	D
5	LVD[1]	LVDSE = 1	114	115	123	135	170	µA	T
6	ACMP[1]	Not using the bandgap (BGBE = 0)	18	20	23	33	65	µA	T
7	ADC[1]	ADLPC = ADLSMP = 1 Not using the bandgap (BGBE = 0)	75	85	100	115	165	µA	T
8	DAC[1]	High power mode; no load on DACO	500	500	500	500	500	µA	T

1 Not available in stop2 mode.

2.7 PRACMP Electricals

Table 12. PRACMP Electrical Specifications

#	Characteristic	Symbol	Min	Typical	Max	Unit	C
1	Supply voltage	V_{PWR}	1.8	—	3.6	V	P
2	Supply current (active) (PRG enabled)	I_{DDACT1}	—	—	60	µA	C
3	Supply current (active) (PRG disabled)	I_{DDACT2}	—	—	40	µA	C
4	Supply current (ACMP and PRG all disabled)	I_{DDDIS}	—	—	2	nA	D
5	Analog input voltage	VAIN	V_{SS} – 0.3	—	V_{DD}	V	—
6	Analog input offset voltage	VAIO	—	5	40	mV	T
7	Analog comparator hysteresis	V_H	3.0	—	20.0	mV	T
8	Analog input leakage current	I_{ALKG}	—	—	1	nA	D
9	Analog comparator initialization delay	tAINIT	—	—	1.0	µs	T

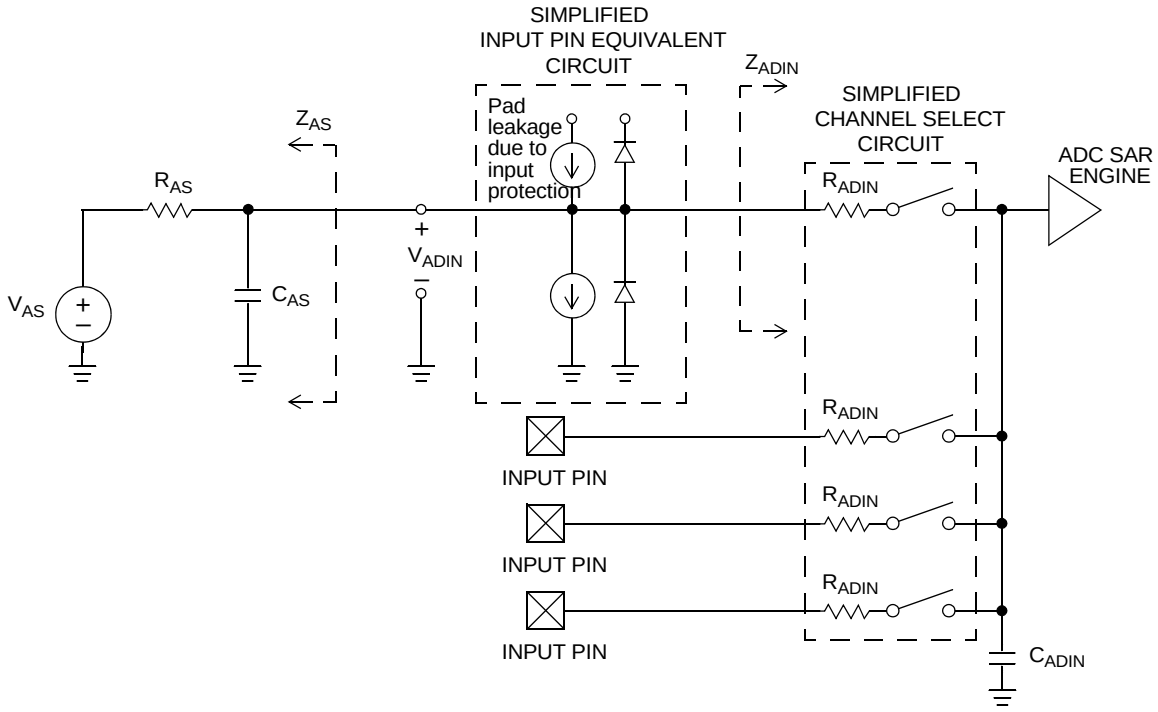

Figure 6. ADC Input Impedance Equivalency Diagram

Table 16. 12-bit SAR ADC Characteristics full operating range (V_{REFH} = V_{DDAD}, > 1.8, V_{REFL} = V_{SSAD} ≤ 8 MHz) (Continued)

Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	C	Comment
Zero-Scale Error	12-bit single-ended mode	E_{ZS}	—	±0.7	±2.0	LSB[2]	T	V_{ADIN} = V_{SSAD}
	11-bit differential mode 10-bit single-ended mode		— —	±0.4 ±0.4	±1.0 ±1.0		T	
	9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	
Full-Scale Error	12-bit single-ended mode	E_{FS}	—	±1.0	±3.5	LSB[2]	T	V_{ADIN} = V_{DDAD}
	11-bit differential mode 10-bit single-ended mode		— —	±0.4 ±0.4	±1.5 ±1.5		T	
	9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	
Quantization Error	All modes	E_Q	—	—	±0.5	LSB[2]	D	
Input Leakage Error	all modes	E_{IL}	I_{In} * R_{AS}			mV	D	I_{In} = leakage current (refer to DC characteristics)
Temp Sensor Slope	–40°C – 25°C	m	—	1.646	—	mV/×C	C	
	25°C – 125°C		—	1.769	—			
Temp Sensor Voltage	25°C	V_{TEMP25}	—	701.2	—	mV	C	

1 All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDAD}

2 Typical values assume V_{DDAD} = 3.0V, Temp = 25°C, f_{ADCK}=2.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3 1 LSB = (V_{REFH} - V_{REFL})/2^N

3 This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

4 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

5 625 ns represents 5 time quanta for CAN applications, under worst-case conditions of 8 MHz CAN bus clock, 1 Mbps CAN Bus speed, and 8 time quanta per bit for bit time settings. 5 time quanta is the minimum time between a synchronization edge and the sample point of a bit using 8 time quanta per bit.

6 Below D_{lock} minimum, the MCG is guaranteed to enter lock. Above D_{lock} maximum, the MCG will not enter lock. But if the MCG is already in lock, then the MCG may stay in lock.

7 Below D_{unl} minimum, the MCG will not exit lock if already in lock. Above D_{unl} maximum, the MCG is guaranteed to exit lock.

Table 18. XOSC (Temperature Range = –40 to 105°C Ambient)

#	Characteristic		Symbol	Min	Typ[1]	Max	Unit
1	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1)	• Low range (RANGE = 0)	f_{lo}	32	—	38.4	kHz
		• High range (RANGE = 1), • FEE or FBE mode [2]	fhi	1	—	5	MHz
		• High range (RANGE = 1), • High gain (HGO = 1), • FBELP mode	fhi	1	—	16	MHz
		• High range (RANGE = 1), • Low power (HGO = 0), • FBELP mode	fhi	1	—	8	MHz
2	Load capacitors		C_1 C_2	See Note [3]			
3	Feedback resistor	Low range (32 kHz to 38.4 kHz)	R_F	—	10	—	MΩ
		High range (1 MHz to 16 MHz)	—	—	1	—	
4	Series resistor — Low range	Low Gain (HGO = 0)	R_S	—	0	—	kΩ
		High Gain (HGO = 1)		—	100	—	
5	Series resistor — High range	• Low Gain (HGO = 0) • High Gain (HGO = 1)					kΩ
		≥ 8 MHz	R_S	—	0	0	
		4 MHz		—	0	10	
		1 MHz		—	0	20	

Table 18. XOSC (Temperature Range = –40 to 105°C Ambient)

#	Characteristic		Symbol	Min	Typ[1]	Max	Unit
6	Crystal start-up time [4, 5]	Low range, low gain (RANGE = 0, HGO = 0)	t_{CSTL}	—	200	—	ms
		Low range, high gain (RANGE = 0, HGO = 1)		—	400	—	
		High range, low gain (RANGE = 1, HGO = 0)	t_{CSTH}	—	5	—	
		High range, high gain (RANGE = 1, HGO = 1)		—	15	—	

1 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

2 When MCG is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

3 See crystal or resonator manufacturer's recommendation.

4 This parameter is characterized and not tested on each device.

5 Proper PC board layout procedures must be followed to achieve specifications.

Table 19. Control Timing

#	Symbol	Parameter	Min	Typical[1]	Max	C	Unit
9	t_{Rise}, t_{Fall}	Port rise and fall time (load = 50 pF)[4], Low Drive					ns
		Slew rate control disabled (PTxSE = 0)	—	11	—	D	
		Slew rate control enabled (PTxSE = 1)	—	35	—	D	
		Slew rate control disabled (PTxSE = 0)	—	40	—	D	
		Slew rate control enabled (PTxSE = 1)	—	75	—	D	

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

3 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

4 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 105 °C.

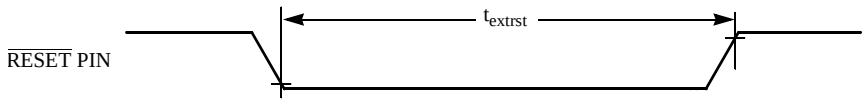

Figure 7. Reset Timing

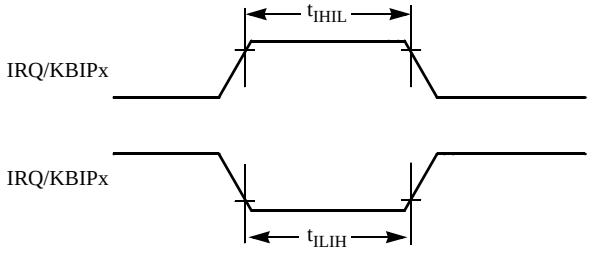

Figure 8. IRQ/KBIPx Timing

2.11.2 TPM Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 20. TPM Input Timing

#	C	Function	Symbol	Min	Max	Unit
1	—	External clock frequency	f_{TPMext}	dc	$f_{Bus}/4$	MHz
2	—	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

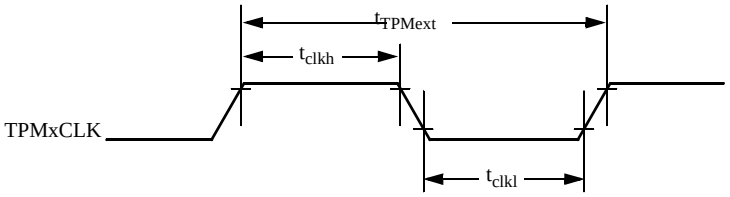

Figure 9. Timer External Clock

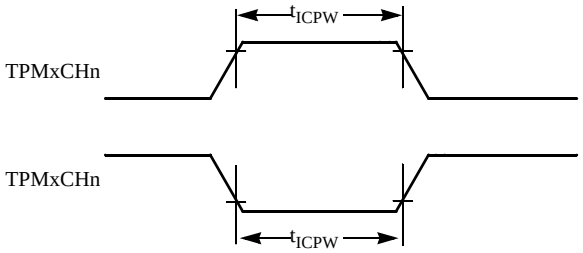

Figure 10. Timer Input Capture Pulse

2.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory chapter in the Reference Manual for this device (MC9S08JE128RM).

Table 22. Flash Characteristics

#	Characteristic	Symbol	Min	Typical	Max	Unit	C
1	Supply voltage for program/erase -40°C to 105°C	$V_{prog/erase}$	1.8	—	3.6	V	D
2	Supply voltage for read operation	V_{Read}	1.8	—	3.6	V	D
3	Internal FCLK frequency[1]	f_{FCLK}	150	—	200	kHz	D
4	Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	µs	D
5	Byte program time (random location)[2]	t_{prog}	9			t_{Fcyc}	P
6	Byte program time (burst mode)[2]	t_{Burst}	4			t_{Fcyc}	P
7	Page erase time[2]	t_{Page}	4000			t_{Fcyc}	P
8	Mass erase time[2]	t_{Mass}	20,000			t_{Fcyc}	P
9	Program/erase endurance[3] T_L to T_H = –40°C to + 105°C T = 25°C		10,000 —	— 100,000	— —	cycles	C
10	Data retention[4]	t_{D_ret}	15	100	—	years	C

1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 **Typical endurance for flash** was evaluated for this product family on the HC9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory*.

4 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.*

2.14 USB Electricals

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit http://www.usb.org.

If the Freescale USB On-the-Go implementation has electrical characteristics that deviate from the standard or require additional information, this space would be used to communicate that information.

Table 23. Internal USB 3.3 V Voltage Regulator Characteristics

#	Characteristic	Symbol	Min	Typ	Max	Unit	C
1	Regulator operating voltage	V_{regin}	3.9	—	5.5	V	C
2	VREG output	V_{regout}	3	3.3	3.6	V	P
3	V_{USB33} input with internal VREG disabled	$V_{usb33in}$	3	3.3	3.6	V	C
4	VREG Quiescent Current	I_{VRQ}	—	0.5	—	mA	C

2.15 VREF Electrical Specifications

Table 24. VREF Electrical Specifications

Num	Characteristic	Symbol	Min	Max	Unit	C
1	Supply voltage	V_{DDA}	1.80	3.6	V	C
2	Temperature	T_A	–40	105	°C	C
3	Output Load Capacitance	C_L	—	100	nf	D
4	Maximum Load	—	—	10	mA	—
5	Voltage Reference Output with Factory Trim. V_{DD} = 3 V.	Vout	1.140	1.160	V	P
6	Temperature Drift (Vmin - Vmax across the full temperature range)	Tdrift	—	10 (TBD)	mV[1]	T
7	Aging Coefficient	Ac	—	TBD	ppm/year	C
8	Powered down Current (Off Mode, VREFEN=0, VRSTEN=0)	I	—	0.10	µA	C
9	Bandgap only (MODE_LV[1:0] = 00)	I	—	75	µA	T
10	Low-Power buffer (MODE_LV[1:0] = 01)	I	—	125	µA	T
11	Tight-Regulation buffer (MODE_LV[1:0] = 10)	I	—	1.1	mA	T
12	Load Regulation MODE_LV = 10	—	—	100	µV/mA	C
13	Line Regulation (Power Supply Rejection)	DC	—	TBD	mV	C
14		AC	TBD	—	dB	

[1] See typical chart below.

Table 25. VREF Limited Range Operating Requirements

#	Characteristic	Symbol	Min	Max	Unit	C	Notes
1	Temperature	T_A	0	50	°C	C	

Table 26. VREF Limited Range Operating Behaviors

#	Characteristic	Symbol	Min	Max	Unit	C	Notes
1	Voltage Reference Output with Factory Trim	Vout	TBD	TBD	µA	C	

3.1 Device Numbering System

Example of the device numbering system:

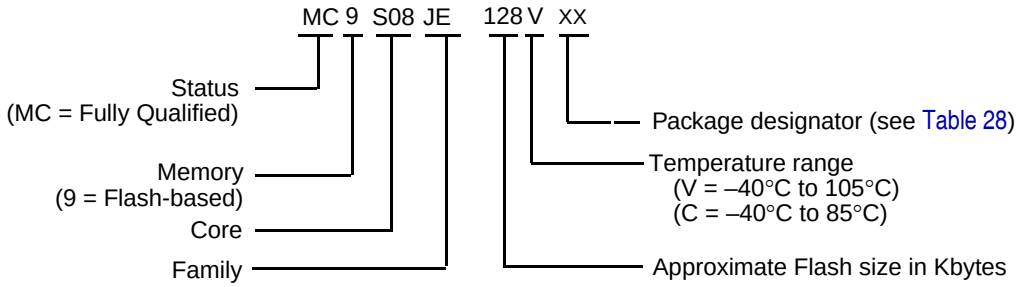

Table 27. Device Numbering System

Device Number[1]	Memory		Available Packages[2]
	Flash	RAM	
MC9S08JE128	131,072	12,288	64 LQFP
	131,072	12,288	80 LQFP
	131,072	12,288	81 MAPBGA
MC9S08JE64	65,536	12,288	64 LQFP

1 See Table 2 for a complete description of modules included on each device.

2 See Table 28 for package information.

3.2 Package Information

Table 28. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
64	Low Quad Flat Package	LQFP	LH	840F-02	98ASS23234W
80	Low Quad Flat Package	LQFP	LK	917-01	98ASS23174W
81	MAPBGA Package	Map PBGA	MB	1662-01	98ASA10670D

3.3 Mechanical Drawings

Table 28 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MC9S08JE128 series Product Summary pages at http://www.freescale.com.

To view the latest drawing, either:

- Click on the appropriate link in Table 28, or
- Open a browser to the Freescale® website (http://www.freescale.com), and enter the appropriate document number (from Table 28) in the “Enter Keyword” search box at the top of the page.