Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, SCI, SPI, USB
Peripherals	LVD, POR, PWM, WDT
Number of I/O	47
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	81-LBGA
Supplier Device Package	81-MAPBGA (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s08je128cmb

Contents

Related Documentation

Find the most current versions of all documents at: http://www.freescale.com.

Reference Manual —MC9S08JE128RM

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

–

A complete description of the modules included on each device is provided in the following table.

Table 2. Versions of On-Chip Modules

Module	Version
Analog-to-Digital Converter (ADC12)	1
Digital to Analog Converter (DAC)	1
Programmable Delay Block	1
Inter-Integrated Circuit (IIC)	3
Central Processing Unit (CPU)	5
On-Chip In-Circuit Debug/Emulator (DBG)	3
Multi-Purpose Clock Generator (MCG)	3
Low Power Oscillator (XOSCVLP)	1
Carrier Modulator Timer (CMT)	1
Programable Analog Comparator (PRACMP)	1
Serial Communications Interface (SCI)	4
Serial Peripheral Interface (SPI)	5
Time of Day (TOD)	1
Universal Serial Bus (USB)	1
Timer Pulse-Width Modulator (TPM)	3
System Integration Module (SIM)	1
Cyclic Redundancy Check (CRC)	3
Keyboard Interrupt (KBI)	2
Voltage Reference (VREF)	1
Voltage Regulator (VREG)	1
Interrupt Request (IRQ)	3
Flash Wrapper	1
GPIO	2
Port Control	1

The block diagram in Figure 1 shows the structure of the MC9S08JE128 series MCU.

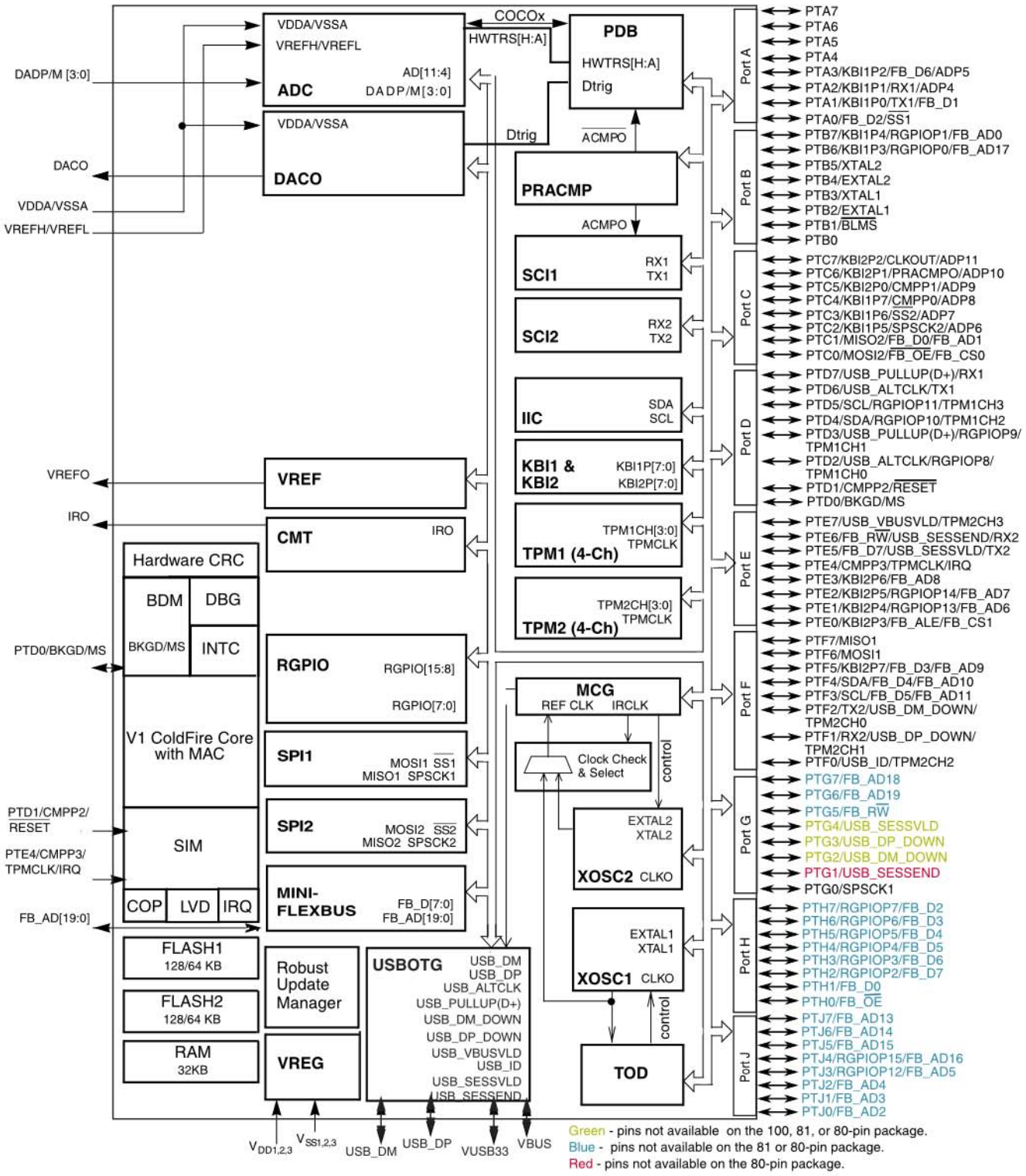


Figure 1. MC9S08JE128 series Block Diagram

1.1.2 80-Pin LQFP

The following figure shows the 80-pin LQFP pinout configuration.

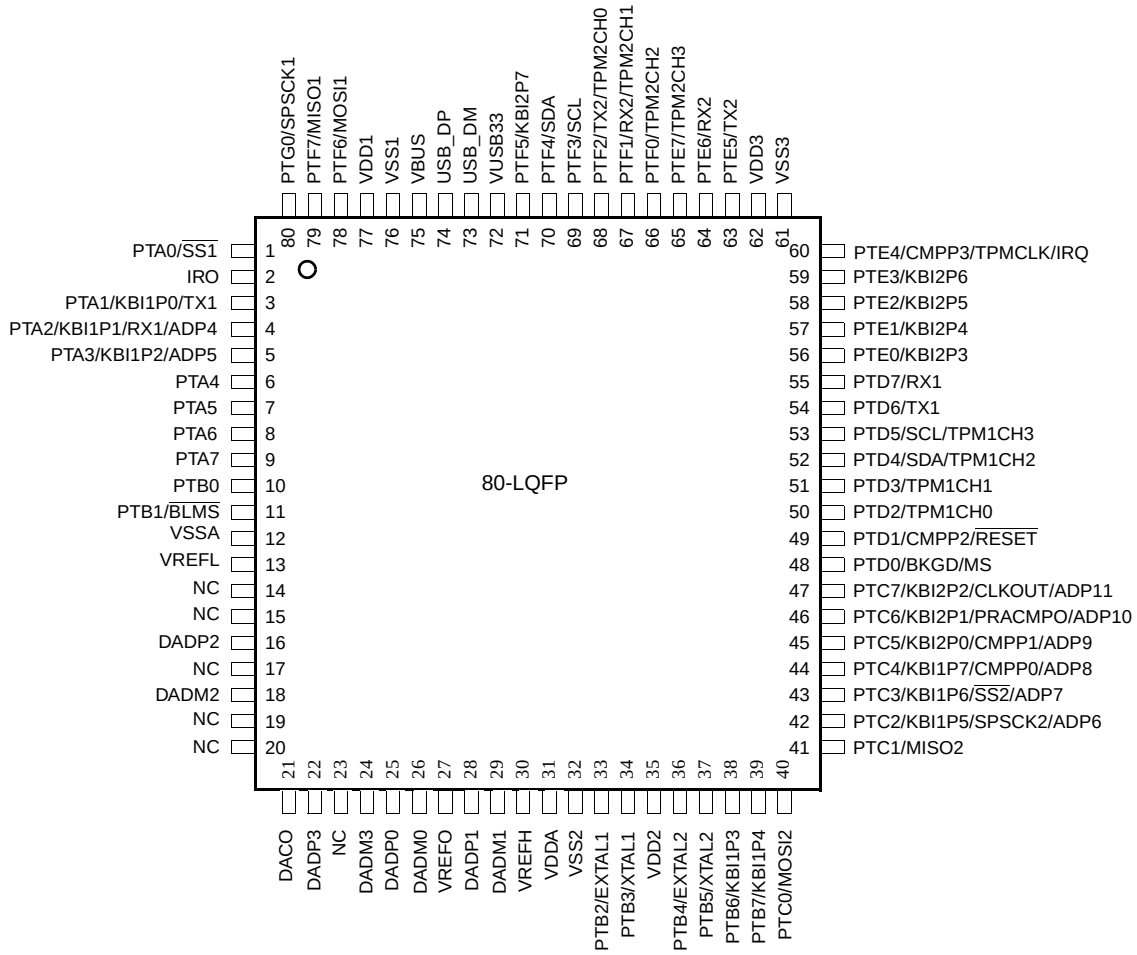


Figure 3. 80-Pin LQFP

1.1.3 81-Pin MAPBGA

The following figure shows the 81-pin MAPBGA pinout configuration.

	1	2	3	4	5	6	7	8	9
A	IRO	PTG0	PTF6	USB_DP	VBUS	VUSB33	PTF4	PTF3	PTE4
B	PTF7	PTA0	PTG1	USB_DM	PTF5	PTE7	PTF1	PTF0	PTE3
C	PTA4	PTA5	PTA6	PTA1	PTF2	PTE6	PTE5	PTE2	PTE1
D		PTA7	PTB0	PTB1	PTA2	PTA3	PTD5	PTD7	PTE0
E		DADM2		VDD2	VDD3	VDD1	PTD2	PTD3	PTD6
F		DADP2		VSS2	VSS3	VSS1	PTB7	PTC7	PTD4
G	DADP0	DACO	DADP3	DADM3	VREFO	PTB6	PTC0	PTC1	PTC2
H	DADM0	DADM1	DADP1		PTC3	PTC4	PTD0	PTC5	PTC6
J	VSSA	VREFL	VREFH	VDDA	PTB2	PTB3	PTD1	PTB4	PTB5

Figure 4. 81-Pin MAPBGA

Table 3. Package Pin Assignments (Continued)

Package			Default Function	ALT1	ALT2	ALT3	Composite Pin Name
81 MAPBGA	80 LQFP	64 LQFP					
J3	30	25	VREFH	—	—	—	VREFH
J4	31	26	VDDA	—	—	—	VDDA
F4	32	27	VSS2	—	—	—	VSS2
J5	33	28	PTB2	EXTAL1	—	—	PTB2/EXTAL1
J6	34	29	PTB3	XTAL1	—	—	PTB3/XTAL1
E4	35	30	VDD2	—	—	—	VDD2
J8	36	31	PTB4	EXTAL2	—	—	PTB4/EXTAL2
J9	37	32	PTB5	XTAL2	—	—	PTB5/XTAL2
G6	38	—	PTB6	KBI1P3	—	—	PTB6/KBI1P3
F7	39	—	PTB7	KBI1P4	—	—	PTB7/KBI1P4
G7	40	33	PTC0	MOSI2	—	—	PTC0/MOSI2
G8	41	34	PTC1	MISO2	—	—	PTC1/MISO2
G9	42	35	PTC2	KBI1P5	SPSCK2	ADP6	PTC2/KBI1P5/SPSCK2/ADP6
H5	43	36	PTC3	KBI1P6	$\overline{SS2}$	ADP7	PTC3/KBI1P6/$\overline{SS2}$/ADP7
H6	44	37	PTC4	KBI1P7	CMPP0	ADP8	PTC4/KBI1P7/CMPP0/ADP8
H8	45	38	PTC5	KBI2P0	CMPP1	ADP9	PTC5/KBI2P0/CMPP1/ADP9
H9	46	39	PTC6	KBI2P1	PRACMPO	ADP10	PTC6/KBI2P1/PRACMPO/ADP10
F8	47	40	PTC7	KBI2P2	CLKOUT	ADP11	PTC7/KBI2P2/CLKOUT/ADP11
H7	48	41	PTD0	BKGD	MS	—	PTD0/BKGD/MS
J7	49	42	PTD1	CMPP2	$\overline{RESET}$	—	PTD1/CMPP2/$\overline{RESET}$
E7	50	43	PTD2	TPM1CH0	—	—	PTD2TPM1CH0
E8	51	44	PTD3	TPM1CH1	—	—	PTD3/TPM1CH1
F9	52	45	PTD4	SDA	TPM1CH2	—	PTD4/SDA/TPM1CH2
D7	53	46	PTD5	SCL	TPM1CH3	—	PTD5/SCL/TPM1CH3
E9	54	47	PTD6	TX1	—	—	PTD6/TX1
D8	55	48	PTD7	RX1	—	—	PTD7/RX1
D9	56	—	PTE0	KBI2P3	—	—	PTE0/KBI2P3
C9	57	—	PTE1	KBI2P4	—	—	PTE1/KBI2P4
C8	58	—	PTE2	KBI2P5	—	—	PTE2/KBI2P5
B9	59	—	PTE3	KBI2P6	—	—	PTE3/KBI2P6
A9	60	49	PTE4	CMPP3	TPMCLK	IRQ	PTE4/CMPP3/TPMCLK/IRQ

2 Preliminary Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MC9S08JE128/64 microcontroller, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. These specifications will, however, be met for production silicon. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

2.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 4. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

2.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 6. Thermal Characteristics

#	Symbol	Rating	Value	Unit
1	T_A	Operating temperature range (packaged):		°C
		MC9S08JE128	–40 to 105	
		MC9S08JE64	–40 to 105	
2	T_{JMAX}	Maximum junction temperature	135	°C
3	θ_{JA}	Thermal resistance[1,2,3,4] Single-layer board — 1s		°C/W
		81-pin MBGA	77	
		80-pin LQFP	55	
		64-pin LQFP	68	
4	θ_{JA}	Thermal resistance[1, 2, 3, 4] Four-layer board — 2s2p		°C/W
		81-pin MBGA	47	
		80-pin LQFP	40	
		64-pin LQFP	49	

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Junction to Ambient Natural Convection

3 1s — Single layer board, one signal layer

4 2s2p — Four layer board, 2 signal and 2 power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power

$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \qquad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \qquad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

2.4 ESD Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with CDF-AEC-Q00 Stress Test Qualification for Automotive Grade Integrated Circuits. (http://www.aecouncil.com/) This device was qualified to AEC-Q100 Rev E.

A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete dc parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 7. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ω
	Storage Capacitance	C	100	pF
	Number of Pulse per pin	—	3	—
Machine	Series Resistance	R1	0	Ω
	Storage Capacitance	C	200	pF
	Number of Pulse per pin	—	3	—
Latch-up	Minimum input voltage limit	—	–2.5	V
	Maximum input voltage limit	—	7.5	V

Table 8. ESD and Latch-Up Protection Characteristics

#	Rating	Symbol	Min	Max	Unit	C
1	Human Body Model (HBM)	V_{HBM}	±2000	—	V	T
2	Machine Model (MM)	V_{MM}	±200	—	V	T
3	Charge Device Model (CDM)	V_{CDM}	±500	—	V	T
4	Latch-up Current at T_A = 125°C	I_{LAT}	±100	—	mA	T

[7] Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

[8] Maximum is highest voltage that POR is guaranteed.

[9] Run at 1 MHz bus frequency

[10] Low voltage detection and warning limits measured at 1 MHz bus frequency.

[11] Factory trimmed at V_{DD} = 3.0 V, Temp = 25°C

Table 12. PRACMP Electrical Specifications

#	Characteristic	Symbol	Min	Typical	Max	Unit	C
10	Programmable reference generator inputs	$V_{In2}(V_{DD25})$	1.8	—	2.75	V	—
11	Programmable reference generator setup delay	t_{PRGST}	—	1	—	µs	D
12	Programmable reference generator step size	Vstep	–0.25	1	0.25	LSB	D
13	Programmable reference generator voltage range	Vprgout	$V_{In}/32$	—	V_{in}	V	P

2.8 12-bit DAC Electricals

Table 13. DAC 12LV Operating Requirements

#	Characteristic	Symbol	Min	Max	Unit	C	Notes
1	Supply voltage	V_{DDA}	1.8	3.6	V	P	
2	Reference voltage	V_{DACR}	1.15	3.6	V	C	
3	Temperature	T_A	–40	105	°C	C	
4	Output load capacitance	C_L	—	100	pF	C	A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.
5	Output load current	I_L	—	1	mA	C	

Table 14. DAC 12-Bit Operating Behaviors

#	Characteristic	Symbol	Min	Max	Unit	C	Notes
1	Resolution	N	12	12	bit	C	
2	Supply current low-power mode	I_{DDA_DACLP}	50	100	µA	C	
3	Supply current high-power mode	I_{DDA_DACHP}	120	500 (TBD)	µA	C	
4	Full-scale Settling time (±0.5 LSB) (0x080 to 0xF7F or 0xF7F to 0x080) low-power mode	$Ts_{FS}LP$	—	200 (TBD)	µs	C	
5	Full-scale Settling time (±0.5 LSB) (0x080 to 0xF7F or 0xF7F to 0x080) high-power mode	$Ts_{FS}HP$	—	30	µs	C	
6	Code-to-code Settling time (±0.5 LSB) (0xBF8 to 0xC08 or 0xC08 to 0xBF8) low-power mode	$Ts_{C\text{-}C}LP$	—	5	µs	C	
7	Code-to-code Settling time (±0.5 LSB) (0xBF8 to 0xC08 or 0xC08 to 0xBF8) high-power mode	$Ts_{C\text{-}C}HP$	—	1(TBD)	µs	C	
8	DAC output voltage range low (high-power mode, no load, DAC set to 0)	$V_{dacoutl}$	—	100 (TBD)	mV	C	
9	DAC output voltage range high (high-power mode, no load, DAC set to 0x0FFF)	$V_{dacouth}$	V_{DACR}-100	—	mV	C	
10	Integral non-linearity error	INL	—	± 8	LSB	C	
11	Differential non-linearity error VDACR is > 2.4 V	DNL	—	± 1	LSB	C	
12	Offset error	E_O	—	± 0.5	%FSR	C	
13	Gain error	E_G	—	± 0.5 (TBD)	%FSR	C	
14	Power supply rejection ratio $V_{DD} \geq 2.4$ V	PSRR	60	—	dB	C	
15	Temperature drift of offset voltage (DAC set to 0x0800)	T_{co}	—	2 (TBD)	mV	C	See Typical Drift figure that follows.
16	Offset aging coefficient	A_c	—	TBD	µV/yr	C	

Figure 5. Offset at Half Scale vs Temperature

Table 18. XOSC (Temperature Range = –40 to 105°C Ambient)

#	Characteristic		Symbol	Min	Typ[1]	Max	Unit
6	Crystal start-up time [4, 5]	Low range, low gain (RANGE = 0, HGO = 0)	t_{CSTL}	—	200	—	ms
		Low range, high gain (RANGE = 0, HGO = 1)		—	400	—	
		High range, low gain (RANGE = 1, HGO = 0)	t_{CSTH}	—	5	—	
		High range, high gain (RANGE = 1, HGO = 1)		—	15	—	

1 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

2 When MCG is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

3 See crystal or resonator manufacturer's recommendation.

4 This parameter is characterized and not tested on each device.

5 Proper PC board layout procedures must be followed to achieve specifications.

2.11 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

2.11.1 Control Timing

Table 19. Control Timing

#	Symbol	Parameter		Min	Typical[1]	Max	C	Unit
1	f_{Bus}	Bus frequency ($t_{cyc} = 1/f_{Bus}$)						MHz
			$V_{DD} \geq 1.8$ V	dc	—	10	D	
			$V_{DD} > 2.1$ V	dc	—	20	D	
			$V_{DD} > 2.4$ V	dc	—	24	D	
2	t_{LPO}	Internal low-power oscillator period		800	990 (TBD)	1500	D	µs
3	t_{extrst}	External reset pulse width[2] ($t_{cyc} = 1/f_{Self\_reset}$)		100	—	—	D	ns
4	t_{rstdrv}	Reset low drive		66 x t_{cyc}	—	—	D	ns
5	t_{MSSU}	Active background debug mode latch setup time		500	—	—	D	ns
6	t_{MSH}	Active background debug mode latch hold time		100	—	—	D	ns
7	t_{ILIH}, t_{IHIL}	IRQ pulse width • Asynchronous path[2] • Synchronous path[3]		 100 1.5 x t_{cyc}	—	—	D	ns
8	t_{ILIH}, t_{IHIL}	KBIPx pulse width • Asynchronous path[2] • Synchronous path[3]		 100 1.5 x t_{cyc}	—	—	D	ns

2.11.2 TPM Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 20. TPM Input Timing

#	C	Function	Symbol	Min	Max	Unit
1	—	External clock frequency	f_{TPMext}	dc	$f_{Bus}/4$	MHz
2	—	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

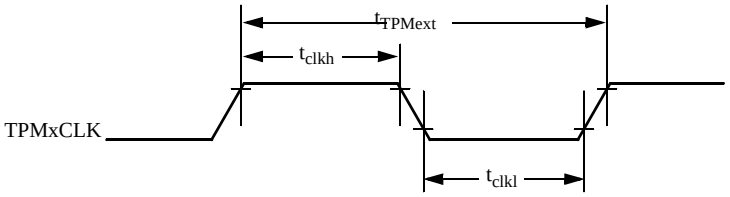


Figure 9. Timer External Clock

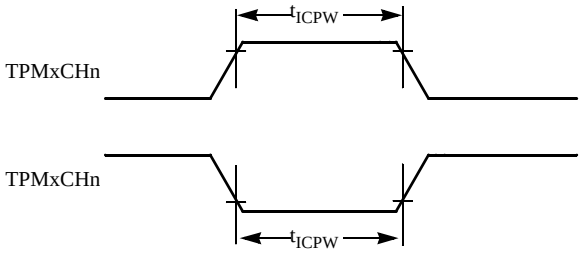
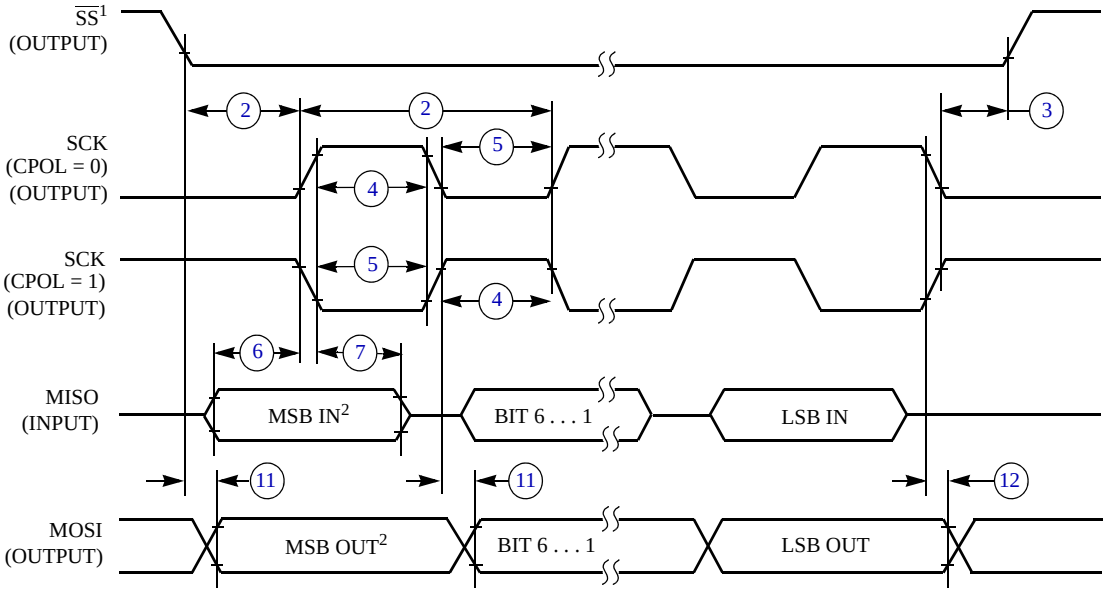
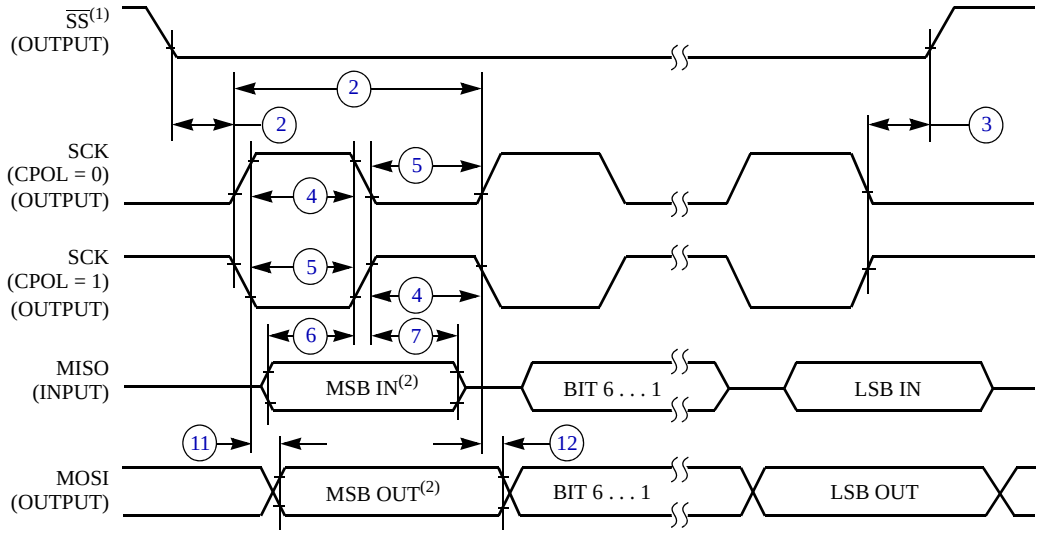


Figure 10. Timer Input Capture Pulse



NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 11. SPI Master Timing (CPHA = 0)



NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 12. SPI Master Timing (CPHA = 1)

2.14 USB Electricals

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit http://www.usb.org.

If the Freescale USB On-the-Go implementation has electrical characteristics that deviate from the standard or require additional information, this space would be used to communicate that information.

Table 23. Internal USB 3.3 V Voltage Regulator Characteristics

#	Characteristic	Symbol	Min	Typ	Max	Unit	C
1	Regulator operating voltage	V_{regin}	3.9	—	5.5	V	C
2	VREG output	V_{regout}	3	3.3	3.6	V	P
3	V_{USB33} input with internal VREG disabled	$V_{usb33in}$	3	3.3	3.6	V	C
4	VREG Quiescent Current	I_{VRQ}	—	0.5	—	mA	C

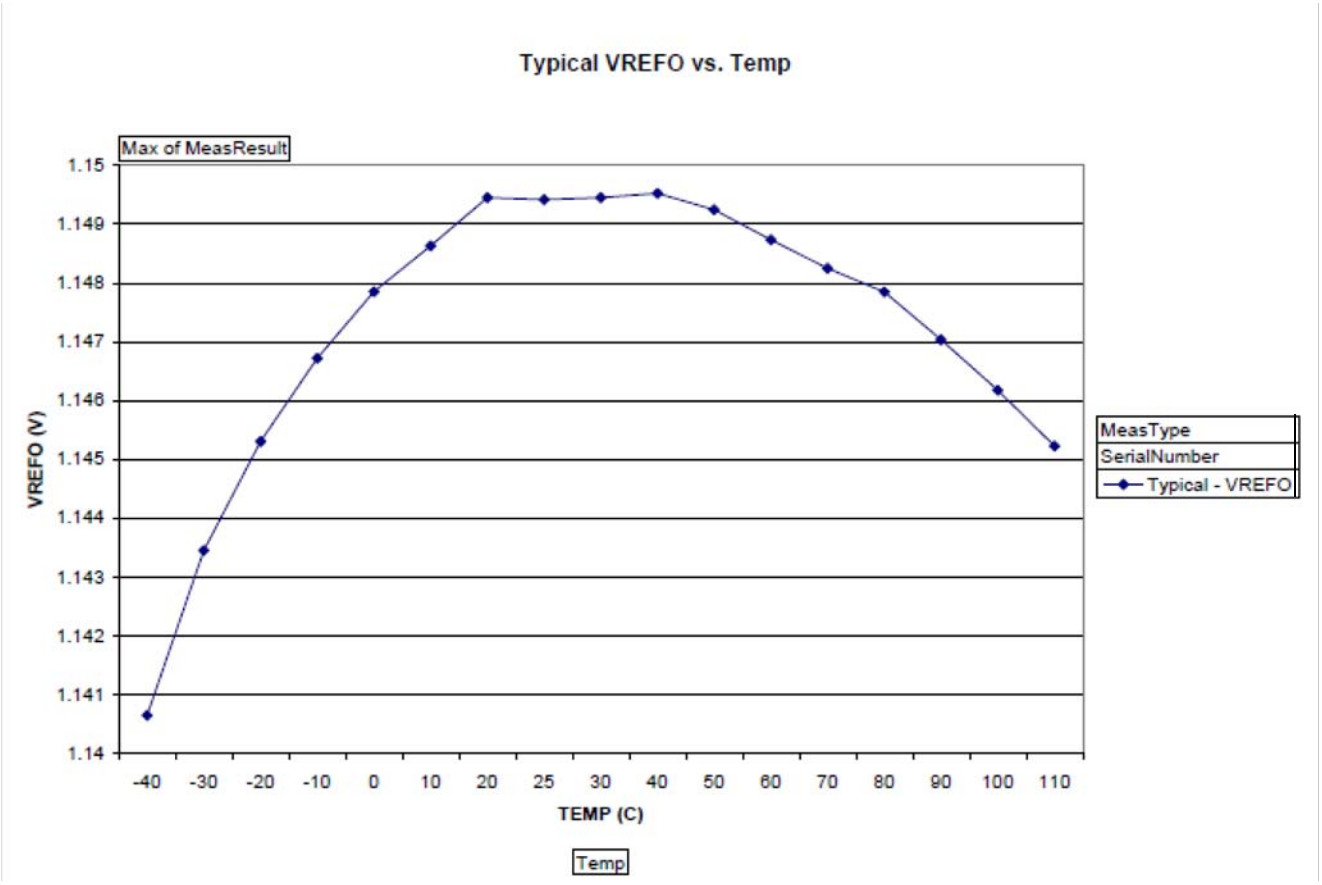


Figure 15. Typical Output vs. Temperature

TBD

Figure 16. Typical Output vs. V_{DD}

3 Ordering Information

This appendix contains ordering information for the device numbering system. MC9S08JE128 and MC9S08JE64 devices.

4 Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

Rev	Date	Description of Changes
0	6/2009	Initial release of the Data Sheet.
1	7/2009	Updated MCG and XOSC Average internal reference frequency.
2	04/2010	Updated electrical characteristic data.

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
http://compass.freescale.net/go/168063291
1-800-441-2447 or 1-303-675-2140
Fax: 1-303-675-2150

LDCForFreescaleSemiconductor@hibbertgroup.com

Document Number: MC9S08JE128
Rev. 3
04/2010

freescale™
semiconductor