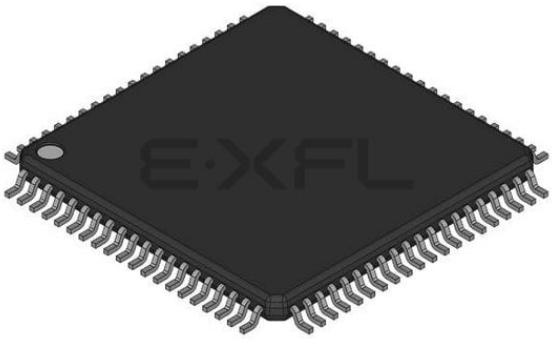

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, SCI, SPI, USB
Peripherals	LVD, POR, PWM, WDT
Number of I/O	46
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s08je128vlk

1 Devices in the MC9S08JE128 series

The following table summarizes the feature set available in the MC9S08JE128 series of MCUs.

Table 1. MC9S08JE128 series Features by MCU and Package

Feature	MC9S08JE128			MC9S08JE64
Pin quantity	81	80	64	64
FLASH size (bytes)	131072			65535
RAM size (bytes)	12K			12K
Programmable Analog Comparator (PRACMP)	yes			yes
Debug Module (DBG)	yes			yes
Multipurpose Clock Generator (MCG)	yes			yes
Inter-Integrated Communication (IIC)	yes			yes
Interrupt Request Pin (IRQ)	yes			yes
Keyboard Interrupt (KBI)	16	16	7	7
Port I/O[1]	47	46	33	33
Dedicated Analog Input Pins	12			12
Power and Ground Pins	8			8
Time Of Day (TOD)	yes			yes
Serial Communications (SCI1)	yes			yes
Serial Communications (SCI2)	yes			yes
Serial Peripheral Interface 1 (SPI1 (FIFO))	yes			yes
Serial Peripheral Interface 2 (SPI2)	yes			yes
Carrier Modulator Timer pin (IRO)	yes			yes
TPM input clock pin (TPMCLK)	yes			yes
TPM1 channels	4			4
TPM2 channels	4	4	2	2
XOSC1	yes			yes
XOSC2	yes			yes
USB	yes			yes
Programmable Delay Block (PDB)	yes			yes
SAR ADC differential channels[2]	4	4	3	3
SAR ADC single-ended channels	8	8	6	6
Voltage reference output pin (VREFO)	yes			yes

1 Port I/O count does not include two (2) output-only and one (1) input-only pins.

2 Each differential channel is comprised of 2 pin inputs.

A complete description of the modules included on each device is provided in the following table.

Table 2. Versions of On-Chip Modules

Module	Version
Analog-to-Digital Converter (ADC12)	1
Digital to Analog Converter (DAC)	1
Programmable Delay Block	1
Inter-Integrated Circuit (IIC)	3
Central Processing Unit (CPU)	5
On-Chip In-Circuit Debug/Emulator (DBG)	3
Multi-Purpose Clock Generator (MCG)	3
Low Power Oscillator (XOSCVLP)	1
Carrier Modulator Timer (CMT)	1
Programable Analog Comparator (PRACMP)	1
Serial Communications Interface (SCI)	4
Serial Peripheral Interface (SPI)	5
Time of Day (TOD)	1
Universal Serial Bus (USB)	1
Timer Pulse-Width Modulator (TPM)	3
System Integration Module (SIM)	1
Cyclic Redundancy Check (CRC)	3
Keyboard Interrupt (KBI)	2
Voltage Reference (VREF)	1
Voltage Regulator (VREG)	1
Interrupt Request (IRQ)	3
Flash Wrapper	1
GPIO	2
Port Control	1

The block diagram in Figure 1 shows the structure of the MC9S08JE128 series MCU.

1.1 Pin Assignments

This section shows the pin assignments for the MC9S08JE128 series devices.

1.1.1 64-Pin LQFP

The following two figures show the 64-pin LQFP pinout configuration.

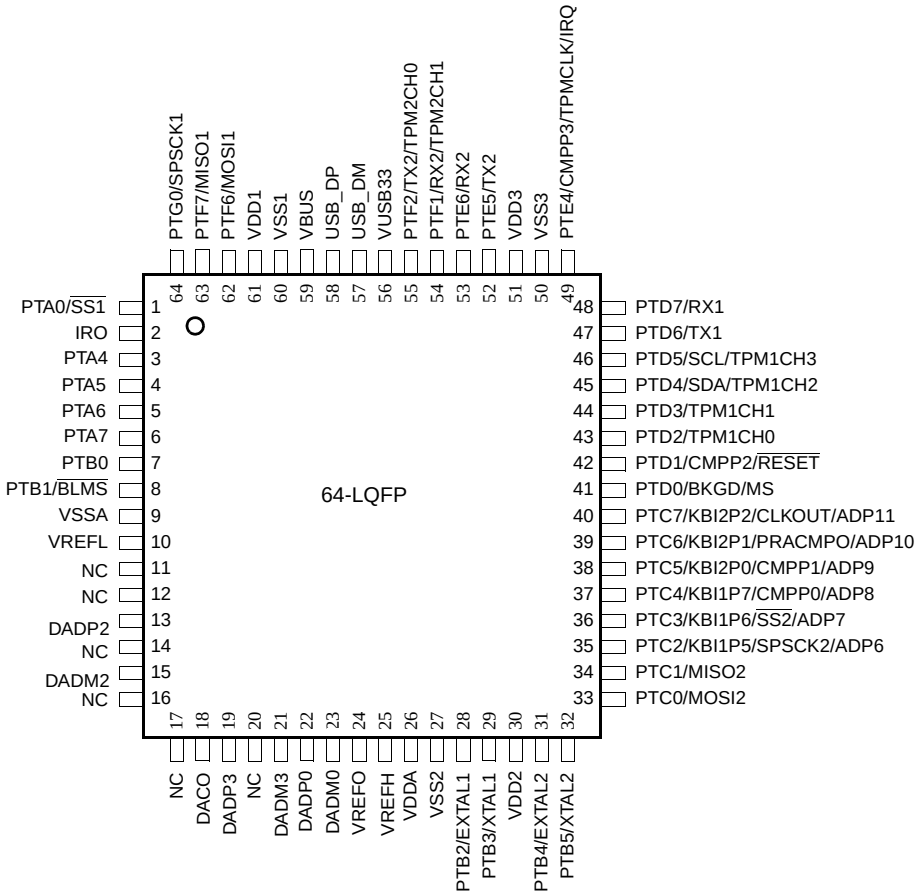

Figure 2. 64-Pin LQFP

1.2 Pin Assignments by Packages

Table 3. Package Pin Assignments

Package			Default Function	ALT1	ALT2	ALT3	Composite Pin Name
81 MAPBGA	80 LQFP	64 LQFP					
B2	1	1	PTA0	$\overline{SS1}$	—	—	PTA0/$\overline{SS1}$
A1	2	2	IRO	—	—	—	IRO
C4	3	—	PTA1	KBI1P0	TX1	—	PTA1/KBI1P0/TX1
D5	4	—	PTA2	KBI1P1	RX1	ADP4	PTA2/KBI1P1/RX1/ADP4
D6	5	—	PTA3	KBI1P2	ADP5	—	PTA3/KBI1P2/ADP5
C1	6	3	PTA4	—	—	—	PTA4
C2	7	4	PTA5	—	—	—	PTA5
C3	8	5	PTA6	—	—	—	PTA6
D2	9	6	PTA7	—	—	—	PTA7
D3	10	7	PTB0	—	—	—	PTB0
D4	11	8	PTB1	$\overline{BLMS}$	—	—	PTB1/$\overline{BLMS}$
J1	12	9	VSSA	—	—	—	VSSA
J2	13	10	VREFL	—	—	—	VREFL
D1	14	11	NC	—	—	—	NC
E1	15	12	NC	—	—	—	NC
F2	16	13	DADP2	—	—	—	DADP2
F1	17	14	NC	—	—	—	NC
E2	18	15	DADM2	—	—	—	DADM2
F3	19	16	NC	—	—	—	NC
E3	20	17	NC	—	—	—	NC
G2	21	18	DACO	—	—	—	DACO
G3	22	19	DADP3	—	—	—	DADP3
H4	23	20	NC	—	—	—	NC
G4	24	21	DADM3	—	—	—	DADM3
G1	25	22	DADP0	—	—	—	DADP0
H1	26	23	DADM0	—	—	—	DADM0
G5	27	24	VREFO	—	—	—	VREFO
H3	28	—	DADP1	—	—	—	DADP1
H2	29	—	DADM1	—	—	—	DADM1

2.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in the following table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

Table 5. Absolute Maximum Ratings

#	Rating	Symbol	Value	Unit
1	Supply voltage	V_{DD}	–0.3 to +3.8	V
2	Maximum current into V_{DD}	I_{DD}	120	mA
3	Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
4	Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	± 25	mA
5	Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}).

2.5 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 9. DC Characteristics

Num	Symbol	Characteristic	Condition	Min	Typ[1]	Max	Unit	C
1	V_{DD}	Operating Voltage	—	1.8[2]	—	3.6	V	—
2	V_{OH}	Output high voltage	All I/O pins, low-drive strength					
			1.8 V, I_{Load} = –600 µA	V_{DD} – 0.5	—	—	V	C
			All I/O pins, high-drive strength					
			2.7 V, I_{Load} = –10 mA	V_{DD} – 0.5	—	—	V	P
			1.8V, I_{Load} = –3 mA	V_{DD} – 0.5	—	—	V	C
3	I_{OHT}	Output high current	Max total I_{OH} for all ports					
			—	—	—	100	mA	D
4	V_{OL}	Output low voltage	All I/O pins, low-drive strength					
			1.8 V, I_{Load} = 600 µA	—	—	0.5	V	C
			All I/O pins, high-drive strength					
			2.7 V, I_{Load} = 10 mA	—	—	0.5	V	P
			1.8 V, I_{Load} = 3 mA	—	—	0.5	V	C
5	I_{OLT}	Output low current	Max total I_{OL} for all ports —	—	—	100	mA	D
6	V_{IH}	Input high voltage	all digital inputs					
			all digital inputs, V_{DD} > 2.7 V	0.70 x V_{DD}	—	—	V	P
			all digital inputs, 2.7 V > V_{DD} ≥ 1.8 V	0.85 x V_{DD}	—	—	V	P

Table 9. DC Characteristics (Continued)

Num	Symbol	Characteristic	Condition	Min	Typ[1]	Max	Unit	C
20	V_{LVDH}[9]	Low-voltage detection threshold — high range	V_{DD} falling					
			—	2.11	2.16	2.22	V	P
			V_{DD} rising					
			—	2.16	2.23	2.27	V	P
21	V_{LVDL}	Low-voltage detection threshold — low range[9]	V_{DD} falling					
			—	1.80	1.84	1.88	V	P
			V_{DD} rising					
			—	1.88	1.93	1.96	V	P
22	V_{LVWH}	Low-voltage warning threshold — high range[9]	V_{DD} falling					
			—	2.36	2.46	2.56	V	P
			V_{DD} rising					
			—	2.36	2.46	2.56	V	P
23	V_{LVWL}	Low-voltage warning threshold — low range[9]	V_{DD} falling					
			—	2.11	2.16	2.22	V	P
			V_{DD} rising					
			—	2.16	2.23	2.27	V	P
24	V_{hys}	Low-voltage inhibit reset/recover hysteresis[10]	—	—	50	—	mV	C
25	V_{BG}	Bandgap Voltage Reference[11]	—	1.15	1.17	1.18	V	P

1 Typical values are measured at 25°C. Characterized, not tested

2 As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above V_{LVDL}.

3 Total Leakage current is the sum value for all GPIO pins; this leakage current is not distributed evenly across all pins but characterization data shows that individual pin leakage current maximums are less than 250 nA.

4 Measured with $V_{In} = V_{DD}$.

5 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

6 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

[7] Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

[8] Maximum is highest voltage that POR is guaranteed.

[9] Run at 1 MHz bus frequency

[10] Low voltage detection and warning limits measured at 1 MHz bus frequency.

[11] Factory trimmed at V_{DD} = 3.0 V, Temp = 25°C

Table 10. Supply Current Characteristics (Continued)

#	Symbol	Parameter	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)	C
5	WI_{DD}	Wait mode supply current — FEI mode, all modules OFF							
			24 MHz	3	TBD	6	mA	–40 to 105	C
			20 MHz	3	TBD	—	mA	–40 to 105	T
			8 MHz	3	TBD	—	mA	–40 to 105	T
			1 MHz	3	TBD	—	mA	–40 to 105	T
6	$S2I_{DD}$	Stop2 mode supply current							
			N/A	3	0.39	0.6	µA	–40 to 25	P
			N/A	3	TBD	TBD	µA	70	C
			N/A	3	7	TBD	µA	85	C
			N/A	3	16	TBD	µA	105	P
			N/A	2	TBD	TBD	µA	–40 to 25	C
			N/A	2	TBD	TBD	µA	70	C
			N/A	2	TBD	TBD	µA	85	C
			N/A	2	TBD	TBD	µA	105	C
7	$S3I_{DD}$	Stop3 mode supply current — No clocks active							
			N/A	3	0.55	0.9	µA	–40 to 25	P
			N/A	3	TBD	TBD	µA	70	C
			N/A	3	14	TBD	µA	85	C
			N/A	3	37	TBD	µA	105	P
			N/A	2	TBD	TBD	µA	–40 to 25	C
			N/A	2	TBD	TBD	µA	70	C
			N/A	2	14	TBD	µA	85	C
			N/A	2	TBD	TBD	µA	105	C

[1] Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

Table 11. Typical Stop Mode Adders

#	Parameter	Condition	Temperature (°C)					Units	C
			-40	25	70	85	105		
1	LPO	—	50	75	100	150	250	nA	D
2	EREFSTEN	RANGE = HGO = 0	600 (TBD)	650 (TBD)	750 (TBD)	850 (TBD)	1000 (TBD)	nA	D
3	IREFSTEN[1]	—	68	70	77	86	120	µA	T
4	TOD	Does not include clock source current	50	75	100	150	250	nA	D
5	LVD[1]	LVDSE = 1	114	115	123	135	170	µA	T
6	ACMP[1]	Not using the bandgap (BGBE = 0)	18	20	23	33	65	µA	T
7	ADC[1]	ADLPC = ADLSMP = 1 Not using the bandgap (BGBE = 0)	75	85	100	115	165	µA	T
8	DAC[1]	High power mode; no load on DACO	500	500	500	500	500	µA	T

1 Not available in stop2 mode.

2.7 PRACMP Electricals

Table 12. PRACMP Electrical Specifications

#	Characteristic	Symbol	Min	Typical	Max	Unit	C
1	Supply voltage	V_{PWR}	1.8	—	3.6	V	P
2	Supply current (active) (PRG enabled)	I_{DDACT1}	—	—	60	µA	C
3	Supply current (active) (PRG disabled)	I_{DDACT2}	—	—	40	µA	C
4	Supply current (ACMP and PRG all disabled)	I_{DDDIS}	—	—	2	nA	D
5	Analog input voltage	VAIN	V_{SS} – 0.3	—	V_{DD}	V	—
6	Analog input offset voltage	VAIO	—	5	40	mV	T
7	Analog comparator hysteresis	V_H	3.0	—	20.0	mV	T
8	Analog input leakage current	I_{ALKG}	—	—	1	nA	D
9	Analog comparator initialization delay	tAINIT	—	—	1.0	µs	T

Table 12. PRACMP Electrical Specifications

#	Characteristic	Symbol	Min	Typical	Max	Unit	C
10	Programmable reference generator inputs	$V_{In2}(V_{DD25})$	1.8	—	2.75	V	—
11	Programmable reference generator setup delay	t_{PRGST}	—	1	—	µs	D
12	Programmable reference generator step size	Vstep	–0.25	1	0.25	LSB	D
13	Programmable reference generator voltage range	Vprgout	$V_{In}/32$	—	V_{in}	V	P

2.8 12-bit DAC Electricals

Table 13. DAC 12LV Operating Requirements

#	Characteristic	Symbol	Min	Max	Unit	C	Notes
1	Supply voltage	V_{DDA}	1.8	3.6	V	P	
2	Reference voltage	V_{DACR}	1.15	3.6	V	C	
3	Temperature	T_A	–40	105	°C	C	
4	Output load capacitance	C_L	—	100	pF	C	A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.
5	Output load current	I_L	—	1	mA	C	

Table 16. 12-bit SAR ADC Characteristics full operating range (V_{REFH} = V_{DDAD}, > 1.8, V_{REFL} = V_{SSAD} ≤ 8 MHz)

Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	C	Comment
Supply Current	ADLPC=1, ADHSC=0	I_{DDAD}	—	215	—	μA	T	ADLSMP=0 ADCO=1
	ADLPC=0, ADHSC=0		—	470	—			
	ADLPC=0, ADHSC=1		—	610	—			
Supply Current	Stop, Reset, Module Off	I_{DDAD}	—	0.01	—	μA	C	
ADC Asynchronous Clock Source	ADLPC=1, ADHSC=0	f_{ADACK}	—	2.4	—	MHz	P	t_{ADACK} = $1/f_{ADACK}$
	ADLPC=0, ADHSC=0		—	5.2	—			
	ADLPC=0, ADHSC=1		—	6.2	—			
Sample Time	See Block Guide for sample times							
Conversion Time	See Block Guide for conversion times							
Total Unadjusted Error	12-bit single-ended mode	TUE	—	±1.75	±3.5	LSB[3]	T	32x Hardware Averaging (AVGE = %1 AVGS = %11)
	11-bit differential mode 10-bit single-ended mode		— —	±0.7 ±0.8	±1.5 ±1.5		T	
	9-bit differential mode 8-bit single-ended mode		— —	±0.5 ±0.5	±1.0 ±1.0		T	
Differential Non-Linearity	12-bit single-ended mode	DNL	—	±0.7	±1	LSB[2]	T	
	11-bit differential mode 10-bit single-ended mode		— —	±0.5 ±0.5	±0.75 ±0.75		T	
	9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	
Integral Non-Linearity	12-bit single-ended mode	INL	—	±1.0	±2.5	LSB[2]	T	
	11-bit differential mode 10-bit single-ended mode		— —	±0.5 ±0.5	±1.0 ±1.0		T	
	9-bit differential mode 8-bit single-ended mode		— —	±0.3 ±0.3	±0.5 ±0.5		T	

Table 16. 12-bit SAR ADC Characteristics full operating range (V_{REFH} = V_{DDAD}, > 1.8, V_{REFL} = V_{SSAD} ≤ 8 MHz) (Continued)

Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	C	Comment
Zero-Scale Error	12-bit single-ended mode	E_{ZS}	—	±0.7	±2.0	LSB[2]	T	V_{ADIN} = V_{SSAD}
	11-bit differential mode 10-bit single-ended mode		— —	±0.4 ±0.4	±1.0 ±1.0		T	
	9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	
Full-Scale Error	12-bit single-ended mode	E_{FS}	—	±1.0	±3.5	LSB[2]	T	V_{ADIN} = V_{DDAD}
	11-bit differential mode 10-bit single-ended mode		— —	±0.4 ±0.4	±1.5 ±1.5		T	
	9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	
Quantization Error	All modes	E_Q	—	—	±0.5	LSB[2]	D	
Input Leakage Error	all modes	E_{IL}	I_{In} * R_{AS}			mV	D	I_{In} = leakage current (refer to DC characteristics)
Temp Sensor Slope	–40°C – 25°C	m	—	1.646	—	mV/×C	C	
	25°C – 125°C		—	1.769	—			
Temp Sensor Voltage	25°C	V_{TEMP25}	—	701.2	—	mV	C	

1 All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDAD}

2 Typical values assume V_{DDAD} = 3.0V, Temp = 25°C, f_{ADCK}=2.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3 1 LSB = (V_{REFH} - V_{REFL})/2^N

2.10 MCG and External Oscillator (XOSC) Characteristics

Table 17. MCG (Temperature Range = –40 to 105°C Ambient)

#	Rating		Symbol	Min	Typical	Max	Unit	C
1	Internal reference startup time		t_{irefst}	—	55	100	µs	D
2	Average internal reference frequency	factory trimmed at VDD=3.0 V and temp=25°C	f_{int_ft}	—	31.25	—	kHz	C
		user trimmed		31.25	—	39.0625		C
3	DCO output frequency range - trimmed	Low range (DRS=00)	f_{dco_t}	16	—	20	MHz	C
		Mid range (DRS=01)		32	—	40		C
		High range[1] (DRS=10)		40	—	60		C
4	Resolution of trimmed DCO output frequency at fixed voltage and temperature	with FTRIM	$\Delta f_{dco\_res\_t}$	—	± 0.1	± 0.2	$\%f_{dco}$	C
		without FTRIM		—	± 0.2	± 0.4		C
5	Total deviation of trimmed DCO output frequency over voltage and temperature	over voltage and temperature	Δf_{dco_t}	—	±1.0	± 2	$\%f_{dco}$	p
		over fixed voltage and temp range of 0 - 70 °C		—	± 0.5	± 1		C
6	Acquisition time	FLL[2]	$t_{fll\_acquire}$	—	—	1	ms	C
		PLL[3]	$t_{pll\_acquire}$	—	—	1		D
7	Long term Jitter of DCO output clock (averaged over 2mS interval) [4]		C_{Jitter}	—	0.02	0.2	$\%f_{dco}$	C
8	VCO operating frequency		f_{vco}	7.0	—	55.0	MHz	D
9	PLL reference frequency range		f_{pll_ref}	1.0	—	2.0	MHz	D
10	Jitter of PLL output clock measured over 625ns [5]	Long term	$f_{pll\_jitter\_625\ ns}$	—	0.566[4]	—	$\%f_{pll}$	D
11	Lock frequency tolerance	Entry[6]	D_{lock}	± 1.49	—	± 2.98	%	D
		Exit[7]	D_{unl}	± 4.47	—	± 5.97		D
12	Lock time	FLL	t_{fll_lock}	—	—	$t_{fll\_acquire}$+ 1075(1/f_{int_t})	s	D
		PLL	t_{pll_lock}	—	—	$t_{pll\_acquire}$+ 1075(1/f_{pll_ref})		D
13	Loss of external clock minimum frequency - RANGE = 0		f_{loc_low}	(3/5) x f_{int_t}	—	—	kHz	D
14	Loss of external clock minimum frequency - RANGE = 1		f_{loc_high}	(16/5) x f_{int_t}	—	—	kHz	D

1 This should not exceed the maximum CPU frequency for this device.

2 This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bit is changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

2.11 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

2.11.1 Control Timing

Table 19. Control Timing

#	Symbol	Parameter		Min	Typical[1]	Max	C	Unit
1	f_{Bus}	Bus frequency ($t_{cyc} = 1/f_{Bus}$)						MHz
			$V_{DD} \geq 1.8$ V	dc	—	10	D	
			$V_{DD} > 2.1$ V	dc	—	20	D	
			$V_{DD} > 2.4$ V	dc	—	24	D	
2	t_{LPO}	Internal low-power oscillator period		800	990 (TBD)	1500	D	µs
3	t_{extrst}	External reset pulse width[2] ($t_{cyc} = 1/f_{Self\_reset}$)		100	—	—	D	ns
4	t_{rstdrv}	Reset low drive		66 x t_{cyc}	—	—	D	ns
5	t_{MSSU}	Active background debug mode latch setup time		500	—	—	D	ns
6	t_{MSH}	Active background debug mode latch hold time		100	—	—	D	ns
7	t_{ILIH}, t_{IHIL}	IRQ pulse width • Asynchronous path[2] • Synchronous path[3]		 100 1.5 x t_{cyc}	—	—	D	ns
8	t_{ILIH}, t_{IHIL}	KBIPx pulse width • Asynchronous path[2] • Synchronous path[3]		 100 1.5 x t_{cyc}	—	—	D	ns

Table 19. Control Timing

#	Symbol	Parameter	Min	Typical[1]	Max	C	Unit
9	t_{Rise}, t_{Fall}	Port rise and fall time (load = 50 pF)[4], Low Drive					ns
		Slew rate control disabled (PTxSE = 0)	—	11	—	D	
		Slew rate control enabled (PTxSE = 1)	—	35	—	D	
		Slew rate control disabled (PTxSE = 0)	—	40	—	D	
		Slew rate control enabled (PTxSE = 1)	—	75	—	D	

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

3 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

4 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 105 °C.

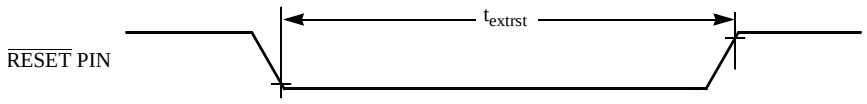

Figure 7. Reset Timing

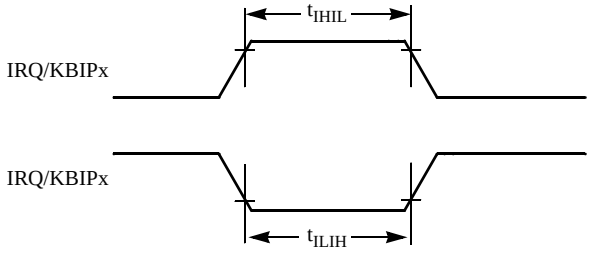

Figure 8. IRQ/KBIPx Timing

2.12 SPI Characteristics

Table 21 and Figure 11 through Figure 14 describe the timing requirements for the SPI system.

Table 21. SPI Timing

No.[1]	Characteristic[2]	Symbol	Min	Max	Unit	C
1	Operating frequency Master Slave	f_{op}	 $f_{Bus}/2048$ 0	 $f_{Bus}/2$ $f_{Bus}/4$	 Hz Hz	D
2	SPSCK period Master Slave	t_{SPSCK}	 2 4	 2048 —	 t_{cyc} t_{cyc}	D
3	Enable lead time Master Slave	t_{Lead}	 1/2 1	 — —	 t_{SPSCK} t_{cyc}	D
4	Enable lag time Master Slave	t_{Lag}	 1/2 1	 — —	 t_{SPSCK} t_{cyc}	D
5	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	 $t_{cyc} - 30$ $t_{cyc} - 30$	 1024 t_{cyc} —	 ns ns	D
6	Data setup time (inputs) Master Slave	t_{SU} t_{SU}	 15 15	 — —	 ns ns	D
7	Data hold time (inputs) Master Slave	t_{HI} t_{HI}	 0 25	 — —	 ns ns	D
8	Slave access time[3]	t_a	—	1	t_{cyc}	D
9	Slave MISO disable time[4]	t_{dis}	—	1	t_{cyc}	D
10	Data valid (after SPSCK edge) Master Slave	t_v	 — —	 25 25	 ns ns	D
11	Data hold time (outputs) Master Slave	t_{HO}	 0 0	 — —	 ns ns	D
12	Rise time Input Output	 t_{RI} t_{RO}	 — —	 $t_{cyc} - 25$ 25	 ns ns	D
13	Fall time Input Output	 t_{FI} t_{FO}	 — —	 $t_{cyc} - 25$ 25	 ns ns	D

1 Numbers in this column identify elements in Figure 11 through Figure 14.

2 All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless noted; 100 pF load on all SPI pins. All timing assumes slew rate control disabled and high drive strength enabled for SPI output pins.

3 Time to data active from high-impedance state.

4 Hold time to high-impedance state.

2.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory chapter in the Reference Manual for this device (MC9S08JE128RM).

Table 22. Flash Characteristics

#	Characteristic	Symbol	Min	Typical	Max	Unit	C
1	Supply voltage for program/erase -40°C to 105°C	$V_{prog/erase}$	1.8	—	3.6	V	D
2	Supply voltage for read operation	V_{Read}	1.8	—	3.6	V	D
3	Internal FCLK frequency[1]	f_{FCLK}	150	—	200	kHz	D
4	Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	µs	D
5	Byte program time (random location)[2]	t_{prog}	9			t_{Fcyc}	P
6	Byte program time (burst mode)[2]	t_{Burst}	4			t_{Fcyc}	P
7	Page erase time[2]	t_{Page}	4000			t_{Fcyc}	P
8	Mass erase time[2]	t_{Mass}	20,000			t_{Fcyc}	P
9	Program/erase endurance[3] T_L to T_H = –40°C to + 105°C T = 25°C		10,000 —	— 100,000	— —	cycles	C
10	Data retention[4]	t_{D_ret}	15	100	—	years	C

1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 **Typical endurance for flash** was evaluated for this product family on the HC9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory*.

4 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.*

3.1 Device Numbering System

Example of the device numbering system:

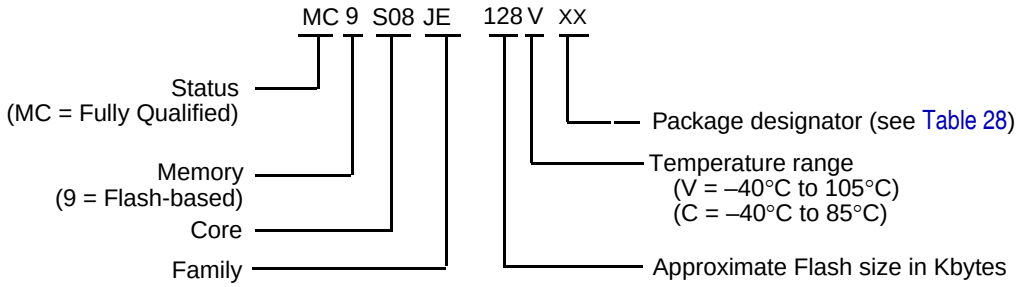

Table 27. Device Numbering System

Device Number[1]	Memory		Available Packages[2]
	Flash	RAM	
MC9S08JE128	131,072	12,288	64 LQFP
	131,072	12,288	80 LQFP
	131,072	12,288	81 MAPBGA
MC9S08JE64	65,536	12,288	64 LQFP

1 See Table 2 for a complete description of modules included on each device.

2 See Table 28 for package information.

3.2 Package Information

Table 28. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
64	Low Quad Flat Package	LQFP	LH	840F-02	98ASS23234W
80	Low Quad Flat Package	LQFP	LK	917-01	98ASS23174W
81	MAPBGA Package	Map PBGA	MB	1662-01	98ASA10670D

3.3 Mechanical Drawings

Table 28 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MC9S08JE128 series Product Summary pages at http://www.freescale.com.

To view the latest drawing, either:

- Click on the appropriate link in Table 28, or
- Open a browser to the Freescale® website (http://www.freescale.com), and enter the appropriate document number (from Table 28) in the “Enter Keyword” search box at the top of the page.

4 Revision History

To provide the most up-to-date information, the revision of our documents on the World Wide Web will be the most current. Your printed copy may be an earlier revision. To verify you have the latest information available, refer to:

http://freescale.com/

The following revision history table summarizes changes contained in this document.

Rev	Date	Description of Changes
0	6/2009	Initial release of the Data Sheet.
1	7/2009	Updated MCG and XOSC Average internal reference frequency.
2	04/2010	Updated electrical characteristic data.