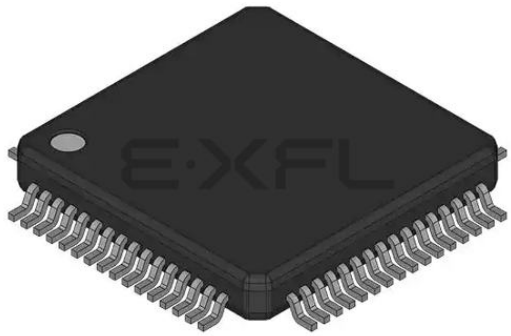

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	S08
Core Size	8-Bit
Speed	48MHz
Connectivity	I²C, SCI, SPI, USB
Peripherals	LVD, POR, PWM, WDT
Number of I/O	33
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 6x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc9s08je64clh

Contents

Related Documentation

Find the most current versions of all documents at: http://www.freescale.com.

Reference Manual —MC9S08JE128RM

Contains extensive product information including modes of operation, memory, resets and interrupts, register definition, port pins, CPU, and all module information.

–

1 Devices in the MC9S08JE128 series

The following table summarizes the feature set available in the MC9S08JE128 series of MCUs.

Table 1. MC9S08JE128 series Features by MCU and Package

Feature	MC9S08JE128			MC9S08JE64
Pin quantity	81	80	64	64
FLASH size (bytes)	131072			65535
RAM size (bytes)	12K			12K
Programmable Analog Comparator (PRACMP)	yes			yes
Debug Module (DBG)	yes			yes
Multipurpose Clock Generator (MCG)	yes			yes
Inter-Integrated Communication (IIC)	yes			yes
Interrupt Request Pin (IRQ)	yes			yes
Keyboard Interrupt (KBI)	16	16	7	7
Port I/O[1]	47	46	33	33
Dedicated Analog Input Pins	12			12
Power and Ground Pins	8			8
Time Of Day (TOD)	yes			yes
Serial Communications (SCI1)	yes			yes
Serial Communications (SCI2)	yes			yes
Serial Peripheral Interface 1 (SPI1 (FIFO))	yes			yes
Serial Peripheral Interface 2 (SPI2)	yes			yes
Carrier Modulator Timer pin (IRO)	yes			yes
TPM input clock pin (TPMCLK)	yes			yes
TPM1 channels	4			4
TPM2 channels	4	4	2	2
XOSC1	yes			yes
XOSC2	yes			yes
USB	yes			yes
Programmable Delay Block (PDB)	yes			yes
SAR ADC differential channels[2]	4	4	3	3
SAR ADC single-ended channels	8	8	6	6
Voltage reference output pin (VREFO)	yes			yes

1 Port I/O count does not include two (2) output-only and one (1) input-only pins.

2 Each differential channel is comprised of 2 pin inputs.

1.1 Pin Assignments

This section shows the pin assignments for the MC9S08JE128 series devices.

1.1.1 64-Pin LQFP

The following two figures show the 64-pin LQFP pinout configuration.

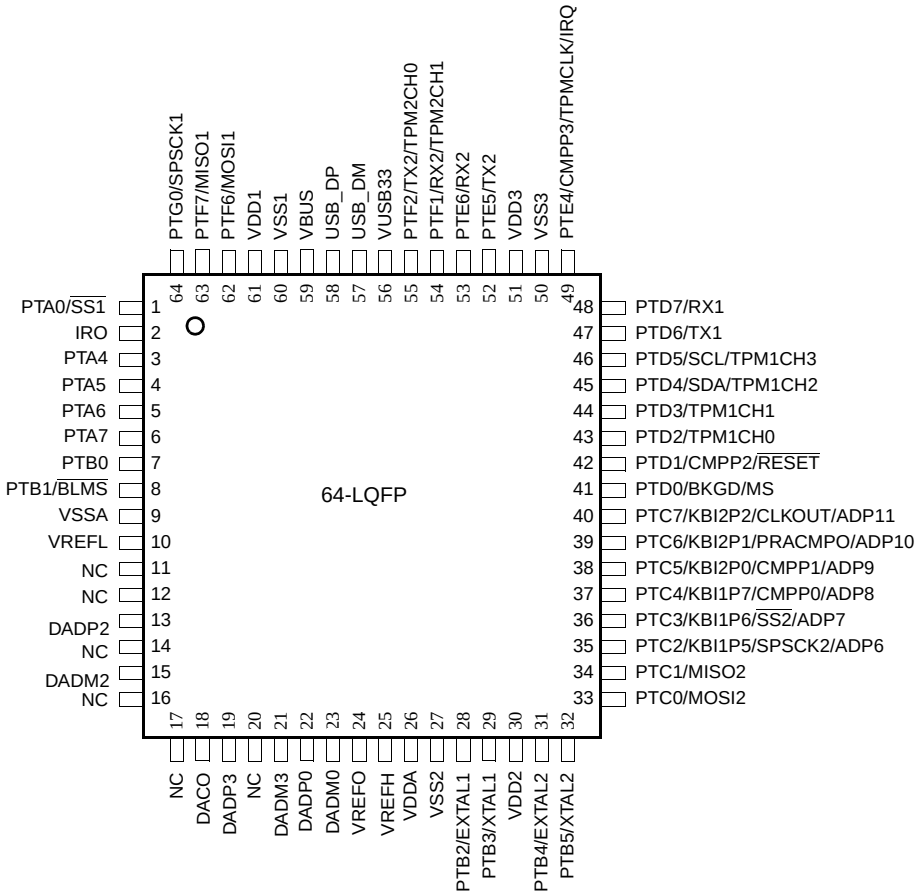


Figure 2. 64-Pin LQFP

Table 3. Package Pin Assignments (Continued)

Package			Default Function	ALT1	ALT2	ALT3	Composite Pin Name
81 MAPBGA	80 LQFP	64 LQFP					
F5	61	50	VSS3	—	—	—	VSS3
E5	62	51	VDD3	—	—	—	VDD3
C7	63	52	PTE5	TX2	—	—	PTE5/TX2
C6	64	53	PTE6	RX2	—	—	PTE6/RX2
B6	65	—	PTE7	TPM2CH3	—	—	PTE7/TPM2CH3
B8	66	—	PTF0	TPM2CH2	—	—	PTF0/TPM2CH2
B7	67	54	PTF1	RX2	TPM2CH1	—	PTF1/RX2/TPM2CH1
C5	68	55	PTF2	TX2	TPM2CH0	—	PTF2/TX2/TPM2CH0
A8	69	—	PTF3	SCL	—	—	PTF3/SCL
A7	70	—	PTF4	SDA	—	—	PTF4/SDA
B5	71	—	PTF5	KBI2P7	—	—	PTF5/KBI2P7
A6	72	56	VUSB33	—	—	—	VUSB33
B4	73	57	USB_DM	—	—	—	USB_DM
A4	74	58	USB_DP	—	—	—	USB_DP
A5	75	59	VBUS	—	—	—	VBUS
F6	76	60	VSS1	—	—	—	VSS1
E6	77	61	VDD1	—	—	—	VDD1
A3	78	62	PTF6	MOSI1	—	—	PTF6/MOSI1
B1	79	63	PTF7	MISO1	—	—	PTF7/MISO1
A2	80	64	PTG0	SPSCK1	—	—	PTG0/SPSCK1
B3	—	—	PTG1	—	—	—	PTG1

2 Preliminary Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MC9S08JE128/64 microcontroller, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. These specifications will, however, be met for production silicon. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

2.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 4. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

2.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in the following table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

Table 5. Absolute Maximum Ratings

#	Rating	Symbol	Value	Unit
1	Supply voltage	V_{DD}	–0.3 to +3.8	V
2	Maximum current into V_{DD}	I_{DD}	120	mA
3	Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
4	Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	± 25	mA
5	Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}).

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \qquad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

2.4 ESD Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with CDF-AEC-Q00 Stress Test Qualification for Automotive Grade Integrated Circuits. (http://www.aecouncil.com/) This device was qualified to AEC-Q100 Rev E.

A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete dc parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 7. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ω
	Storage Capacitance	C	100	pF
	Number of Pulse per pin	—	3	—
Machine	Series Resistance	R1	0	Ω
	Storage Capacitance	C	200	pF
	Number of Pulse per pin	—	3	—
Latch-up	Minimum input voltage limit	—	–2.5	V
	Maximum input voltage limit	—	7.5	V

Table 8. ESD and Latch-Up Protection Characteristics

#	Rating	Symbol	Min	Max	Unit	C
1	Human Body Model (HBM)	V_{HBM}	±2000	—	V	T
2	Machine Model (MM)	V_{MM}	±200	—	V	T
3	Charge Device Model (CDM)	V_{CDM}	±500	—	V	T
4	Latch-up Current at T_A = 125°C	I_{LAT}	±100	—	mA	T

Table 9. DC Characteristics (Continued)

Num	Symbol	Characteristic	Condition	Min	Typ[1]	Max	Unit	C
7	V_{IL}	Input low voltage all digital inputs						
			all digital inputs, $V_{DD} > 2.7$ V	—	—	0.35 x V_{DD}	V	P
			all digital inputs, $2.7 > V_{DD} \geq 1.8$ V	—	—	0.30 x V_{DD}	V	P
8	V_{hys}	Input hysteresis all digital inputs	—	0.06 x V_{DD}	—	—	mV	C
9	$\|I_{In}\|$	Input leakage current all input only pins (Per pin)	$V_{In} = V_{DD}$ or V_{SS}	—	—	0.25 (TBD)	µA	P
10	$\|I_{OZ}\|$	Hi-Z (off-state) leakage current all input/output (per pin)	$V_{In} = V_{DD}$ or V_{SS}	—	—	1(TBD)	µA	P
11	$\|I_{OZ}\|$	Leakage current for analog output pins (DACO, VREFO) all input/output (per pin)	$V_{In} = V_{DD}$ or V_{SS}	—	—	(TBD)	µA	P
12	$\|I_{InT}\|$	Total Leakage Current[3] For all pins		—	—	2	µA	D
13	R_{PU}	Pull-up resistors	—	17.5	—	52.5	kΩ	P
14	R_{PD}	Internal pull-down resistors[4]	—	17.5	—	52.5	kΩ	P
15	I_{IC}	DC injection current [5, 6, 7] Single pin limit						
			$V_{SS} > V_{IN} > V_{DD}$	–0.2	—	0.2	mA	D
		Total MCU limit, includes sum of all stressed pins						
			$V_{SS} > V_{IN} > V_{DD}$	–5	—	5	mA	D
16	C_{In}	Input Capacitance, all pins	—	—	—	8	pF	C
17	V_{RAM}	RAM retention voltage	—	—	0.6	1.0	V	C
18	V_{POR}	POR re-arm voltage[8]	—	0.9	1.4	1.79	V	C
19	t_{POR}	POR re-arm time	—	10	—	—	µs	D

Table 9. DC Characteristics (Continued)

Num	Symbol	Characteristic	Condition	Min	Typ[1]	Max	Unit	C
20	V_{LVDH}[9]	Low-voltage detection threshold — high range	V_{DD} falling					
			—	2.11	2.16	2.22	V	P
			V_{DD} rising					
			—	2.16	2.23	2.27	V	P
21	V_{LVDL}	Low-voltage detection threshold — low range[9]	V_{DD} falling					
			—	1.80	1.84	1.88	V	P
			V_{DD} rising					
			—	1.88	1.93	1.96	V	P
22	V_{LVWH}	Low-voltage warning threshold — high range[9]	V_{DD} falling					
			—	2.36	2.46	2.56	V	P
			V_{DD} rising					
			—	2.36	2.46	2.56	V	P
23	V_{LVWL}	Low-voltage warning threshold — low range[9]	V_{DD} falling					
			—	2.11	2.16	2.22	V	P
			V_{DD} rising					
			—	2.16	2.23	2.27	V	P
24	V_{hys}	Low-voltage inhibit reset/recover hysteresis[10]	—	—	50	—	mV	C
25	V_{BG}	Bandgap Voltage Reference[11]	—	1.15	1.17	1.18	V	P

1 Typical values are measured at 25°C. Characterized, not tested

2 As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above V_{LVDL}.

3 Total Leakage current is the sum value for all GPIO pins; this leakage current is not distributed evenly across all pins but characterization data shows that individual pin leakage current maximums are less than 250 nA.

4 Measured with $V_{In} = V_{DD}$.

5 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

6 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

Table 10. Supply Current Characteristics (Continued)

#	Symbol	Parameter	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)	C
5	WI_{DD}	Wait mode supply current — FEI mode, all modules OFF							
			24 MHz	3	TBD	6	mA	–40 to 105	C
			20 MHz	3	TBD	—	mA	–40 to 105	T
			8 MHz	3	TBD	—	mA	–40 to 105	T
			1 MHz	3	TBD	—	mA	–40 to 105	T
6	$S2I_{DD}$	Stop2 mode supply current							
			N/A	3	0.39	0.6	µA	–40 to 25	P
			N/A	3	TBD	TBD	µA	70	C
			N/A	3	7	TBD	µA	85	C
			N/A	3	16	TBD	µA	105	P
			N/A	2	TBD	TBD	µA	–40 to 25	C
			N/A	2	TBD	TBD	µA	70	C
			N/A	2	TBD	TBD	µA	85	C
			N/A	2	TBD	TBD	µA	105	C
7	$S3I_{DD}$	Stop3 mode supply current — No clocks active							
			N/A	3	0.55	0.9	µA	–40 to 25	P
			N/A	3	TBD	TBD	µA	70	C
			N/A	3	14	TBD	µA	85	C
			N/A	3	37	TBD	µA	105	P
			N/A	2	TBD	TBD	µA	–40 to 25	C
			N/A	2	TBD	TBD	µA	70	C
			N/A	2	14	TBD	µA	85	C
			N/A	2	TBD	TBD	µA	105	C

[1] Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

Table 12. PRACMP Electrical Specifications

#	Characteristic	Symbol	Min	Typical	Max	Unit	C
10	Programmable reference generator inputs	$V_{In2}(V_{DD25})$	1.8	—	2.75	V	—
11	Programmable reference generator setup delay	t_{PRGST}	—	1	—	µs	D
12	Programmable reference generator step size	Vstep	–0.25	1	0.25	LSB	D
13	Programmable reference generator voltage range	Vprgout	$V_{In}/32$	—	V_{in}	V	P

2.8 12-bit DAC Electricals

Table 13. DAC 12LV Operating Requirements

#	Characteristic	Symbol	Min	Max	Unit	C	Notes
1	Supply voltage	V_{DDA}	1.8	3.6	V	P	
2	Reference voltage	V_{DACR}	1.15	3.6	V	C	
3	Temperature	T_A	–40	105	°C	C	
4	Output load capacitance	C_L	—	100	pF	C	A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.
5	Output load current	I_L	—	1	mA	C	

2.9 ADC Characteristics

Table 15. 12-bit ADC Operating Conditions

#	Symb	Characteristic	Conditions	Min	Typ[1]	Max	Unit	C	Comment
1	V_{DDAD}	Supply voltage	Absolute	1.8	—	3.6	V	D	
2	ΔV_{DDAD}		Delta to V_{DD} (V_{DD}-V_{DDAD})[2]	-100	0	+100	mV	D	
3	ΔV_{SSAD}	Ground voltage	Delta to V_{SS} (V_{SS}-V_{SSAD})[2]	-100	0	+100	mV	D	
4	V_{REFH}	Ref Voltage High		1.13	V_{DDAD}	V_{DDAD}	V	D	
5	V_{REFL}	Ref Voltage Low		V_{SSAD}	V_{SSAD}	V_{SSAD}	V	D	
6	V_{ADIN}	Input Voltage		V_{REFL}	—	V_{REFH}	V	D	
7	C_{ADIN}	Input Capacitance		—	4	5	pF	C	
8	R_{ADIN}	Input Resistance		—	2	5	kΩ	C	
9	R_{AS}	Analog Source Resistance							External to MCU Assumes ADLSMP=0
			12-bit mode f_{ADCK} > 4 MHz	—	—	2	kΩ	C	
			f_{ADCK} < 4 MHz	—	—	5	kΩ	C	
			11/10-bit mode f_{ADCK} > 8 MHz	—	—	2	kΩ	C	
			4 MHz < f_{ADCK} < 8 MHz	—	—	5	kΩ	C	
			f_{ADCK} < 4 MHz	—	—	10	kΩ	C	
			9/8-bit mode f_{ADCK} > 4 MHz	—	—	5	kΩ	C	
			f_{ADCK} < 4 MHz	—	—	10	kΩ	C	
10	f_{ADCK}	ADC Conversion Clock Freq.	High Speed (ADLPC=0, ADHSC=1)	1.0	—	8.0	MHz	D	
			High Speed (ADLPC=0, ADHSC=0)	1.0	—	5.0	MHz	D	
			Low Power (ADLPC=1, ADHSC=1)	1.0	—	2.5	MHz	D	

1 Typical values assume V_{DDAD} = 3.0 V, Temp = 25 °C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

Table 16. 12-bit SAR ADC Characteristics full operating range (V_{REFH} = V_{DDAD}, > 1.8, V_{REFL} = V_{SSAD} ≤ 8 MHz) (Continued)

Characteristic	Conditions[1]	Symb	Min	Typ[2]	Max	Unit	C	Comment
Zero-Scale Error	12-bit single-ended mode	E_{ZS}	—	±0.7	±2.0	LSB[2]	T	V_{ADIN} = V_{SSAD}
	11-bit differential mode 10-bit single-ended mode		— —	±0.4 ±0.4	±1.0 ±1.0		T	
	9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	
Full-Scale Error	12-bit single-ended mode	E_{FS}	—	±1.0	±3.5	LSB[2]	T	V_{ADIN} = V_{DDAD}
	11-bit differential mode 10-bit single-ended mode		— —	±0.4 ±0.4	±1.5 ±1.5		T	
	9-bit differential mode 8-bit single-ended mode		— —	±0.2 ±0.2	±0.5 ±0.5		T	
Quantization Error	All modes	E_Q	—	—	±0.5	LSB[2]	D	
Input Leakage Error	all modes	E_{IL}	I_{In} * R_{AS}			mV	D	I_{In} = leakage current (refer to DC characteristics)
Temp Sensor Slope	–40°C – 25°C	m	—	1.646	—	mV/×C	C	
	25°C – 125°C		—	1.769	—			
Temp Sensor Voltage	25°C	V_{TEMP25}	—	701.2	—	mV	C	

1 All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDAD}

2 Typical values assume V_{DDAD} = 3.0V, Temp = 25°C, f_{ADCK}=2.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3 1 LSB = (V_{REFH} - V_{REFL})/2^N

2.11 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

2.11.1 Control Timing

Table 19. Control Timing

#	Symbol	Parameter		Min	Typical[1]	Max	C	Unit
1	f_{Bus}	Bus frequency ($t_{cyc} = 1/f_{Bus}$)						MHz
			$V_{DD} \geq 1.8$ V	dc	—	10	D	
			$V_{DD} > 2.1$ V	dc	—	20	D	
			$V_{DD} > 2.4$ V	dc	—	24	D	
2	t_{LPO}	Internal low-power oscillator period		800	990 (TBD)	1500	D	µs
3	t_{extrst}	External reset pulse width[2] ($t_{cyc} = 1/f_{Self\_reset}$)		100	—	—	D	ns
4	t_{rstdrv}	Reset low drive		66 x t_{cyc}	—	—	D	ns
5	t_{MSSU}	Active background debug mode latch setup time		500	—	—	D	ns
6	t_{MSH}	Active background debug mode latch hold time		100	—	—	D	ns
7	t_{ILIH}, t_{IHIL}	IRQ pulse width • Asynchronous path[2] • Synchronous path[3]		 100 1.5 x t_{cyc}	—	—	D	ns
8	t_{ILIH}, t_{IHIL}	KBIPx pulse width • Asynchronous path[2] • Synchronous path[3]		 100 1.5 x t_{cyc}	—	—	D	ns

Table 19. Control Timing

#	Symbol	Parameter	Min	Typical[1]	Max	C	Unit
9	t_{Rise}, t_{Fall}	Port rise and fall time (load = 50 pF)[4], Low Drive					ns
		Slew rate control disabled (PTxSE = 0)	—	11	—	D	
		Slew rate control enabled (PTxSE = 1)	—	35	—	D	
		Slew rate control disabled (PTxSE = 0)	—	40	—	D	
		Slew rate control enabled (PTxSE = 1)	—	75	—	D	

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

3 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

4 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 105 °C.

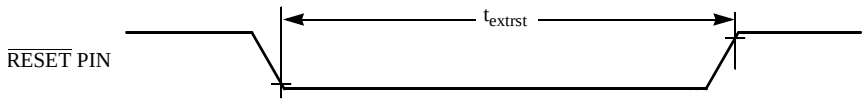


Figure 7. Reset Timing

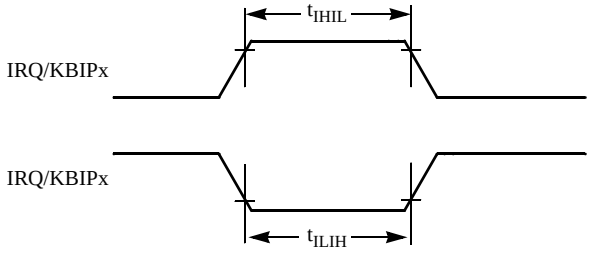


Figure 8. IRQ/KBIPx Timing

2.11.2 TPM Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 20. TPM Input Timing

#	C	Function	Symbol	Min	Max	Unit
1	—	External clock frequency	f_{TPMext}	dc	$f_{Bus}/4$	MHz
2	—	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

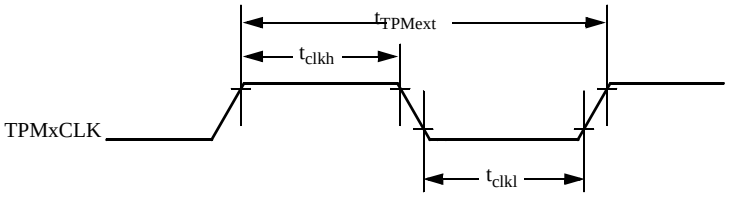


Figure 9. Timer External Clock

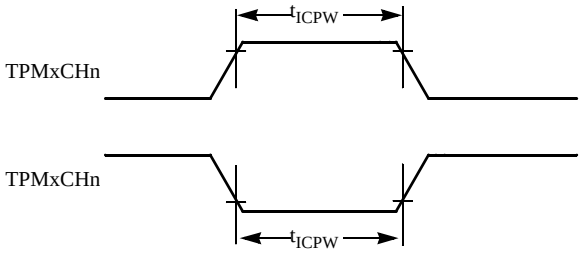
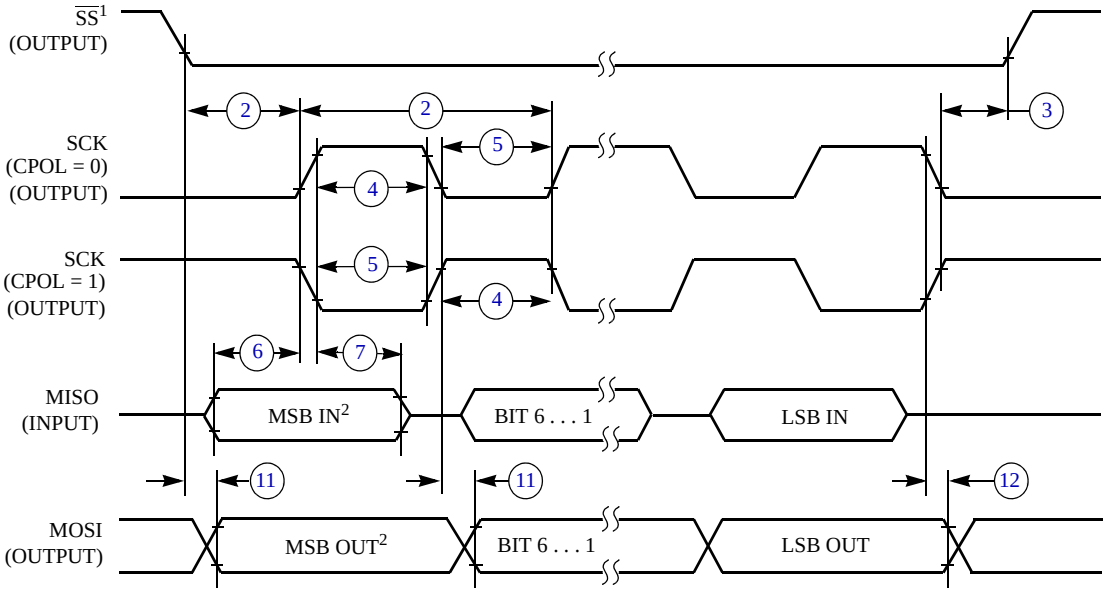
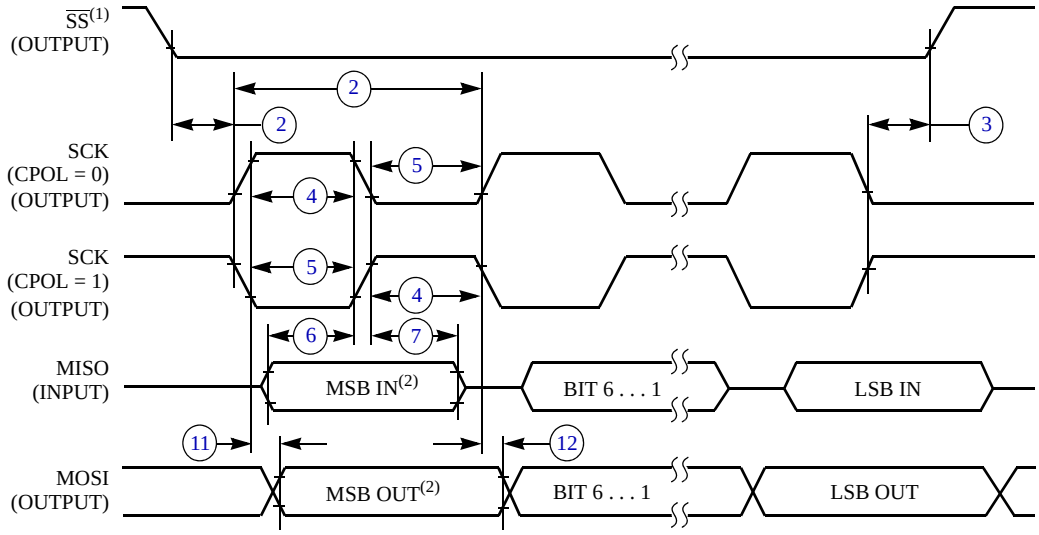


Figure 10. Timer Input Capture Pulse



NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 11. SPI Master Timing (CPHA = 0)



NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 12. SPI Master Timing (CPHA = 1)

2.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory chapter in the Reference Manual for this device (MC9S08JE128RM).

Table 22. Flash Characteristics

#	Characteristic	Symbol	Min	Typical	Max	Unit	C
1	Supply voltage for program/erase -40°C to 105°C	$V_{prog/erase}$	1.8	—	3.6	V	D
2	Supply voltage for read operation	V_{Read}	1.8	—	3.6	V	D
3	Internal FCLK frequency[1]	f_{FCLK}	150	—	200	kHz	D
4	Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	µs	D
5	Byte program time (random location)[2]	t_{prog}	9			t_{Fcyc}	P
6	Byte program time (burst mode)[2]	t_{Burst}	4			t_{Fcyc}	P
7	Page erase time[2]	t_{Page}	4000			t_{Fcyc}	P
8	Mass erase time[2]	t_{Mass}	20,000			t_{Fcyc}	P
9	Program/erase endurance[3] T_L to T_H = –40°C to + 105°C T = 25°C		10,000 —	— 100,000	— —	cycles	C
10	Data retention[4]	t_{D_ret}	15	100	—	years	C

1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 **Typical endurance for flash** was evaluated for this product family on the HC9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory*.

4 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.*

2.15 VREF Electrical Specifications

Table 24. VREF Electrical Specifications

Num	Characteristic	Symbol	Min	Max	Unit	C
1	Supply voltage	V_{DDA}	1.80	3.6	V	C
2	Temperature	T_A	–40	105	°C	C
3	Output Load Capacitance	C_L	—	100	nf	D
4	Maximum Load	—	—	10	mA	—
5	Voltage Reference Output with Factory Trim. V_{DD} = 3 V.	Vout	1.140	1.160	V	P
6	Temperature Drift (Vmin - Vmax across the full temperature range)	Tdrift	—	10 (TBD)	mV[1]	T
7	Aging Coefficient	Ac	—	TBD	ppm/year	C
8	Powered down Current (Off Mode, VREFEN=0, VRSTEN=0)	I	—	0.10	µA	C
9	Bandgap only (MODE_LV[1:0] = 00)	I	—	75	µA	T
10	Low-Power buffer (MODE_LV[1:0] = 01)	I	—	125	µA	T
11	Tight-Regulation buffer (MODE_LV[1:0] = 10)	I	—	1.1	mA	T
12	Load Regulation MODE_LV = 10	—	—	100	µV/mA	C
13	Line Regulation (Power Supply Rejection)	DC	—	TBD	mV	C
14		AC	TBD	—	dB	

[1] See typical chart below.

Table 25. VREF Limited Range Operating Requirements

#	Characteristic	Symbol	Min	Max	Unit	C	Notes
1	Temperature	T_A	0	50	°C	C	

Table 26. VREF Limited Range Operating Behaviors

#	Characteristic	Symbol	Min	Max	Unit	C	Notes
1	Voltage Reference Output with Factory Trim	Vout	TBD	TBD	µA	C	

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

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