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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CSIO, EBI/EMI, I ² C, LINbus, SD, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	120
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2c38h0agv2000a



(Top View)



- The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
20	-	-	-	P55	E	I
				SOT15_1 (SDA15_1)		
				RTO05_1 (PPG04_1)		
				TIOB10_2		
				MADATA21_0		
21	-	-	-	P56	E	I
				SCK15_1 (SCL15_1)		
				DTTIOX_1		
				TIOB0_1		
				MADATA22_0		
22	-	-	-	P57	E	I
				IC00_1		
				TIOB1_1		
				MADATA23_0		
23	18	15	F5	PAD	N	I
				SCK3_0 (SCL3_0)		
				TIOB9_0		
				BIN3_0		
				MADATA13_0		
24	19	16	F6	PAE	N	I
				ADTG_0		
				SOT3_0 (SDA3_0)		
				TIOB10_0		
				ZIN3_0		
				MADATA14_0		
25	20	17	G2	PAF	I	K
				SIN3_0		
				TIOB11_0		
				INT16_0		
				MADATA15_0		
26	-	-	-	P58	E	K
				SIN11_1		
				IC01_1		
				TIOB2_1		
				INT02_2		
				MADATA24_0		
27	-	-	-	P59	E	I
				SOT11_1 (SDA11_1)		
				IC02_1		
				TIOB3_1		
				MADATA25_0		
28	-	-	-	P5A	E	I
				SCK11_1 (SCL11_1)		
				IC03_1		
				TIOB4_1		
				MADATA26_0		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
42	32	27	J5	P36	L	K
				IC01_0		
				INT02_1		
				S_DATA3_0		
43	33	28	J4	P37	L	K
				IC00_0		
				INT03_1		
				S_DATA2_0		
44	34	29	J3	P38	E	I
				ADTG_2		
				DTTIOX_0		
				S_WP_0		
45	35	30	J2	P39	G	K
				SIN2_1		
				RTO00_0 (PPG00_0)		
				TIOA0_1		
				AIN3_1		
				INT16_1		
				S_CD_0		
				MAD24_0		
46	36	31	K1	P3A	G	K
				SOT2_1 (SDA2_1)		
				RTO01_0 (PPG00_0)		
				TIOA1_1		
				BIN3_1		
				INT17_1		
				MAD23_0		
47	37	32	K2	P3B	G	K
				SCK2_1 (SCL2_1)		
				RTO02_0 (PPG02_0)		
				TIOA2_1		
				ZIN3_1		
				INT18_1		
				MAD22_0		
				MNALE_0		
48	38	33	K3	P3C	G	K
				SIN13_0		
				RTO03_0 (PPG02_0)		
				TIOA3_1		
				INT19_1		
				MAD21_0		
				MNCLE_0		
49	39	34	K4	P3D	G	I
				SOT13_0 (SDA13_0)		
				RTO04_0 (PPG04_0)		
				TIOA4_1		
				MAD20_0		
				MNWEX_0		

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Base Timer 7	TIOA7_0	Base Timer ch 7 TIOA pin	181	149	119	F9
	TIOA7_1		87	72	-	N9
	TIOA7_2		202	-	-	-
	TIOB7_0	Base Timer ch 7 TIOB pin	180	148	118	E9
	TIOB7_1		88	73	-	P9
	TIOB7_2		201	-	-	-
Base Timer 8	TIOA8_0	Base Timer ch 8 TIOA pin	2	2	2	B2
	TIOA8_1		142	116	92	G10
	TIOA8_2		10	10	-	E2
	TIOB8_0	Base Timer ch 8 TIOB pin	18	17	14	F4
	TIOB8_1		143	117	93	G9
	TIOB8_2		11	11	-	E3
Base Timer 9	TIOA9_0	Base Timer ch 9 TIOA pin	3	3	3	C2
	TIOA9_1		126	102	-	J10
	TIOA9_2		12	12	-	E4
	TIOB9_0	Base Timer ch 9 TIOB pin	23	18	15	F5
	TIOB9_1		127	103	-	J9
	TIOB9_2		13	-	-	-
Base Timer 10	TIOA10_0	Base Timer ch 10 TIOA pin	4	4	4	C3
	TIOA10_1		128	104	-	H10
	TIOA10_2		19	-	-	-
	TIOB10_0	Base Timer ch 10 TIOB pin	24	19	16	F6
	TIOB10_1		129	105	-	J14
	TIOB10_2		20	-	-	-
Base Timer 11	TIOA11_0	Base Timer ch 11 TIOA pin	5	5	5	D5
	TIOA11_1		138	112	-	G13
	TIOA11_2		33	-	-	-
	TIOB11_0	Base Timer ch 11 TIOB pin	25	20	17	G2
	TIOB11_1		139	113	-	F14
	TIOB11_2		51	41	-	L2
Base Timer 12	TIOA12_0	Base Timer ch 12 TIOA pin	6	6	6	D2
	TIOA12_1		140	114	-	G12
	TIOA12_2		52	42	-	L3
	TIOB12_0	Base Timer ch 12 TIOB pin	30	21	18	G3
	TIOB12_1		141	115	-	G11
	TIOB12_2		53	43	-	M2

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Base Timer 13	TIOA13_0	Base Timer ch 13 TIOA pin	7	7	7	D1
	TIOA13_1		154	124	100	E12
	TIOA13_2		34	24	-	G6
	TIOB13_0	Base Timer ch 13 TIOB pin	31	22	19	G4
	TIOB13_1		155	125	101	E13
	TIOB13_2		35	25	-	H4
Base Timer 14	TIOA14_0	Base Timer ch 14 TIOA pin	183	151	121	D8
	TIOA14_1		89	74	-	M9
	TIOA14_2		204	-	-	-
	TIOB14_0	Base Timer ch 14 TIOB pin	182	150	120	C8
	TIOB14_1		90	75	-	L9
	TIOB14_2		203	-	-	-
Base Timer 15	TIOA15_0	Base Timer ch 15 TIOA pin	187	155	125	B7
	TIOA15_1		78	63	-	K5
	TIOA15_2		206	-	-	-
	TIOB15_0	Base timer ch 15 TIOB pin	186	154	124	F8
	TIOB15_1		79	64	-	K6
	TIOB15_2		205	-	-	-
Debugger	SWCLK	Serial wire debug interface clock input pin	165	135	111	A12
	SWDIO	Serial wire debug interface data input/output pin	167	137	113	B12
	SWO	Serial wire viewer output pin	168	138	114	B11
	TCK	JTAG test clock input pin	165	135	111	A12
	TDI	JTAG test data input pin	166	136	112	C12
	TDO	JTAG debug data output pin	168	138	114	B11
	TMS	JTAG test mode state input/output pin	167	137	113	B12
	TRACECLK	Trace CLK output pin of ETM/HTM	131	107	87	H12
	TRACED0	Trace data output pin of ETM/ Trace data output pin of HTM	132	108	88	H14
	TRACED1		133	109	89	G14
	TRACED2		134	110	90	H13
	TRACED3		135	111	91	H11
	TRACED4	Trace data output pin of HTM	138	112	-	G13
	TRACED5		139	113	-	F14
	TRACED6		140	114	-	G12
	TRACED7		141	115	-	G11
	TRACED8		119	-	-	-
	TRACED9		120	-	-	-
	TRACED10		121	-	-	-
	TRACED11		122	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
External interrupt	INT06_0	External interrupt request 06 input pin	80	65	55	L6
	INT06_1		87	72	-	N9
	INT06_2		103	-	-	-
	INT07_0	External interrupt request 07 input pin	82	67	57	L8
	INT07_1		88	73	-	P9
	INT07_2		102	-	-	-
	INT08_0	External interrupt request 08 input pin	114	94	78	L11
	INT08_1		127	103	-	J9
	INT08_2		119	-	-	-
	INT09_0	External interrupt request 09 input pin	123	99	83	J13
	INT09_1		128	104	-	H10
	INT09_2		120	-	-	-
	INT10_0	External interrupt request 10 input pin	130	106	86	H9
	INT10_1		138	112	-	G13
	INT10_2		149	-	-	-
	INT11_0	External interrupt request 11 input pin	133	109	89	G14
	INT11_1		139	113	-	F14
	INT11_2		151	-	-	-
	INT12_0	External interrupt request 12 input pin	194	162	132	E7
	INT12_1		169	139	-	C11
	INT12_2		175	-	-	-
	INT13_0	External interrupt request 13 input pin	184	152	122	E8
	INT13_1		170	140	-	D11
	INT13_2		176	-	-	-
	INT14_0	External interrupt request 14 input pin	192	160	130	A6
	INT14_1		171	141	-	B10
	INT14_2		201	-	-	-
	INT15_0	External interrupt request 15 input pin	193	161	131	D7
	INT15_1		172	142	-	C10
	INT15_2		206	-	-	-
	INT16_0	External interrupt request 16 input pin	25	20	17	G2
	INT16_1		45	35	30	J2
	INT17_0	External interrupt request 17 input pin	30	21	18	G3
	INT17_1		46	36	31	K1
	INT18_0	External interrupt request 18 input pin	31	22	19	G4
	INT18_1		47	37	32	K2
	INT19_0	External interrupt request 19 input pin	36	26	21	H2
	INT19_1		48	38	33	K3

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	P00	General-purpose I/O port 0	164	134	110	B13
	P01		165	135	111	A12
	P02		166	136	112	C12
	P03		167	137	113	B12
	P04		168	138	114	B11
	P08		30	21	18	G3
	P09		31	22	19	G4
	P0A		32	23	20	G5
	P10	General-purpose I/O port 1	114	94	78	L11
	P11		115	95	79	K13
	P12		116	96	80	K12
	P13		117	97	81	K14
	P14		118	98	82	K11
	P15		123	99	83	J13
	P16		124	100	84	J12
	P17		125	101	85	J11
	P18		130	106	86	H9
	P19		131	107	87	H12
	P1A		132	108	88	H14
	P1B		133	109	89	G14
	P1C		134	110	90	H13
	P1D		135	111	91	H11
	P1E		142	116	92	G10
	P1F		143	117	93	G9
	P20	General-purpose I/O port 2	158	128	104	C13
	P21		157	127	103	D13
	P22		156	126	102	D12
	P23		155	125	101	E13
	P24		154	124	100	E12
	P25		153	123	99	E11
	P26		152	122	98	E10
	P27		147	121	97	F13
	P28		146	120	96	F12
	P29		145	119	95	F11
	P2A		144	118	94	F10

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	PA0	General-purpose I/O port A	2	2	2	B2
	PA1		3	3	3	C2
	PA2		4	4	4	C3
	PA3		5	5	5	D5
	PA4		6	6	6	D2
	PA5		7	7	7	D1
	PA6		8	8	8	D3
	PA7		9	9	9	D4
	PA8		14	13	10	E5
	PA9		15	14	11	F1
	PAA		16	15	12	F2
	PAB		17	16	13	F3
	PAC		18	17	14	F4
	PAD		23	18	15	F5
	PAE		24	19	16	F6
	PAF		25	20	17	G2
	PB0	General-purpose I/O port B	126	102	-	J10
	PB1		127	103	-	J9
	PB2		128	104	-	H10
	PB3		129	105	-	J14
	PB4		138	112	-	G13
	PB5		139	113	-	F14
	PB6		140	114	-	G12
	PB7		141	115	-	G11
	PB8		119	-	-	-
	PB9		120	-	-	-
	PBA		121	-	-	-
	PBB		122	-	-	-
	PBC		148	-	-	-
	PBD		149	-	-	-
	PBE		150	-	-	-
	PBF		151	-	-	-

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent this, do the following:

1. Avoid exposure to rapid temperature changes, which can cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
3. When Dry Packages are opened, it is recommended to have humidity between 40% and 70%.
4. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in these aluminum laminate bags for storage.
5. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

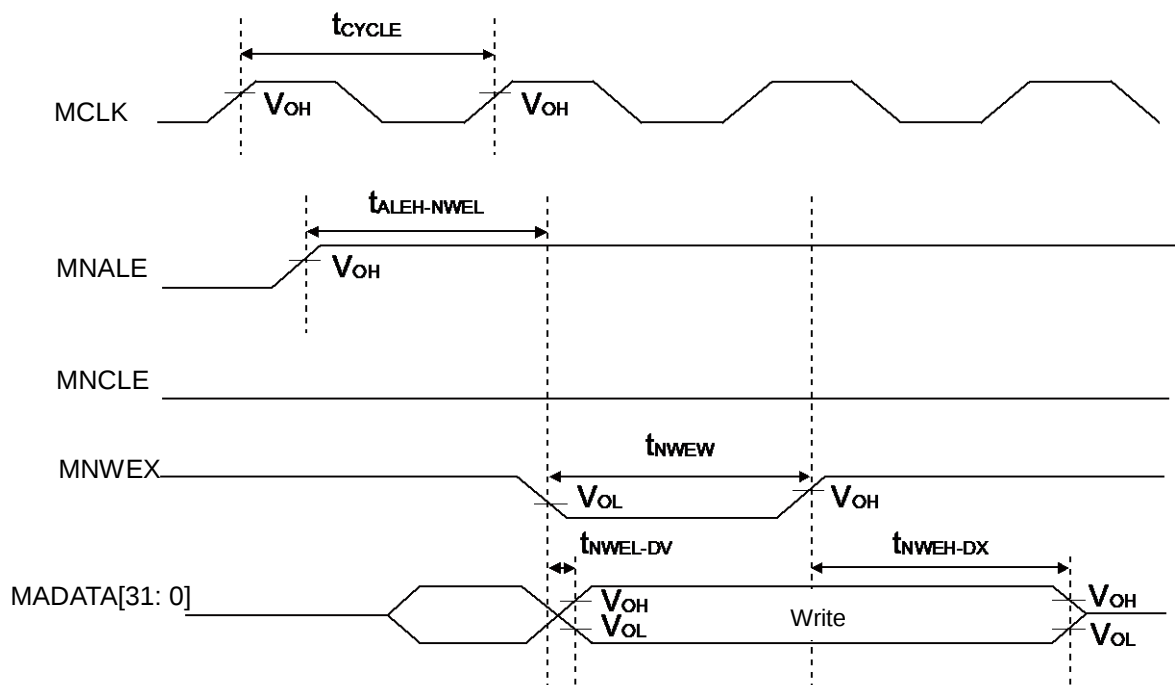
Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

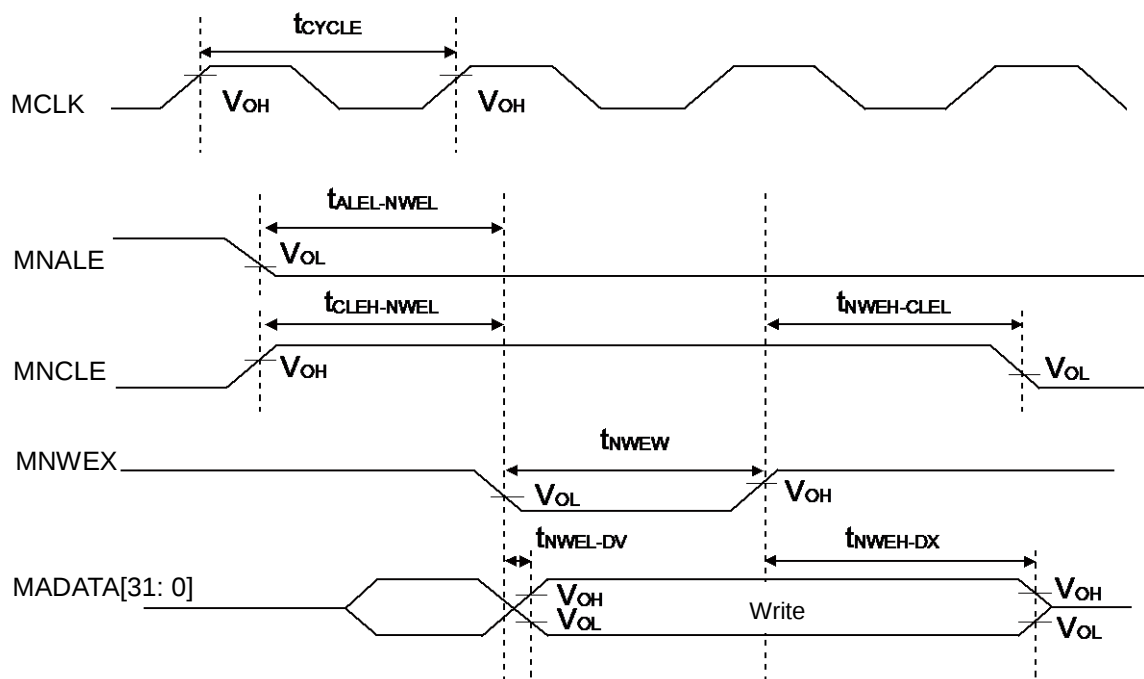
1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons, and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ). Wearing of conductive clothing and shoes, and the use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of Styrofoam or other highly static-prone materials for storage of completed board assemblies.

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC Mode or Deep Standby Stop mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
J	Analog output selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled	Maintain previous state	*2	*3	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	External interrupt enable selected					Maintain previous state	Maintain previous state			
	Resource other than above selected						Hi-Z/internal input fixed at 0			
	GPIO selected									
K	External interrupt enable selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled			Hi-Z/internal input fixed at 0			
	GPIO selected									
L	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	GPIO selected									

NAND Flash Address Write



NAND Flash Command Write

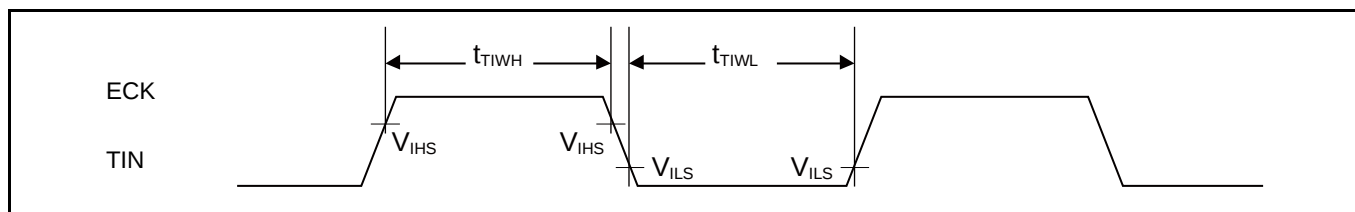


12.4.11 Base Timer Input Timing

Timer Input Timing

($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$)

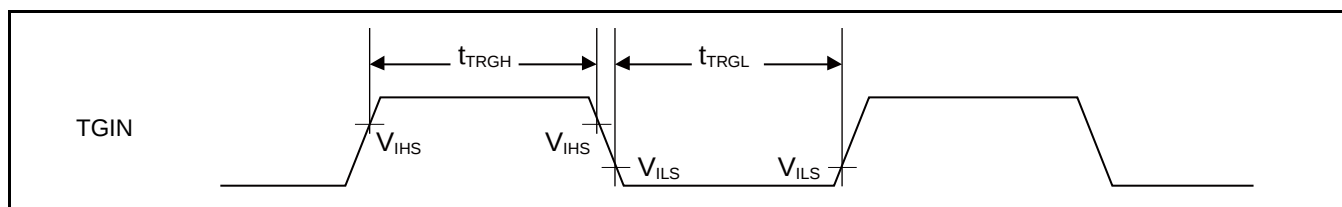
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH} , t_{TIWL}	TIOAn/TIOBn (when using as ECK, TIN)	-	$2t_{CYCP}$	-	ns	



Trigger Input Timing

($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH} , t_{TRGL}	TIOAn/TIOBn (when using as TGIN)	-	$2t_{CYCP}$	-	ns	



Note:

- t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the base timer is connected, see 8. Block Diagram in this data sheet.

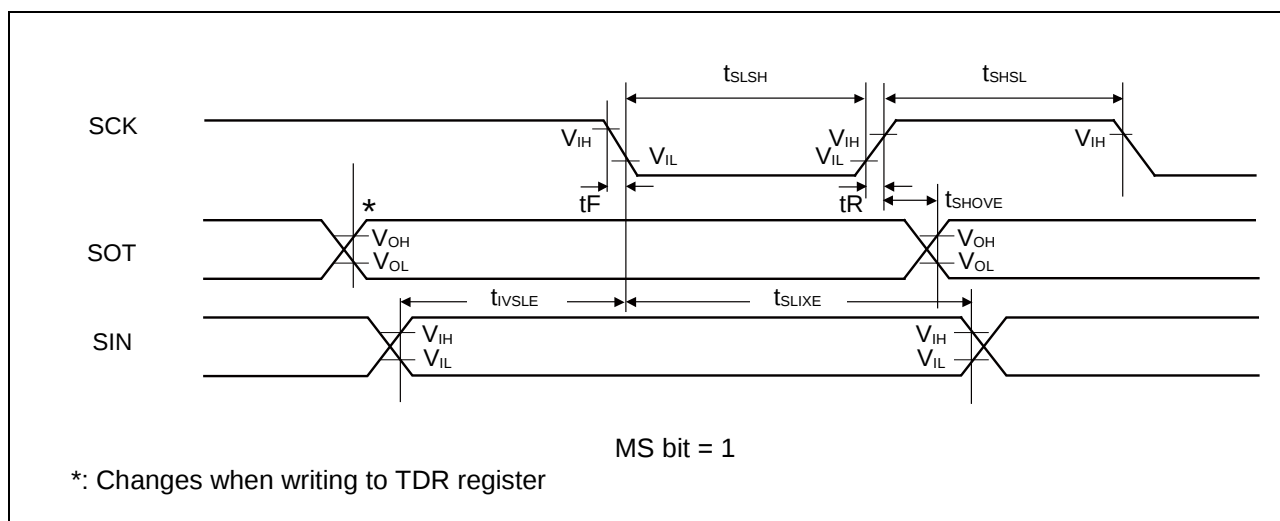
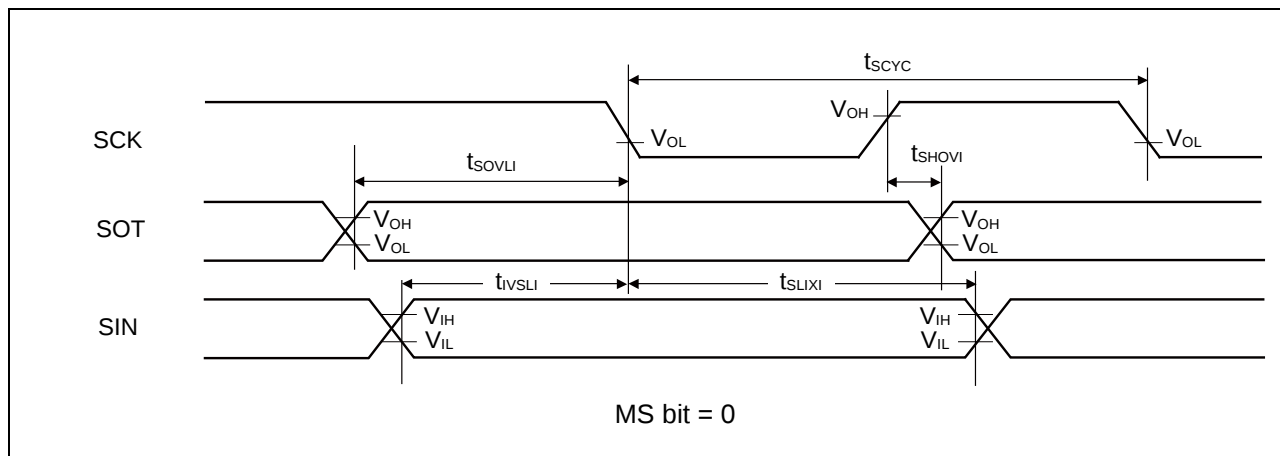
Synchronous Serial (SPI = 0, SCINV = 1)

 (V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V _{CC} < 4.5 V		V _{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t _{SCYC}	SCKx	Internal shift clock operation	4t _{CYCP}	-	4t _{CYCP}	-	ns
SCK↑→SOT delay time	t _{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↓ setup time	t _{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK↓→SIN hold time	t _{SLIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t _{LSLH}	SCKx		2t _{CYCP} - 10	-	2t _{CYCP} - 10	-	ns
Serial clock H pulse width	t _{SHSL}	SCKx	External shift clock operation	t _{CYCP} + 10	-	t _{CYCP} + 10	-	ns
SCK↑→SOT delay time	t _{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↓ setup time	t _{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK↓→SIN hold time	t _{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK fall time	t _F	SCKx		-	5	-	5	ns
SCK rise time	t _R	SCKx		-	5	-	5	ns

Notes:

- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- These characteristics only guarantee the same relocate port number; for example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance C_L = 30 pF.



When Using Synchronous Serial Chip Select (SCINV = 1, CSLVL = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V _{CC} < 4.5 V		V _{CC} ≥ 4.5 V		Units
			Min	Max	Min	Max	
SCS ↑ → SCK ↑ setup time	t _{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK ↓ → SCS ↓ hold time	t _{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t _{CSDI}		(*3)-50 +5t _{CYCP}	(*3)+50 +5t _{CYCP}	(*3)-50 +5t _{CYCP}	(*3)+50 +5t _{CYCP}	ns
SCS ↑ → SCK ↑ setup time	t _{CSSE}	External shift clock operation	3t _{CYCP} +30	-	3t _{CYCP} +30	-	ns
SCK ↓ → SCS ↓ hold time	t _{CSHE}		0	-	0	-	ns
SCS deselect time	t _{CSDE}		3t _{CYCP} +30	-	3t _{CYCP} +30	-	ns
SCS ↑ → SOT delay time	t _{DSE}		-	40	-	40	ns
SCS ↓ → SOT delay time	t _{DEE}		0	-	0	-	ns

(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).
- When the external load capacitance C_L = 30 pF.

When Using High-Speed Synchronous Serial Chip Select (SCINV = 1, CSLVL = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V _{CC} < 4.5 V		V _{CC} ≥ 4.5 V		Unit
			Min	Min	Min	Max	
SCS↓→SCK↓ setup time	t _{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↑→SCS↑ hold time	t _{CSHI}		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t _{CSDI}		(*3)-20 +5t _{CYCP}	(*3)+20 +5t _{CYCP}	(*3)-20 +5t _{CYCP}	(*3)+20 +5t _{CYCP}	ns
SCS↓→SCK↑ setup time	t _{CSSE}	External shift clock operation	3t _{CYCP} +15	-	3t _{CYCP} +15	-	ns
SCK↑→SCS↑ hold time	t _{CSHE}		0	-	0	-	ns
SCS deselect time	t _{CSDE}		3t _{CYCP} +15	-	3t _{CYCP} +15	-	ns
SCS↓→SOT delay time	t _{DSE}		-	25	-	25	ns
SCS↑→SOT delay time	t _{DEE}		0	-	0	-	ns

(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).
- When the external load capacitance C_L = 30 pF.

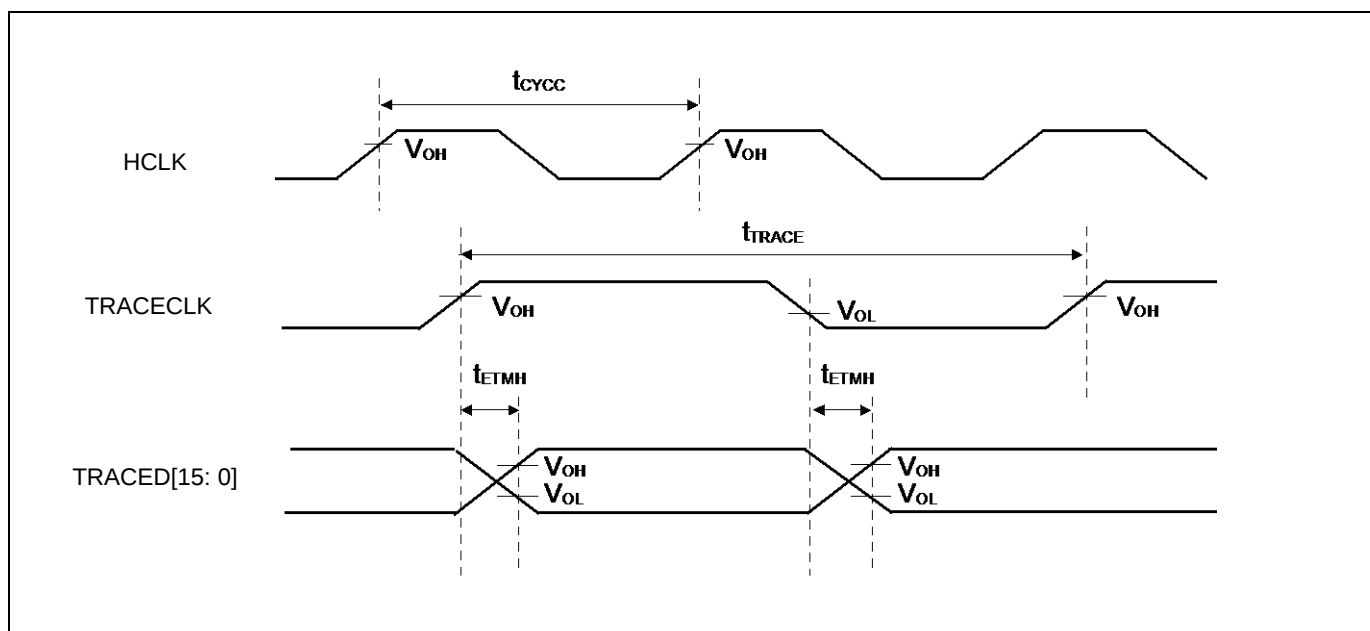
12.4.17 ETM/ HTM Timing

($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Data hold	t_{ETMH}	TRACECLK, TRACED[15: 0]	$V_{CC} \geq 4.5 V$	2	9	ns	
			$V_{CC} < 4.5 V$	2	15		
TRACECLK frequency	$1/t_{TRACE}$	TRACECLK	$V_{CC} \geq 4.5 V$		50	MHz	
			$V_{CC} < 4.5 V$		32	MHz	
TRACECLK clock cycle	t_{TRACE}	TRACECLK	$V_{CC} \geq 4.5 V$	20	-	ns	
			$V_{CC} < 4.5 V$	31.25	-	ns	

Note:

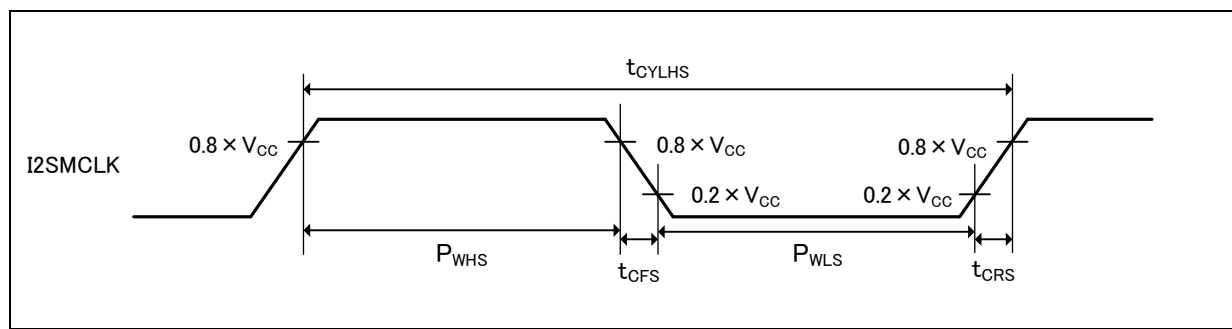
- When the external load capacitance $C_L = 30 pF$.



I2SMCLK Input Characteristics

($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{CHS}	I2SMCK	-	-	25	MHz	
Input clock cycle	t_{CYLHS}	-	-	40	-	ns	
Input clock pulse width	-	-	P_{WHS}/t_{CYLHS} P_{WLS}/t_{CYLHS}	45	55	%	When using external clock
Input clock rise time and fall time	t_{CFS} t_{CRS}	-	-	-	5	ns	When using external clock



I2SMCLK Output Characteristics

($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output frequency	f_{CHS}	I2SMCK	-	-	12.288	MHz	

