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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CSIO, EBI/EMI, I ² C, LINbus, SD, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	120
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2c39h0agv2000a

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Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
158	128	104	C13	P20	I	F
				NMIX		
				WKUP0		
159	129	105	E14	USBVCC1	-	-
160	130	106	D14	P82	H	R
				UDM1		
161	131	107	C14	P83	H	R
				UDP1		
162	132	108	B14	VSS	-	-
163	133	109	A13	VCC	-	-
164	134	110	B13	P00	E	G
				TRSTX		
165	135	111	A12	P01	E	G
				TCK		
				SWCLK		
166	136	112	C12	P02	E	G
				TDI		
167	137	113	B12	P03	E	G
				TMS		
				SWDIO		
168	138	114	B11	P04	E	G
				TDO		
				SWO		
169	139	-	C11	P90	S	K
				INT12_1		
				Q_IO3_0		
170	140	-	D11	P91	S	K
				SIN5_1		
				INT13_1		
171	141	-	B10	Q_IO2_0	S	K
				P92		
				SOT5_1 (SDA5_1)		
				INT14_1		
172	142	-	C10	Q_IO1_0	S	K
				P93		
				SCK5_1 (SCL5_1)		
				INT15_1		
173	143	-	D10	Q_IO0_0	S	I
				P94		
				CTS5_1		
174	144	-	B9	Q_SCK_0	S	I
				P95		
				RTS5_1		
175	-	-	-	Q_CS0_0	S	K
				P96		
				INT12_2		
176	-	-	-	Q_CS1_0	S	K
				P97		
				INT13_2		
177	145	115	C9	Q_CS2_0	K	V
				PC0		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
178	146	116	B8	PC1	K	V
				TIOB6_0		
179	147	117	D9	PC2	K	V
				TIOA6_0		
180	148	118	E9	PC3	K	V
				TIOB7_0		
181	149	119	F9	PC4	K	V
				TIOA7_0		
182	150	120	C8	PC5	K	V
				TIOB14_0		
183	151	121	D8	PC6	K	V
				TIOA14_0		
184	152	122	E8	PC7	E	W
				INT13_0		
				CROUT_1		
185	153	123	A10	PC8	K	V
186	154	124	F8	PC9	K	V
				TIOB15_0		
187	155	125	B7	PCA	K	V
				TIOA15_0		
188	156	126	A9	VCC	-	-
189	157	127	A8	VSS	-	-
190	158	128	A7	PCB	L	W
				INT28_0		
191	159	129	C7	PCC	K	V
192	160	130	A6	PCD	L	W
				SOT4_1 (SDA4_1)		
				INT14_0		
193	161	131	D7	PCE	L	W
				SIN4_1		
				INT15_0		
194	162	132	E7	PCF	L	W
				RTS4_1		
				INT12_0		
195	163	133	F7	PD0	L	W
				INT30_1		
196	164	134	B6	PD1	L	W
				INT31_1		
197	165	135	C6	PD2	L	V
				CTS4_1		
				FRCK2_1		
198	166	136	D6	P6E	E	W
				ADTG_5		
				SCK4_1 (SCL4_1)		
				IC23_1		
				INT29_0		

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Base Timer 13	TIOA13_0	Base Timer ch 13 TIOA pin	7	7	7	D1
	TIOA13_1		154	124	100	E12
	TIOA13_2		34	24	-	G6
	TIOB13_0	Base Timer ch 13 TIOB pin	31	22	19	G4
	TIOB13_1		155	125	101	E13
	TIOB13_2		35	25	-	H4
Base Timer 14	TIOA14_0	Base Timer ch 14 TIOA pin	183	151	121	D8
	TIOA14_1		89	74	-	M9
	TIOA14_2		204	-	-	-
	TIOB14_0	Base Timer ch 14 TIOB pin	182	150	120	C8
	TIOB14_1		90	75	-	L9
	TIOB14_2		203	-	-	-
Base Timer 15	TIOA15_0	Base Timer ch 15 TIOA pin	187	155	125	B7
	TIOA15_1		78	63	-	K5
	TIOA15_2		206	-	-	-
	TIOB15_0	Base timer ch 15 TIOB pin	186	154	124	F8
	TIOB15_1		79	64	-	K6
	TIOB15_2		205	-	-	-
Debugger	SWCLK	Serial wire debug interface clock input pin	165	135	111	A12
	SWDIO	Serial wire debug interface data input/output pin	167	137	113	B12
	SWO	Serial wire viewer output pin	168	138	114	B11
	TCK	JTAG test clock input pin	165	135	111	A12
	TDI	JTAG test data input pin	166	136	112	C12
	TDO	JTAG debug data output pin	168	138	114	B11
	TMS	JTAG test mode state input/output pin	167	137	113	B12
	TRACECLK	Trace CLK output pin of ETM/HTM	131	107	87	H12
	TRACED0	Trace data output pin of ETM/ Trace data output pin of HTM	132	108	88	H14
	TRACED1		133	109	89	G14
	TRACED2		134	110	90	H13
	TRACED3		135	111	91	H11
	TRACED4	Trace data output pin of HTM	138	112	-	G13
	TRACED5		139	113	-	F14
	TRACED6		140	114	-	G12
	TRACED7		141	115	-	G11
	TRACED8		119	-	-	-
	TRACED9		120	-	-	-
	TRACED10		121	-	-	-
	TRACED11		122	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	P30	General-purpose I/O port 3	34	24	-	G6
	P31		35	25	-	H4
	P32		36	26	21	H2
	P33		37	27	22	J1
	P34		38	28	23	H3
	P35		41	31	26	H6
	P36		42	32	27	J5
	P37		43	33	28	J4
	P38		44	34	29	J3
	P39		45	35	30	J2
	P3A		46	36	31	K1
	P3B		47	37	32	K2
	P3C		48	38	33	K3
	P3D		49	39	34	K4
	P3E		50	40	35	L1
	P40	General-purpose I/O port 4	56	46	38	N2
	P41		57	47	39	N3
	P42		58	48	40	M3
	P43		59	49	41	L4
	P44		60	50	42	M4
	P45		61	51	43	N4
	P46		73	58	50	P5
	P47		74	59	51	P6
	P48		76	61	53	N6
	P49		77	62	54	M6
	P4A		65	-	-	-
	P4B		66	-	-	-
	P4C		67	-	-	-
	P4D		68	-	-	-
	P4E		69	-	-	-

Notes on Power-on

Turn power on/off in the following order or at the same time. The device operates normally after all power on.

VBAT only Power-on is possible when VBAT and VCC turns Power-on and Hibernation control is setting and then VCC turns Power-off. About Hibernation control, see Chapter 7-2: VBAT Domain(B) in FM4 Family Peripheral Manual Main Part(002-04856).

Turning on: VBAT → VCC → USBVCC0
VBAT → VCC → USBVCC1
VCC → AVCC → AVRH
Turning off: AVRH → AVCC → VCC
USBVCC1 → VCC → VBAT
USBVCC0 → VCC → VBAT

Serial Communication

There is a possibility of receiving incorrect data as a result of noise or other issues introduced by the serial communication. Take care to design the printed circuit board to minimize noise.

Consider the case of introducing error as a result of noise, perform error detection such as by applying a checksum of data at the end. If an error is detected, retransmit the data.

Differences in Characteristics within the Product Line

The electric characteristics including power consumption, ESD, latch-up, noise, and oscillation differ among members of the product line because chip layout and memory structures are not the same; for example, different sizes, flash versus ROM, etc. If you are switching to a different product of the same series, please make sure to evaluate the electric characteristics.

Pull-Up Function of 5 V Tolerant I/O

Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5 V tolerant I/O.

Pin Doubled as Debug Function

The pin doubled as TDO/TMS/TDI/TCK/TRSTX, SWO/SWDIO/SWCLK should be used as output only. Do not use as input.

Calculation Method of Power Dissipation (Pd)

The power dissipation is shown in the following formula.

$$P_d = V_{CC} \times I_{CC} + \sum (I_{OL} \times V_{OL}) + \sum ((V_{CC} - V_{OH}) \times (-I_{OH}))$$

I_{OL} : L level output current

I_{OH} : H level output current

V_{OL} : L level output voltage

V_{OH} : H level output voltage

I_{CC} is the current drawn by the device.

It can be analyzed as follows.

$$I_{CC} = I_{CC}(\text{INT}) + \sum I_{CC}(\text{IO})$$

$I_{CC}(\text{INT})$: Current drawn by internal logic and memory, etc. through the regulator

$\sum I_{CC}(\text{IO})$: Sum of current (I/O switching current) drawn by the output pin

For $I_{CC}(\text{INT})$, it can be anticipated by (1) Current Rating in 12.3. DC Characteristics (This rating value does not include $I_{CC}(\text{IO})$ for a value at pin fixed).

For $I_{CC}(\text{IO})$, it depends on system used by customers.

The calculation formula is shown below.

$$I_{CC}(\text{IO}) = (C_{\text{INT}} + C_{\text{EXT}}) \times V_{CC} \times f_{\text{SW}}$$

C_{INT} : Pin internal load capacitance
 C_{EXT} : External load capacitance of output pin
 f_{SW} : Pin switching frequency

Parameter	Symbol	Conditions	Capacitance Value
Pin internal load capacitance	C_{INT}	4 mA type	1.93 pF
		8 mA type	3.45 pF
		12 mA type	3.42 pF

Calculate $I_{CC}(\text{Max})$ as follows when the power dissipation can be evaluated by yourself:

Measure current value $I_{CC}(\text{Typ})$ at normal temperature (+25°C).

Add maximum leakage current value $I_{CC}(\text{leak_max})$ at operating on a value in (1).

$$I_{CC}(\text{Max}) = I_{CC}(\text{Typ}) + I_{CC}(\text{leak_max})$$

Parameter	Symbol	Conditions	Current Value
Maximum leakage current at operating	$I_{CC}(\text{leak_max})$	$T_J = +125^\circ\text{C}$	79.2 mA
		$T_J = +105^\circ\text{C}$	39.4 mA
		$T_J = +85^\circ\text{C}$	26.5 mA

Current Explanation Diagram

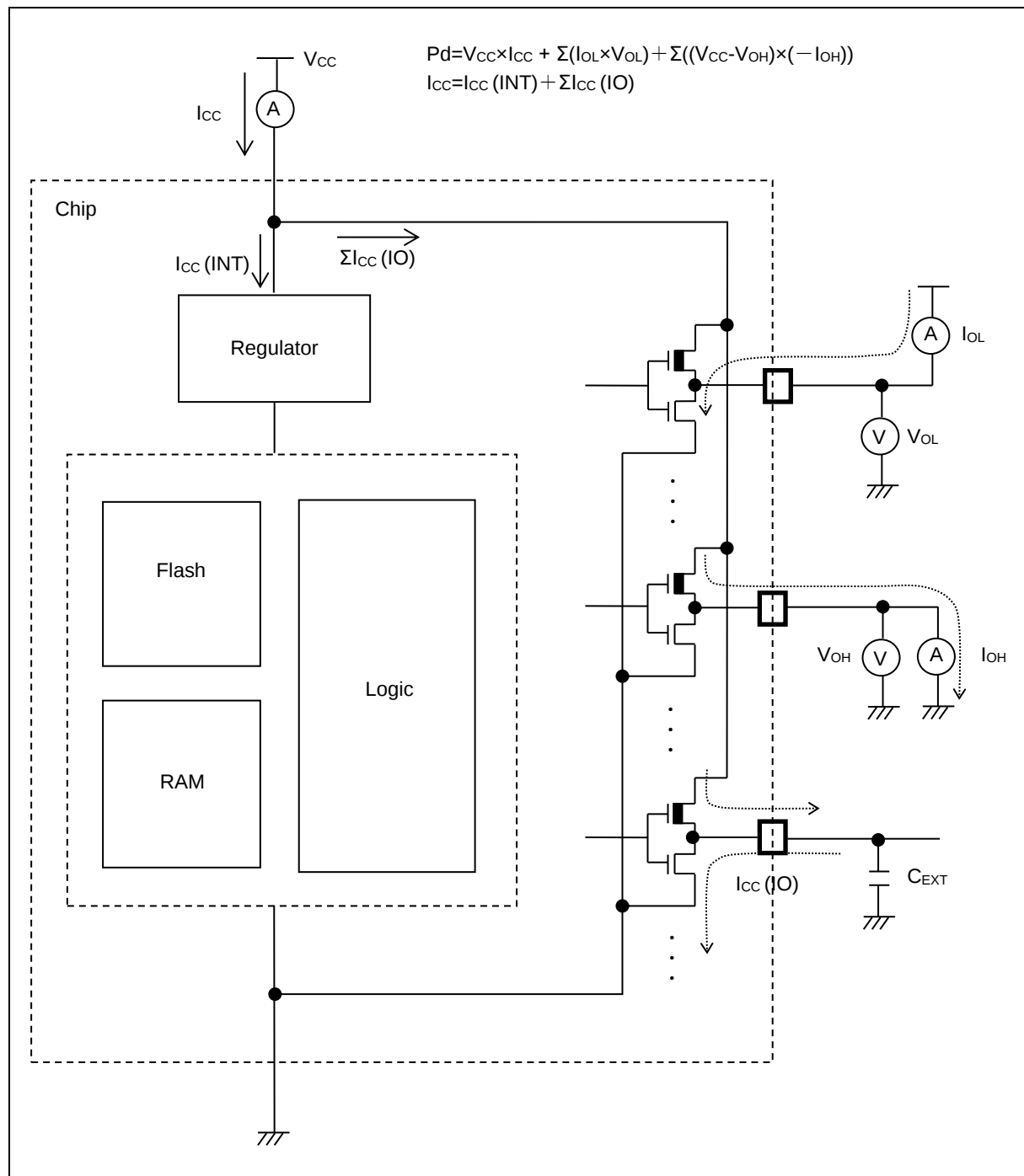


Table 12-8 Typical and Maximum Current Consumption in Stop Mode, Timer Mode and RTC Mode

Parameter	Symbol	Pin Name	Conditions	Frequency	Value		Unit	Remarks	
					Typ*1	Max*2			
Power supply current	I _{CCH}	V _{CC}	Stop mode	-	0.56	3.01	mA	*3, *4 T _A = +25°C	
					-	27.03	mA	*3, *4 T _A = +85°C	
					-	39.92	mA	*3, *4 T _A = +105°C	
	I _{CCT}		Timer mode*5 (main oscillation)	4 MHz	1.40	3.85	mA	*3, *4 T _A = +25°C	
					-	27.87	mA	*3, *4 T _A = +85°C	
					-	40.76	mA	*3, *4 T _A = +105°C	
			Timer mode (built-in High-speed CR)	4 MHz	0.95	3.40	mA	*3, *4 T _A = +25°C	
					-	27.42	mA	*3, *4 T _A = +85°C	
					-	40.31	mA	*3, *4 T _A = +105°C	
			Timer mode*6 (sub oscillation)	32 kHz	0.57	3.02	mA	*3, *4 T _A = +25°C	
					-	27.04	mA	*3, *4 T _A = +85°C	
					-	39.93	mA	*3, *4 T _A = +105°C	
			Timer mode (built-in Low-speed CR)	100 kHz	0.58	3.03	mA	*3, *4 T _A = +25°C	
					-	27.05	mA	*3, *4 T _A = +85°C	
					-	39.94	mA	*3, *4 T _A = +105°C	
			I _{CCR}	RTC mode*6 (sub oscillation)	32 kHz	0.57	3.02	mA	*3, *4 T _A = +25°C
						-	27.04	mA	*3, *4 T _A = +85°C
						-	39.93	mA	*3, *4 T _A = +105°C

*1: V_{CC} = 3.3V

*2: V_{CC} = 5.5V

*3: When all ports are fixed

*4: When LVD is off

*5: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

*6: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)

12.4.4 Operating Conditions of Main PLL (in the Case of Using Main Clock for Input Clock of PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time* ¹ (lock up time)	t _{LOCK}	100	-	-	μs	
PLL input clock frequency	f _{PLLI}	4	-	16	MHz	
PLL multiplication rate	-	13	-	100	multiplier	
PLL macro oscillation clock frequency	f _{PLLO}	200	-	400	MHz	
Main PLL clock frequency* ²	f _{CLKPLL}	-	-	200	MHz	

*1: Time from when the PLL starts operating until the oscillation stabilizes

*2: For more information about Main PLL clock (CLKPLL), see Chapter 2-1: Clock in FM4 Family Peripheral Manual Main Part (002-04856).

12.4.5 Operating Conditions of USB PLL · I²S PLL (in the Case of Using Main Clock for Input Clock of PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time* ¹ (lock up time)	t _{LOCK}	100	-	-	μs	
PLL input clock frequency	f _{PLLI}	4	-	16	MHz	
PLL multiplication rate	-	13	-	100	multiplier	
PLL macro oscillation clock frequency	f _{PLLO}	200	-	400	MHz	USB
				384	MHz	I ² S
USB clock frequency * ²	f _{CLKPLL}	-	-	50	MHz	After the M frequency division
I ² S clock frequency * ³	f _{CLKPLL}	-	-	12.288	MHz	After the M frequency division

*1: Time from when the PLL starts operating until the oscillation stabilizes

*2: For more information about USB/Ethernet clock, see Chapter 2-2: USB/Ethernet Clock Generation in FM4 Family Peripheral Manual Communication Macro Part (002-04862).

*3: For more information about I²S clock, see Chapter 7-1: I²S Clock Generation in FM4 Family Peripheral Manual Communication Macro Part (002-04862).

SDRAM Mode

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Value	Unit		Unit	Remarks
				Min	Max		
Output frequency	t _{CYCSD}	MSDCLK	-	-	50	MHz	
Address delay time	t _{AOSD}	MSDCLK, MAD[15: 0]	-	2	12	ns	
MSDCLK ↑ → Data output delay time	t _{DOSD}	MSDCLK, MADATA[31: 0]	-	2	12	ns	
MSDCLK ↑ → Data output Hi-Z time	t _{DOZSD}	MSDCLK, MADATA[31: 0]	-	2	19.5	ns	
MDQM[3: 0] delay time	t _{WROSD}	MSDCLK, MDQM[1: 0]	-	1	12	ns	
MCSX delay time	t _{MCSSD}	MSDCLK, MCSX8	-	2	12	ns	
MRASX delay time	t _{RASSD}	MSDCLK, MRASX	-	2	12	ns	
MCASX delay time	t _{CASSD}	MSDCLK, MCASX	-	2	12	ns	
MSDWEX delay time	t _{WESD}	MSDCLK, MSDWEX	-	2	12	ns	
MSDCKE delay time	t _{CKESD}	MSDCLK, MSDCKE	-	2	12	ns	
Data set up time	t _{DSSD}	MSDCLK, MADATA[31: 0]	-	19	-	ns	
Data hold time	t _{DHSD}	MSDCLK, MADATA[31: 0]	-	0	-	ns	

Note:

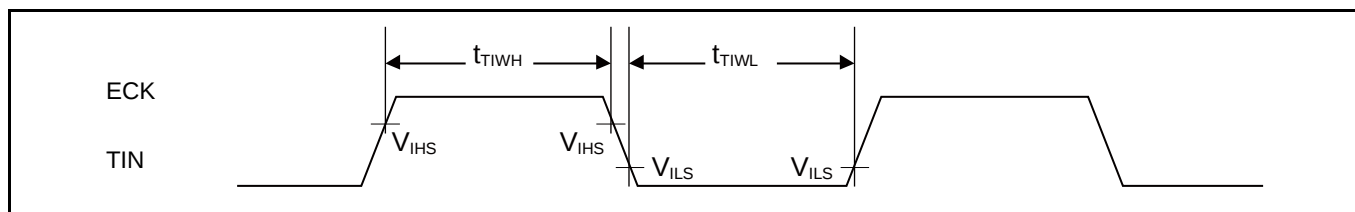
- When the external load capacitance C_L = 30 pF

12.4.11 Base Timer Input Timing

Timer Input Timing

($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$)

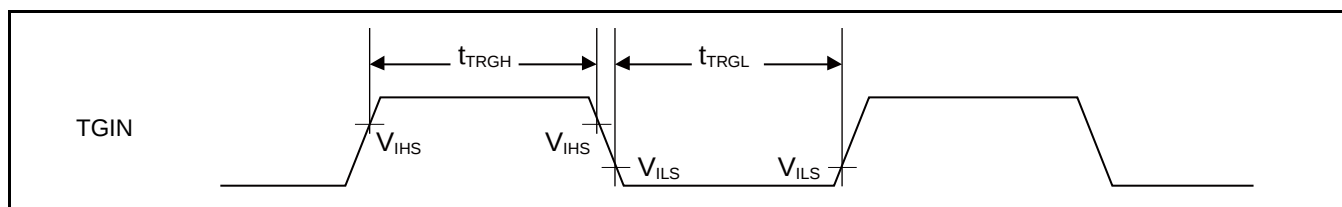
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH} , t_{TIWL}	TIOAn/TIOBn (when using as ECK, TIN)	-	$2t_{CYCP}$	-	ns	



Trigger Input Timing

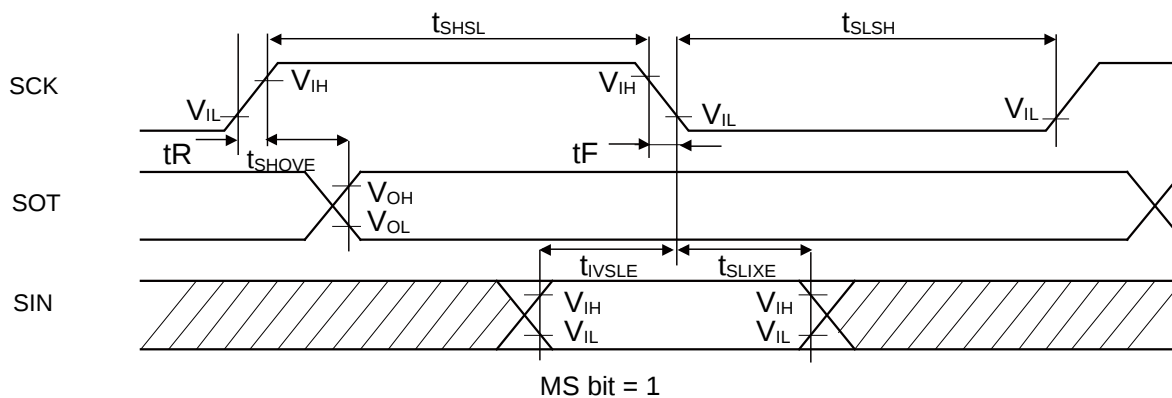
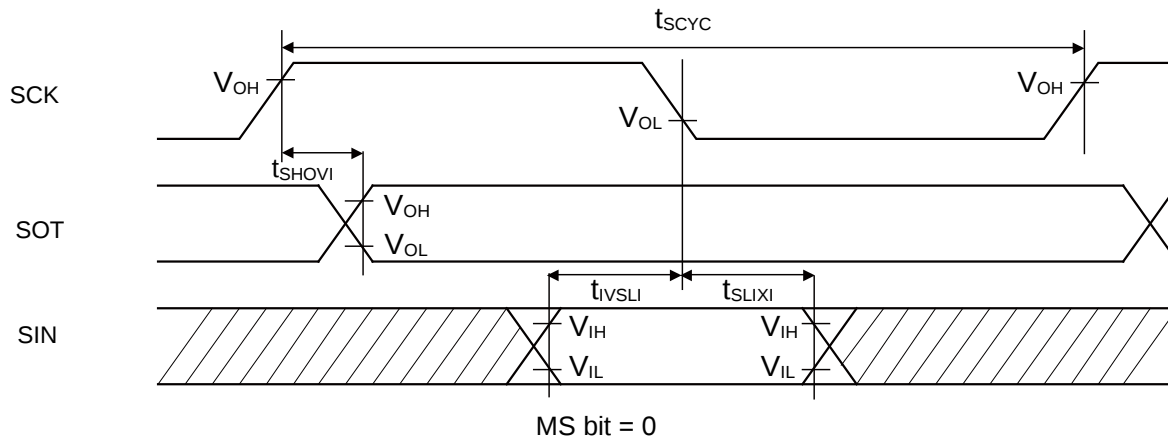
($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$)

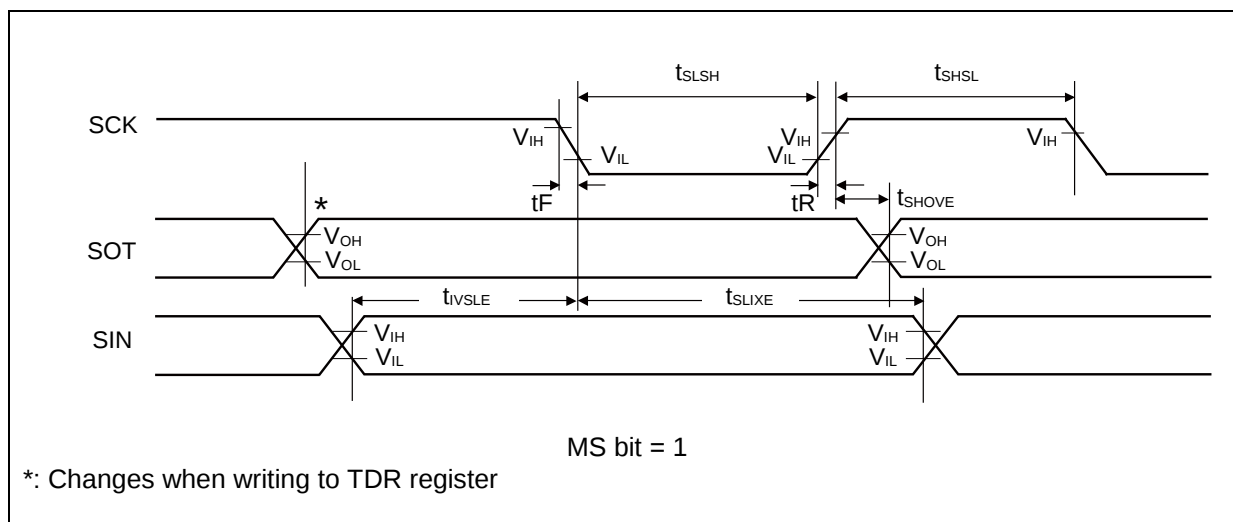
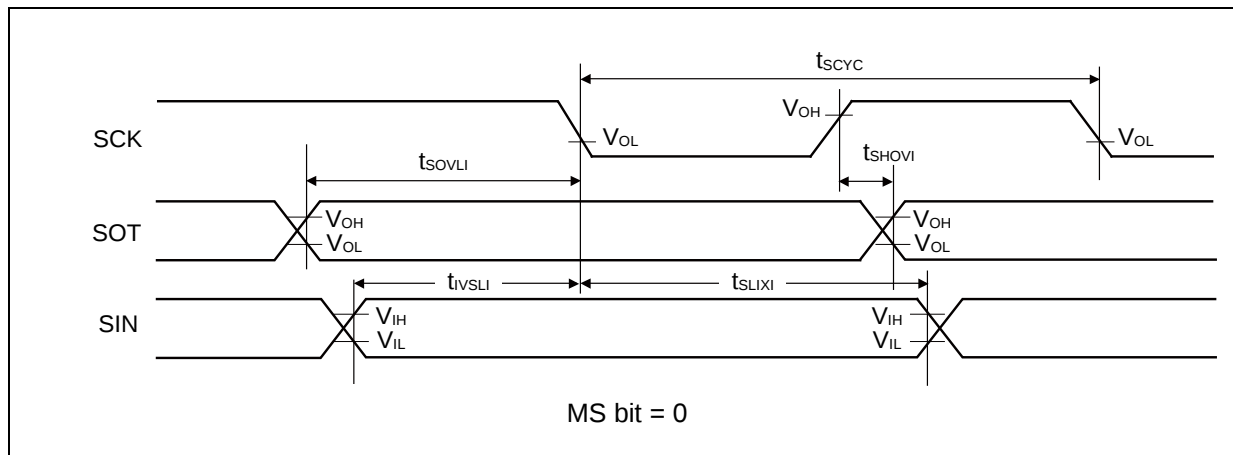
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH} , t_{TRGL}	TIOAn/TIOBn (when using as TGIN)	-	$2t_{CYCP}$	-	ns	

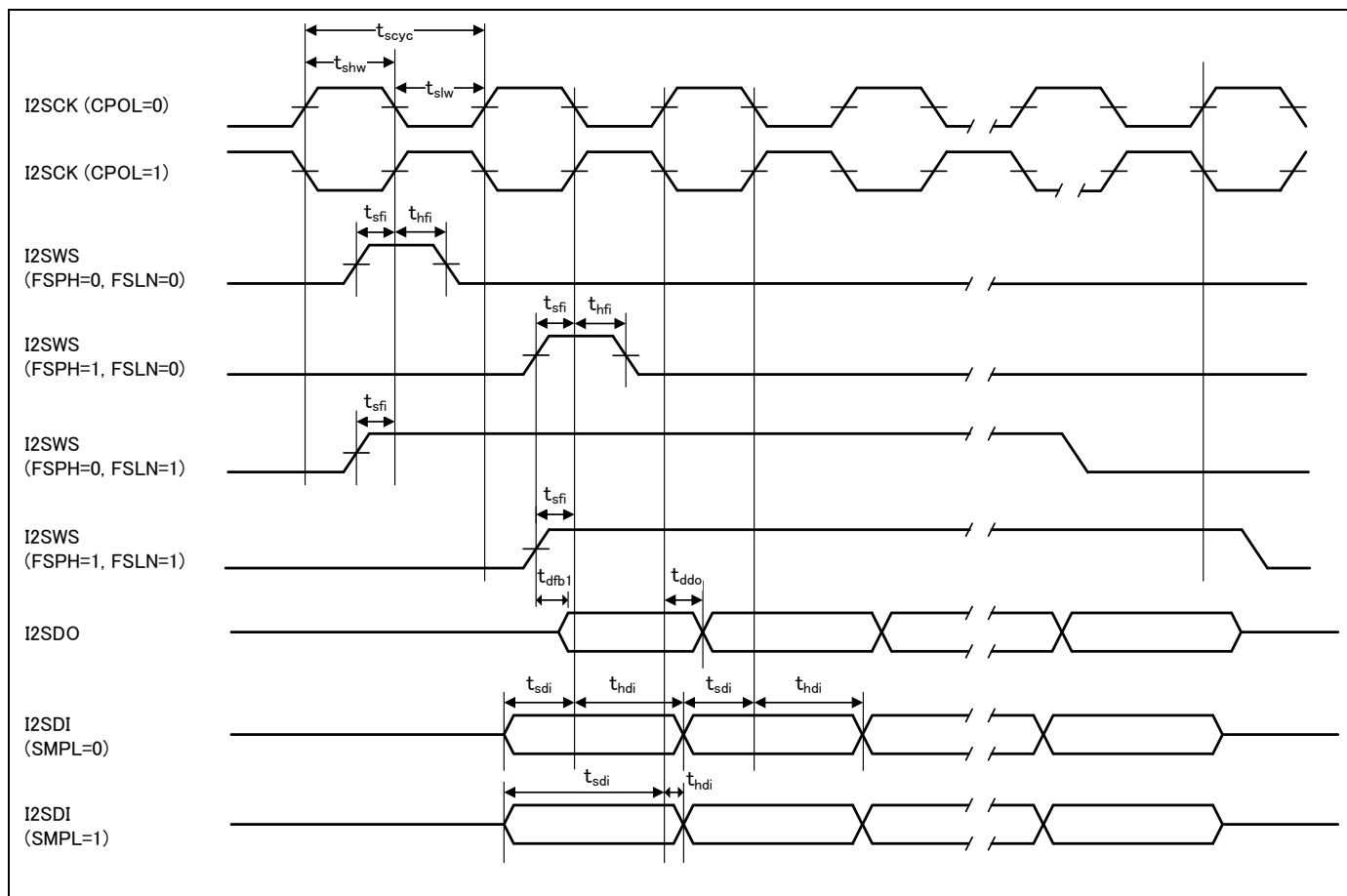


Note:

- t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the base timer is connected, see 8. Block Diagram in this data sheet.

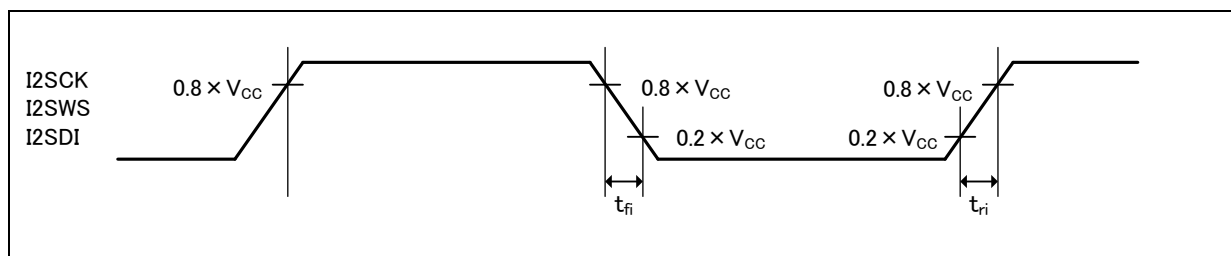






Notes:

- See Chapter7-2: I²S (Inter-IC Sound bus) Interface in FM4 Family Peripheral Manual Communication Macro Part (002-04862) for the details of FSPH, FSLN, SMPL
- I2SCK input is selectable polarity by CPOL bit of CNTREG register



12.8 Low-Voltage Detection Characteristics

12.8.1 Low-Voltage Detection Reset

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	-	2.46	2.55	2.64	V	When voltage drops
Released voltage	VDH	-	2.51	2.60	2.69	V	When voltage rises

12.8.2 Interrupt of Low-Voltage Detection

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 00111	2.80	2.90	3.00	V	When voltage drops
Released voltage	VDH		2.90	3.00	3.11	V	When voltage rises
Detected voltage	VDL	SVHI = 00100	2.99	3.10	3.21	V	When voltage drops
Released voltage	VDH		3.09	3.20	3.31	V	When voltage rises
Detected voltage	VDL	SVHI = 01100	3.18	3.30	3.42	V	When voltage drops
Released voltage	VDH		3.28	3.40	3.52	V	When voltage rises
Detected voltage	VDL	SVHI = 01111	3.67	3.80	3.93	V	When voltage drops
Released voltage	VDH		3.76	3.90	4.04	V	When voltage rises
Detected voltage	VDL	SVHI = 01110	3.76	3.90	4.04	V	When voltage drops
Released voltage	VDH		3.86	4.00	4.14	V	When voltage rises
Detected voltage	VDL	SVHI = 01001	4.05	4.20	4.35	V	When voltage drops
Released voltage	VDH		4.15	4.30	4.45	V	When voltage rises
Detected voltage	VDL	SVHI = 01000	4.15	4.30	4.45	V	When voltage drops
Released voltage	VDH		4.25	4.40	4.55	V	When voltage rises
Detected voltage	VDL	SVHI = 11000	4.25	4.40	4.55	V	When voltage drops
Released voltage	VDH		4.34	4.50	4.66	V	When voltage rises
LVD stabilization wait time	T _{LVDW}	-	-	-	6000×t _{CYCP} *	μs	

*: t_{CYCP} indicates the APB2 bus clock cycle time.

12.11.2 Recovery Cause: Reset

The time from reset release to the program operation start is shown.

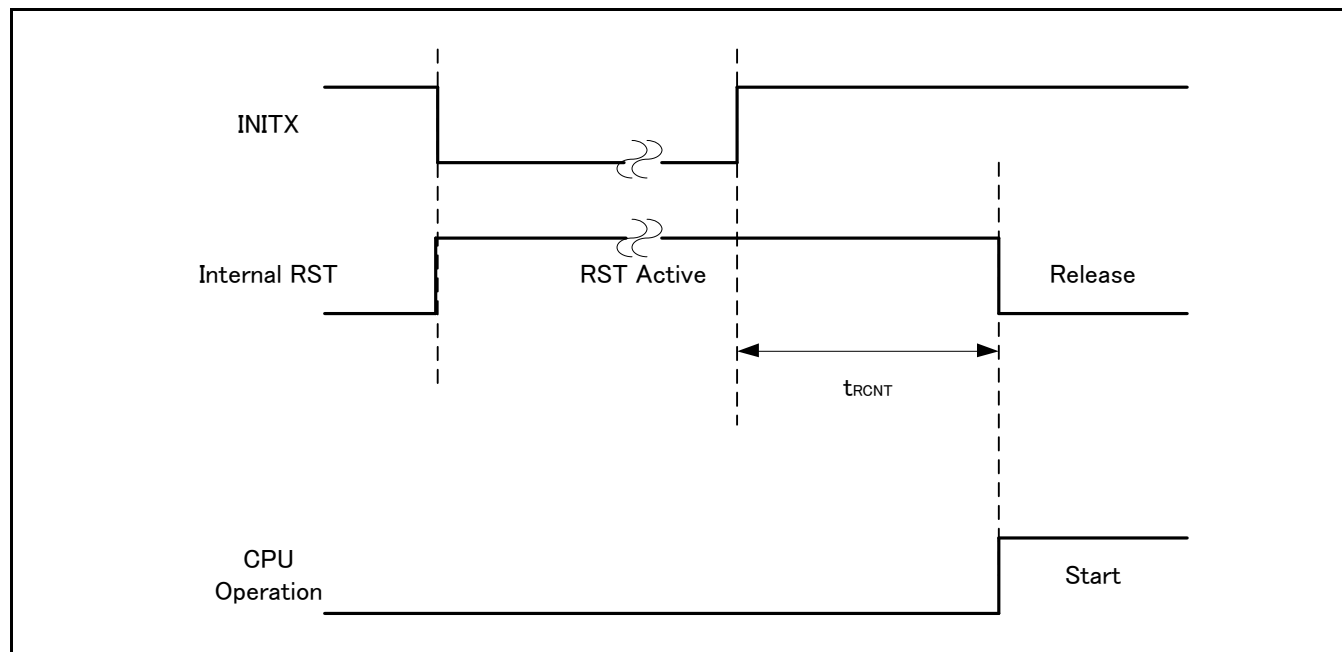
Recovery Count Time

($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t_{RCNT}	155	266	μs	
High-speed CR Timer mode Main Timer mode PLL Timer mode		155	266	μs	
Low-speed CR Timer mode		315	567	μs	
Sub Timer mode		315	567	μs	
RTC mode Stop mode		315	567	μs	
Deep Standby RTC mode with RAM retention Deep Standby Stop mode with RAM retention		336	667	μs	without RAM retention
		336	667	μs	with RAM retention

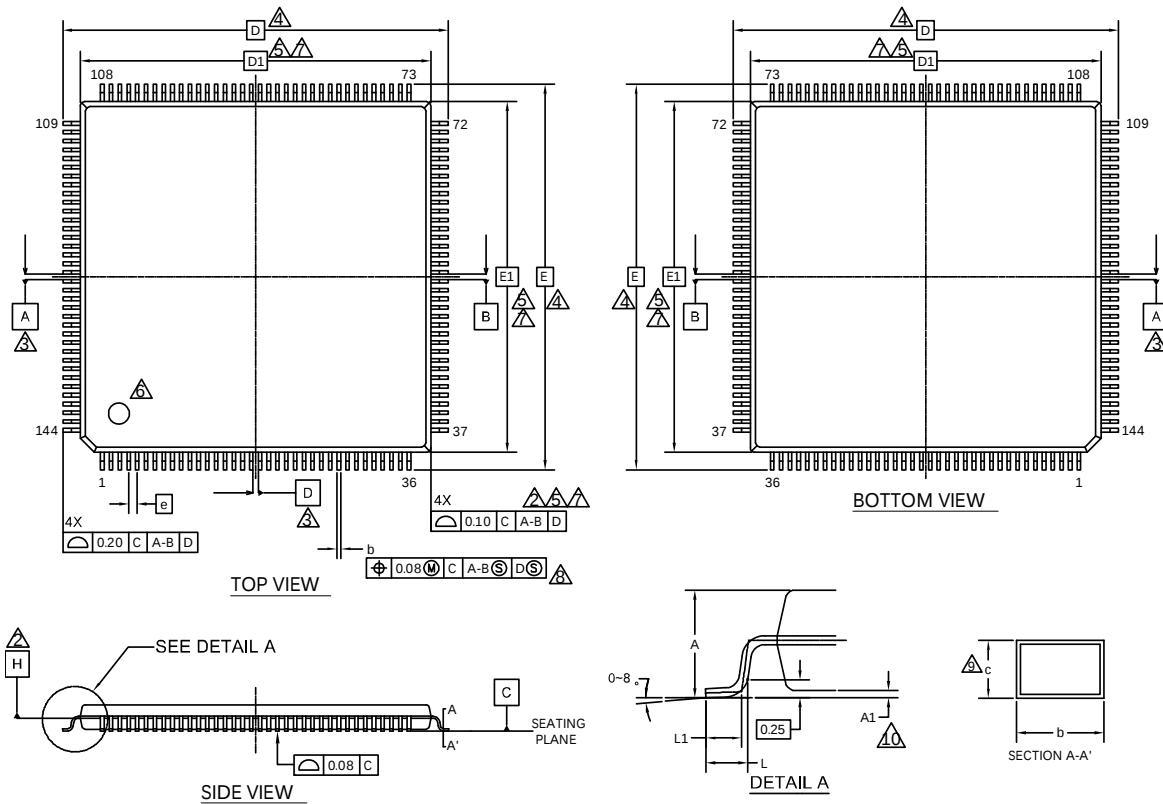
*: The maximum value depends on the built-in CR accuracy.

Example of Standby Recovery Operation (when in INITX Recovery)



14. Package Dimensions

Package Type	Package Code
LQFP 144	LQS 144

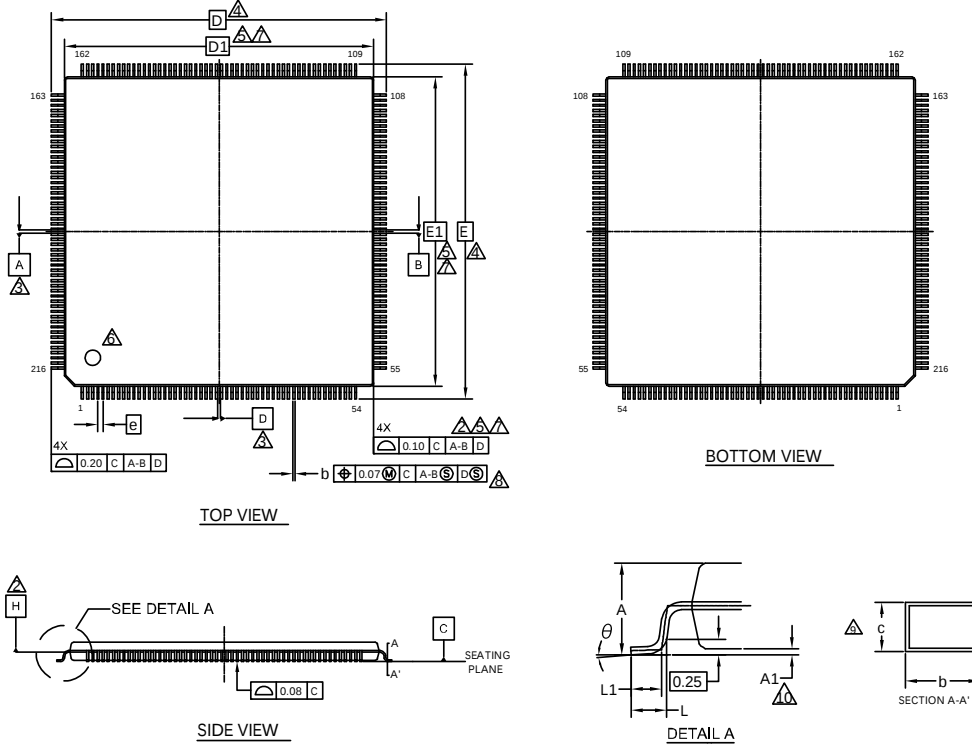


SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.17	0.22	0.27
c	0.09	—	0.20
D	22.00 BSC		
D1	20.00 BSC		
e	0.50 BSC		
E	22.00 BSC		
E1	20.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

NOTES

- ALL DIMENSIONS ARE IN MILLIMETERS
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE.
- DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Package Type	Package Code
LQFP 216	LQQ 216



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.13	0.18	0.23
c	0.09	—	0.20
D	26.00 BSC.		
D1	24.00 BSC.		
e	0.40 BSC.		
E	26.00 BSC.		
E1	24.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

NOTES

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-15153 **

PACKAGE OUTLINE, 216 LEAD LQFP
24.0X24.0X1.7 MM LQQ216 REV**

15. Major Changes

Spancion Publication Number: S6E2C3_DS709-00012

Page	Section	Change Results
Revision 0.1		
-	-	Initial release
Revision 1.0		
11 13 87 88	2. Features 3. Product Lineup 10. Block Diagram 12. Memory Map	Deleted HDM-CEC/Remote Control Receiver.
16-18	5. Pin Assignments	Deleted the pins of HDM-CEC/Remote Control Receiver.(CEC0,CEC1) Revised the pin name of I2S. (MI2S*_0→MI2S*0_0) Deleted the pin of IGTRG0_0.
20-71	6. Pin Descriptions	Deleted the pins of HDM-CEC/Remote Control Receiver.(CEC0,CEC1) Revised the pin name of I2S. (MI2S*_0→MI2S*0_0) Revised the pin number of PF7 in LQFP216.(91→90) revised the pin number of X1. (73, 58, 50, P5→107, 87, 71, P13) Revised the pin number of X0A. (107, 87, 71, P13→73, 58, 50, P5)
72-79	7. I/O Circuit Type	Revised IOH/IOL of Type S.(IOH=-12mA→-10mA, IOL=12mA→10mA) Added the case of using I2C in Type E, F, G, L, N, S.
94-101	13. Pin Status In Each CPU State	Deleted X and Y in Pin Status Type.
102-103	14.1. Absolute Maximum Ratings	Added 10mA type.
104-107	14.2. Recommended Operating Conditions	Added AVRL in Analog reference voltage. Revised the leakage current in Maximum leakage current at operating
108-117	14.3.1. Current Rating	Revised the maximum current of each category.
118-119	14.3.2. Pin Characteristics	Added the characteristic of external bus in H level input voltage (hysteresis input). Added the characteristic of 10 mA type.
122	14.4.5. Operating Conditions of USB PLL · I2S PLL (in the case of using main clock for input clock of PLL)	Revised the maximum of I2S PLL macro oscillation clock frequency. (307.2 MHz→384 MHz)
186	14.5.12-bit A/D Converter	Revised the minimum of Sampling time. Revised the characteristic of State transition time to operation permission Added AVRL in Analog reference voltage.
194	14.8.2. Interrupt of Low-Voltage Detection	Revised the SVHI values in Conditions

NOTE: Please see “Document History” about later revised information.