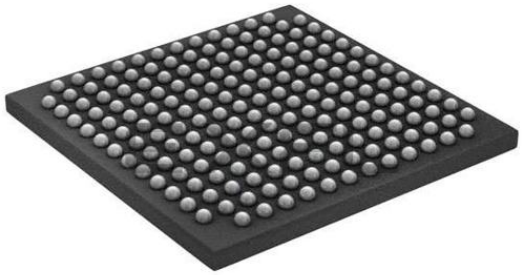


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CSIO, EBI/EMI, I²C, LINbus, SD, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	152
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	192-LFBGA
Supplier Device Package	192-FBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2c39j0agb1000a

4. Pin Descriptions

List of Pin Functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.

Use the extended port function register (EPFR) to select the pin.

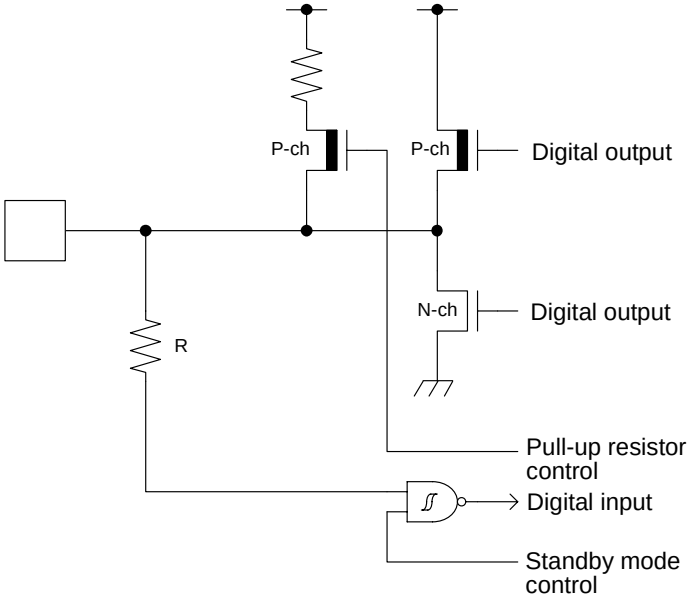
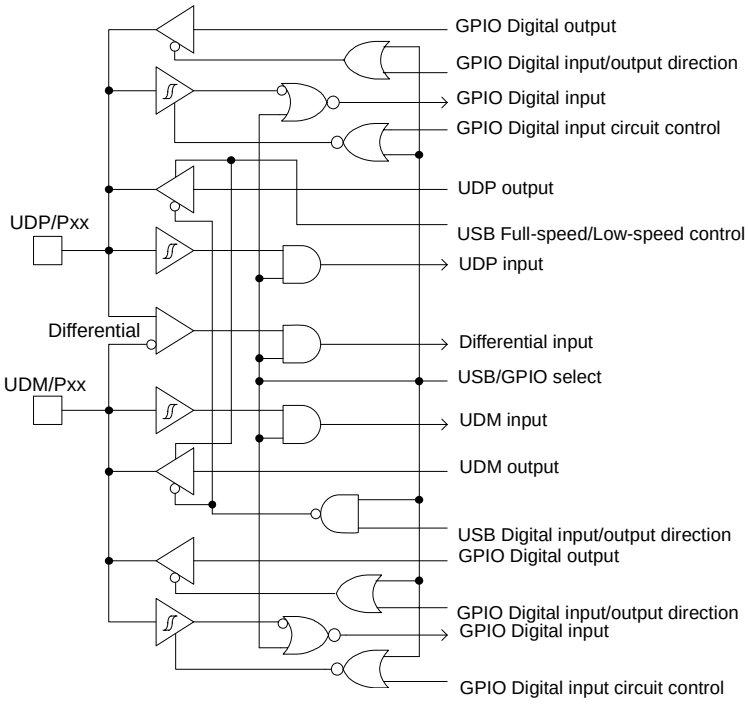
Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
1	1	1	C1	VCC	-	-
2	2	2	B2	PA0 RTO20_0 (PPG20_0) TIOA8_0 AIN2_0 INT00_0 MADATA00_0	G	K
3	3	3	C2	PA1 RTO21_0 (PPG20_0) TIOA9_0 BIN2_0 MADATA01_0	G	I
4	4	4	C3	PA2 RTO22_0 (PPG22_0) TIOA10_0 ZIN2_0 MADATA02_0	G	I
5	5	5	D5	PA3 RTO23_0 (PPG22_0) TIOA11_0 MADATA03_0	G	I
6	6	6	D2	PA4 RTO24_0 (PPG24_0) TIOA12_0 MADATA04_0	G	I
7	7	7	D1	PA5 SIN1_0 RTO25_0 (PPG24_0) TIOA13_0 INT01_0 MADATA05_0	G	K
8	8	8	D3	PA6 SOT1_0 (SDA1_0)) DTTI2X_0 MADATA06_0	E	I
9	9	9	D4	PA7 SCK1_0 (SCL1_0) IC20_0 MADATA07_0	E	I

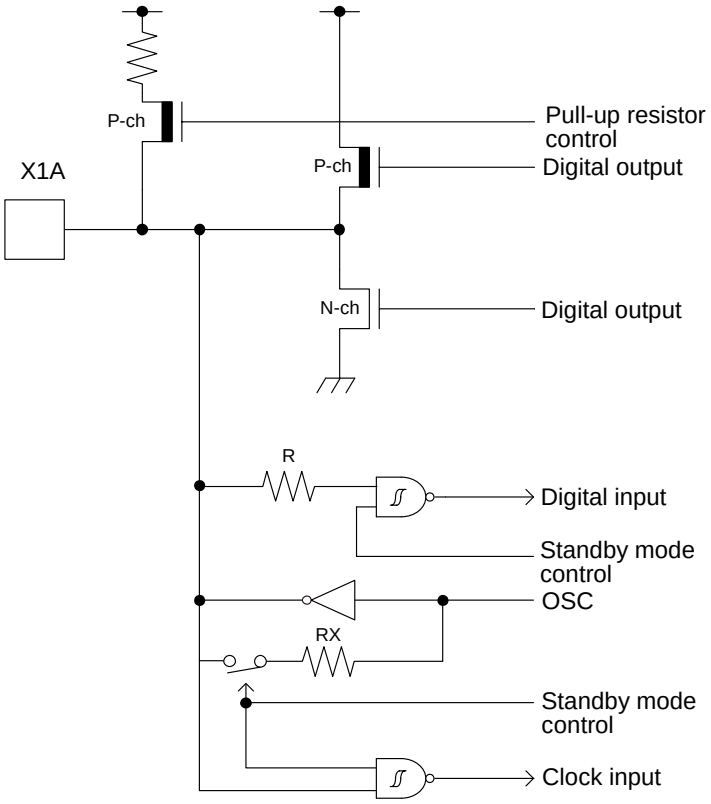
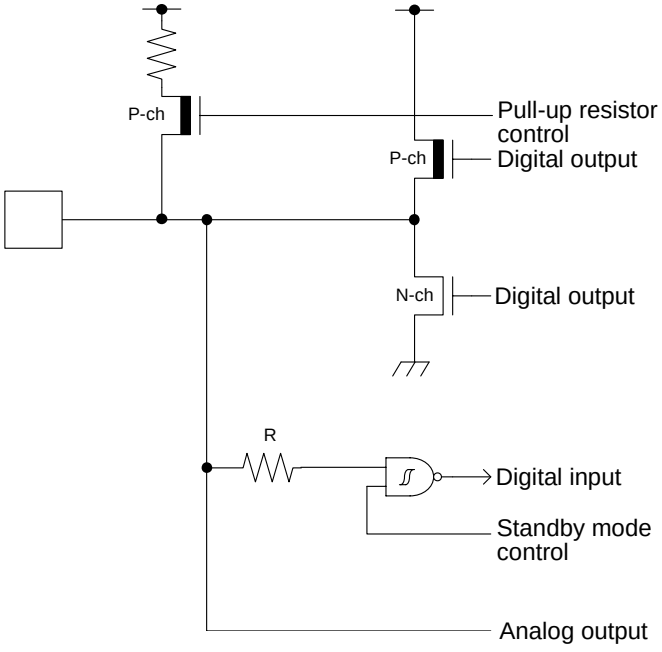
Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Debugger	TRACED12	Trace data output pin of HTM	148	-	-	-
	TRACED13		149	-	-	-
	TRACED14		150	-	-	-
	TRACED15		151	-	-	-
	TRSTX	JTAG test reset Input pin	164	134	110	B13
External bus	MAD00_0	External bus interface address bus	81	66	56	J6
	MAD01_0		82	67	57	L8
	MAD02_0		83	68	58	K8
	MAD03_0		84	69	59	J8
	MAD04_0		91	76	60	K9
	MAD05_0		92	77	61	P10
	MAD06_0		93	78	62	N10
	MAD07_0		96	79	63	L10
	MAD08_0		97	80	64	K10
	MAD09_0		98	81	65	M10
	MAD10_0		142	116	92	G10
	MAD11_0		143	117	93	G9
	MAD12_0		144	118	94	F10
	MAD13_0		145	119	95	F11
	MAD14_0		146	120	96	F12
	MAD15_0		147	121	97	F13
	MAD16_0		152	122	98	E10
	MAD17_0		153	123	99	E11
	MAD18_0		154	124	100	E12
	MAD19_0		50	40	35	L1
	MAD20_0		49	39	34	K4
	MAD21_0		48	38	33	K3
	MAD22_0		47	37	32	K2
	MAD23_0		46	36	31	K1
	MAD24_0		45	35	30	J2
	MCSX0_0	External bus interface chip select output pin	71	56	48	M5
	MCSX1_0		70	55	47	L5
	MCSX2_0		61	51	43	N4
	MCSX3_0		60	50	42	M4
	MCSX4_0		59	49	41	L4
	MCSX5_0		58	48	40	M3
	MCSX6_0		57	47	39	N3
	MCSX7_0		56	46	38	N2
	MCSX8_0		88	73	-	P9

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
External bus	MCLKOUT_0	External bus interface external clock output pin	32	23	20	G5
	MNALE_0	External bus interface ALE signal to control NAND flash output pin	47	37	32	K2
	MNCLE_0	External bus interface CLE signal to control NAND flash output pin	48	38	33	K3
	MNREX_0	External bus interface read enable signal to control NAND flash	50	40	35	L1
	MNWEX_0	External bus interface write enable signal to control NAND flash	49	39	34	K4
	MOEX_0	External bus interface read enable signal for SRAM	209	169	137	C5
	MWEX_0	External bus interface write enable signal for SRAM	210	170	138	B4
	MSDCLK_0	SDRAM interface SDRAM clock output pin	90	75	-	L9
	MSDCKE_0	SDRAM interface SDRAM clock enable pin	89	74	-	M9
	MRASX_0	SDRAM interface SDRAM column active strobe pin	85	70	-	N8
	MCASX_0	SDRAM interface SDRAM row active strobe pin	86	71	-	M8
	MSDWEX_0	SDRAM interface SDRAM write enable pin	87	72	-	N9
External interrupt	INT00_0	External interrupt request 00 input pin	2	2	2	B2
	INT00_1		38	28	23	H3
	INT00_2		19	-	-	-
	INT01_0	External interrupt request 01 input pin	7	7	7	D1
	INT01_1		41	31	26	H6
	INT01_2		51	41	-	L2
	INT02_0	External interrupt request 02 input pin	14	13	10	E5
	INT02_1		42	32	27	J5
	INT02_2		26	-	-	-
	INT03_0	External interrupt request 03 input pin	17	16	13	F3
	INT03_1		43	33	28	J4
	INT03_2		34	24	-	G6
	INT04_0	External interrupt request 04 input pin	59	49	41	L4
	INT04_1		100	83	67	M11
	INT04_2		65	-	-	-
	INT05_0	External interrupt request 05 input pin	70	55	47	L5
	INT05_1		86	71	-	M8
	INT05_2		68	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	PC0	General-purpose I/O port C	177	145	115	C9
	PC1		178	146	116	B8
	PC2		179	147	117	D9
	PC3		180	148	118	E9
	PC4		181	149	119	F9
	PC5		182	150	120	C8
	PC6		183	151	121	D8
	PC7		184	152	122	E8
	PC8		185	153	123	A10
	PC9		186	154	124	F8
	PCA		187	155	125	B7
	PCB		190	158	128	A7
	PCC		191	159	129	C7
	PCD		192	160	130	A6
	PCE		193	161	131	D7
	PCF		194	162	132	E7
	PD0	General-purpose I/O port D	195	163	133	F7
	PD1		196	164	134	B6
	PD2		197	165	135	C6
	PE0	General-purpose I/O port E	104	84	68	N13
	PE2		106	86	70	P12
	PE3		107	87	71	P13
	PF0	General-purpose I/O port F	78	63	-	K5
	PF1		79	64	-	K6
	PF2		85	70	-	N8
	PF3		86	71	-	M8
	PF4		87	72	-	N9
	PF5		88	73	-	P9
	PF6		89	74	-	M9
	PF7		90	75	-	L9
	PF8		94	-	-	-
	PF9		95	-	-	-
	PFA		101	-	-	-
	PFB		102	-	-	-
	PFC		103	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Serial 9	SIN9_0	Multi-function serial interface ch 9 input pin	82	67	57	L8
	SIN9_1		120	-	-	-
	SOT9_0 (SDA9_0)	Multi-function serial interface ch 9 output pin. This pin operates as SOT9 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA9 when it is used in an I²C (operation mode 4).	83	68	58	K8
	SOT9_1 (SDA9_1)		121	-	-	-
	SCK9_0 (SCL9_0)	Multi-function serial interface ch 9 clock I/O pin. This pin operates as SCK9 when it is used in a CSIO (operation mode 2) and as SCL9 when it is used in an I²C (operation mode 4).	84	69	59	J8
	SCK9_1 (SCL9_1)		122	-	-	-
Multi-Function Serial 10	SIN10_0	Multi-function serial interface ch 10 input pin	114	94	78	L11
	SIN10_1		51	41	-	L2
	SOT10_0 (SDA10_0)	Multi-function serial interface ch 10 output pin. This pin operates as SOT10 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA10 when it is used in an I²C (operation mode 4).	115	95	79	K13
	SOT10_1 (SDA10_1)		52	42	-	L3
	SCK10_0 (SCL10_0)	Multi-function serial interface ch 10 clock I/O pin. This pin operates as SCK10 when it is used in a CSIO (operation mode 2) and as SCL10 when it is used in an I²C (operation mode 4).	116	96	80	K12
	SCK10_1 (SCL10_1)		53	43	-	M2
Multi-Function Serial 11	SIN11_0	Multi-function serial interface ch 11 input pin	123	99	83	J13
	SIN11_1		26	-	-	-
	SOT11_0 (SDA11_0)	Multi-function serial interface ch 11 output pin. This pin operates as SOT11 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA11 when it is used in an I²C (operation mode 4).	124	100	84	J12
	SOT11_1 (SDA11_1)		27	-	-	-
	SCK11_0 (SCL11_0)	Multi-function serial interface ch 11 clock I/O pin. This pin operates as SCK11 when it is used in a CSIO (operation mode 2) and as SCL11 when it is used in an I²C (operation mode 4).	125	101	85	J11
	SCK11_1 (SCL11_1)		28	-	-	-

Type	Circuit	Remarks
G		・ CMOS level output ・ CMOS level hysteresis input ・ Pull-up resistor control ・ Standby mode control ・ Pull-up resistor: approximately 50 kΩ ・ I_{OH} = -12 mA, I_{OL} = 12 mA ・ When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.
H		It is possible to select either USB I/O or GPIO function. When the USB I/O is selected: ・ Full-speed, low-speed control When the GPIO is selected: ・ CMOS level output ・ CMOS level hysteresis input ・ Standby mode control ・ I_{OH} = -20.5 mA, I_{OL} = 18.5 mA

Type	Circuit	Remarks
Q		It is possible to select the sub oscillation/GPIO function. When the sub oscillation is selected: ・ Oscillation feedback resistor: approximately 10 MΩ When the GPIO is selected: ・ CMOS level output. ・ CMOS level hysteresis input ・ Pull-up resistor control ・ Pull-up resistor: approximately 50 kΩ ・ I_{OH} = -4 mA, I_{OL} = 4 mA ・ For I/O setting, refer to VBAT Domain in the "FM4 Family Peripheral Manual Main Part (002-04856)."
R		・ CMOS level output ・ CMOS level hysteresis input ・ Analog output ・ Pull-up resistor control ・ Standby mode control ・ Pull-up resistor: approximately 50 kΩ ・ I_{OH} = -4 mA, I_{OL} = 4 mA (4.5V to 5.5V) ・ I_{OH} = -2 mA, I_{OL} = 2 mA (2.7V to 4.5V)

Latch-Up

Semiconductor devices are constructed by the formation of p-type and n-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic pnpn junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred milliamps to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

As previously mentioned, all semiconductor devices have inherent rates of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

6.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

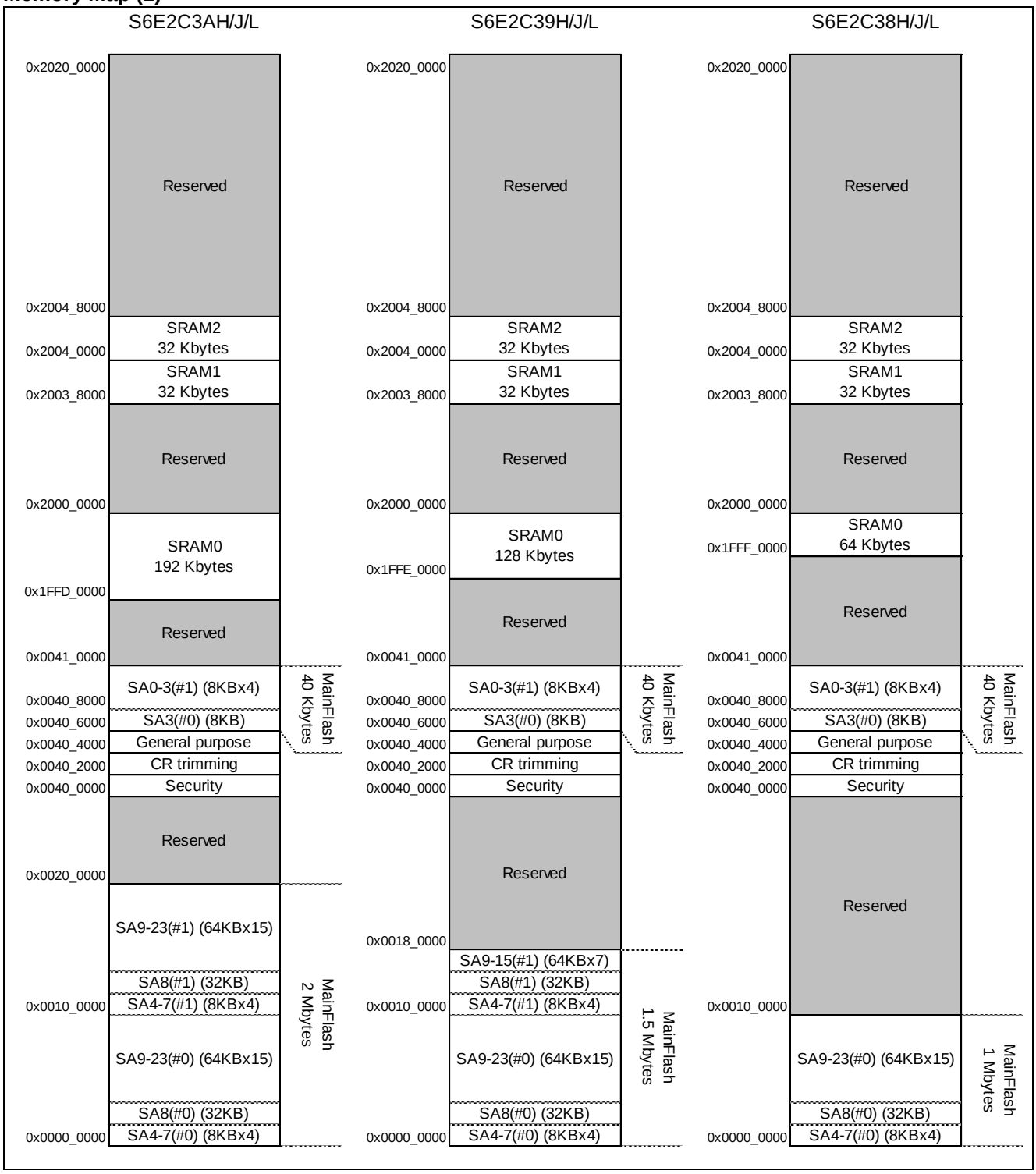
Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Memory Map (2)



*: See S6E2CC/S6E2C5/S6E2C4/S6E2C3/S6E2C2/S6E2C1 Series Flash Programming Manual to confirm the detail of flash Memory.

Package thermal resistance and maximum permissible power for each package are shown below.
The operation is guaranteed maximum permissible power or less for semiconductor devices.

Table for Package Thermal Resistance and Maximum Permissible Power

Package	Printed Circuit Board	Thermal Resistance θ_{JA} (°C/W)	Maximum Permissible Power (mW)	
			T_A = +85°C	T_A = +105°C
LQS144 (0.5-mm pitch)	Single-layered both sides	48	833	417
	4 layers	33	1212	606
LQP176 (0.5-mm pitch)	Single-layered both sides	45	889	444
	4 layers	31	1290	645
LQQ216 (0.4-mm pitch)	Single-layered both sides	46	870	435
	4 layers	32	1250	625
LBE192 (0.8-mm pitch)	Single-layered both sides	-	-	-
	4 layers	35	1143	571

WARNING:

1. *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.*
2. *Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.*
3. *No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet.*
4. *Users considering application outside the listed conditions are advised to contact their representatives beforehand.*

12.3 DC Characteristics

12.3.1 Current Rating

Table 12-1 Typical and Maximum Current Consumption in Normal Operation (PLL), Code Running from Flash Memory (Flash Accelerator Mode and Trace Buffer Function Enabled)

Parameter	Symbol	Pin Name	Conditions		Frequency*4	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation *7,*8 (PLL)	*5	200 MHz	117	224	mA	*3 When all peripheral clocks are on
					192 MHz	113	219	mA	
					180 MHz	106	211	mA	
				*6	160 MHz	95	197	mA	
					144 MHz	86	186	mA	
					120 MHz	73	169	mA	
					100 MHz	61	155	mA	
					80 MHz	50	140	mA	
					60 MHz	39	126	mA	
					40 MHz	27	112	mA	
					20 MHz	16	97	mA	
					8 MHz	8.7	88.9	mA	
					4 MHz	6.4	86.1	mA	
				*5	200 MHz	71	168	mA	*3 When all peripheral clocks are off
					192 MHz	68	165	mA	
					180 MHz	64	159	mA	
				*6	160 MHz	58	151	mA	
					144 MHz	52	144	mA	
					120 MHz	44	134	mA	
					100 MHz	38	126	mA	
					80 MHz	31	117	mA	
					60 MHz	24	109	mA	
					40 MHz	17	100	mA	
					20 MHz	10	91	mA	
					8 MHz	6.3	86.1	mA	
					4 MHz	5.0	84.5	mA	

*1: T_A = +25°C, V_{CC} = 3.3 V

*2: T_J = +125°C, V_{CC} = 5.5 V

*3: When all ports are fixed

*4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK

*5: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 11, FBFCR.BE = 1)

*6: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 1)

*7: Firmware being executed during data collection for this table is not being accessed from the MainFlash memory."

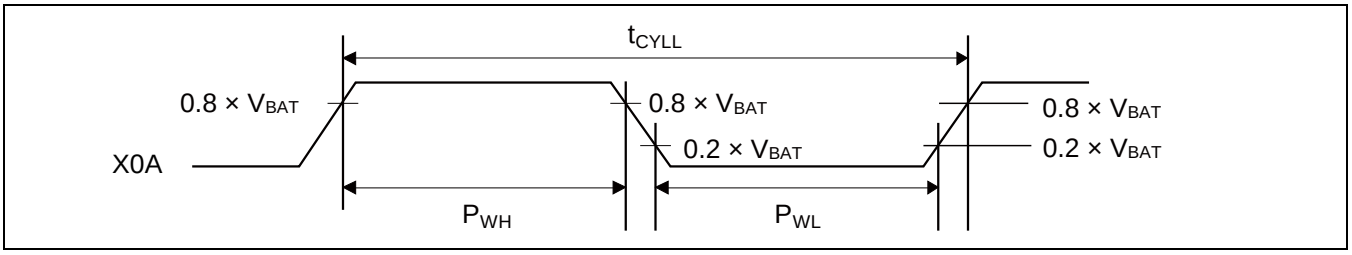
*8: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

12.4.2 Sub Clock Input Characteristics

(V_{BAT} = 1.65V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	$1/t_{CYLL}$	X0A, X1A	-	-	32.768	-	kHz	When crystal oscillator is connected *
			-	32	-	100	kHz	When using external clock
Input clock cycle	t_{CYLL}		-	10	-	31.25	µs	When using external clock
Input clock pulse width	-		P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	45	-	55	%	When using external clock

*: For more information about crystal oscillator, see Sub crystal oscillator in 7. Handling Devices.



12.4.3 Built-In CR Oscillation Characteristics

Built-In High-speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRH}	T_J = - 20°C to + 105°C	3.92	4	4.08	MHz	When trimming *1
		T_J = - 40°C to + 125°C	3.88	4	4.12		
		T_J = - 40°C to + 125°C	3	4	5		When not trimming
Frequency stabilization time	t_{CRWT}	-	-	-	30	µs	*2

*1: In the case of using the values in CR trimming area of flash memory at shipment for frequency/temperature trimming

*2: This is the time to stabilize the frequency of the High-speed CR clock after setting trimming value. During this period, it is able to use the High-speed CR clock as a source clock.

Built-In Low-speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Condition	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRL}	-	50	100	150	kHz	

Synchronous Serial (SPI = 1, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
SOT→SCK↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK fall time	tF	SCKx		-	5	-	5	ns
SCK rise time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.*
- *These characteristics only guarantee the same relocate port number; for example, the combination of SCKx_0 and SOTx_1 is not guaranteed.*
- *When the external load capacitance C_L = 30 pF.*

When Using Synchronous Serial Chip Select (SCINV = 1, CSLVL = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	ns
SCS↓→SCK↓ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↑→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS↓→SOT delay time	t_{DSE}		-	40	-	40	ns
SCS↑→SOT delay time	t_{DEE}		0	-	0	-	ns

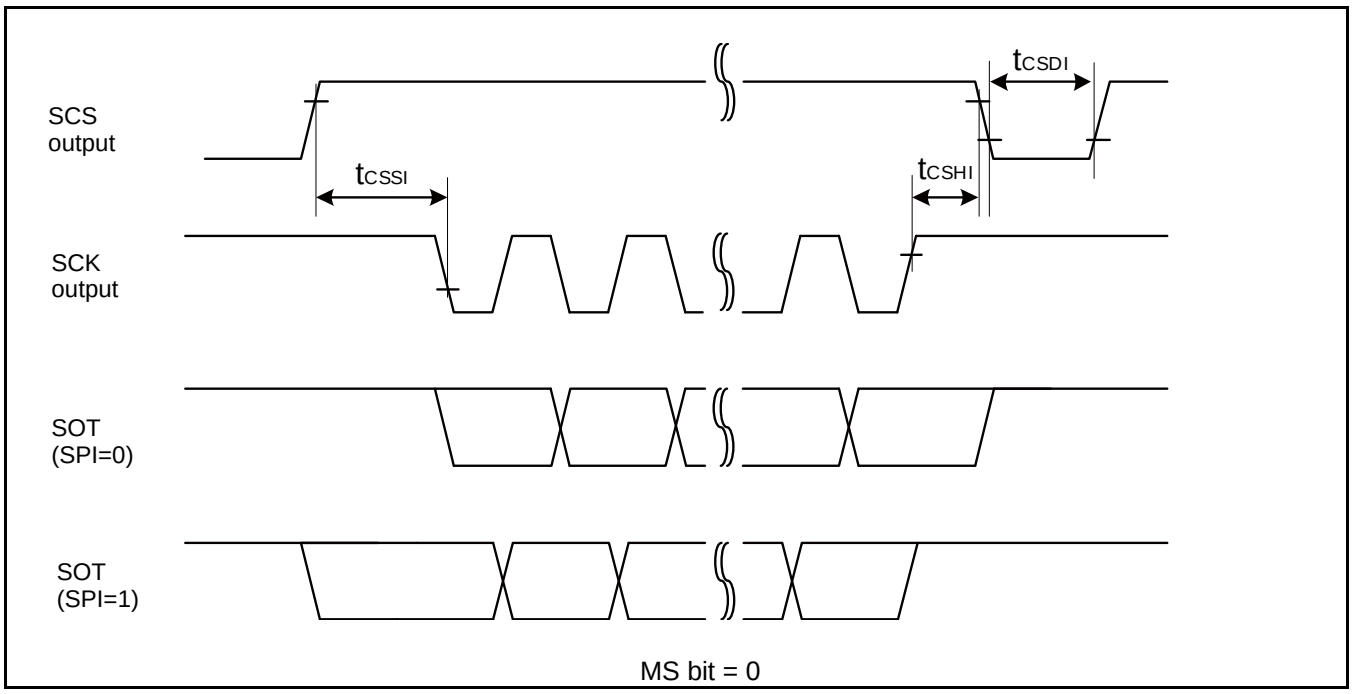
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

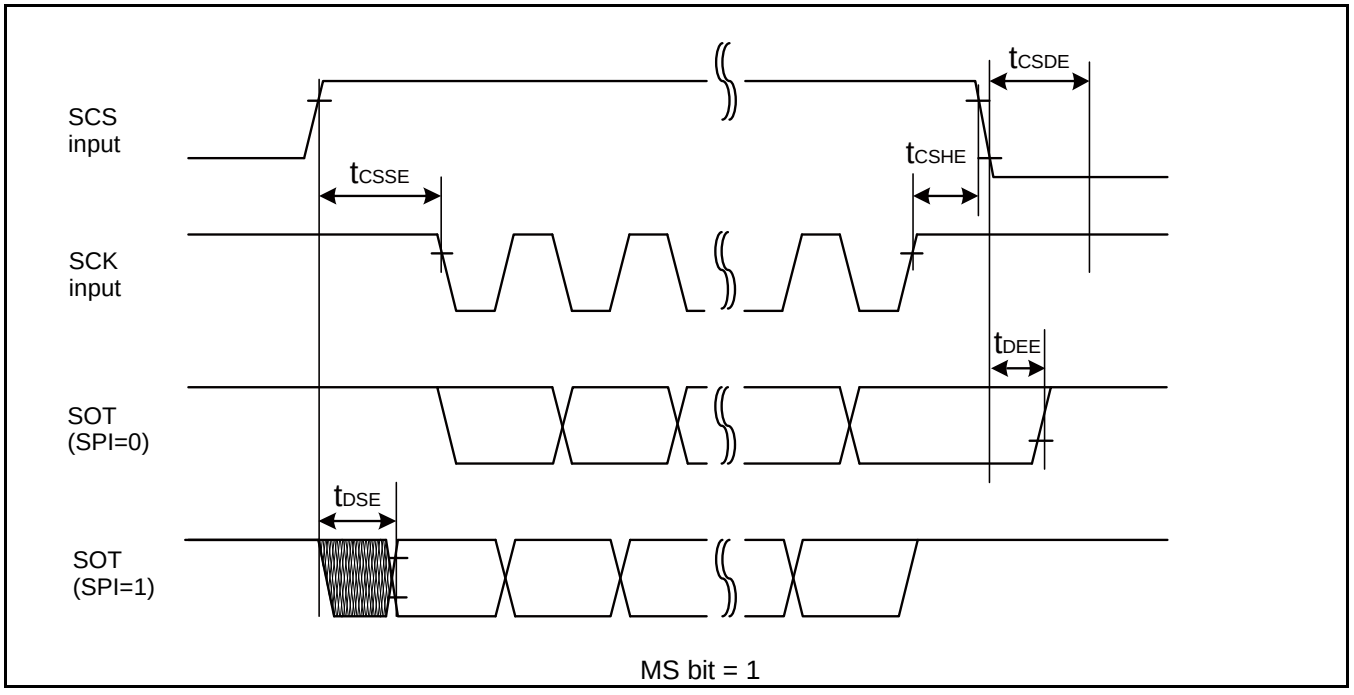
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.*
- *For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0



MS bit = 1

12.4.19 I²S Timing

Master Mode Timing

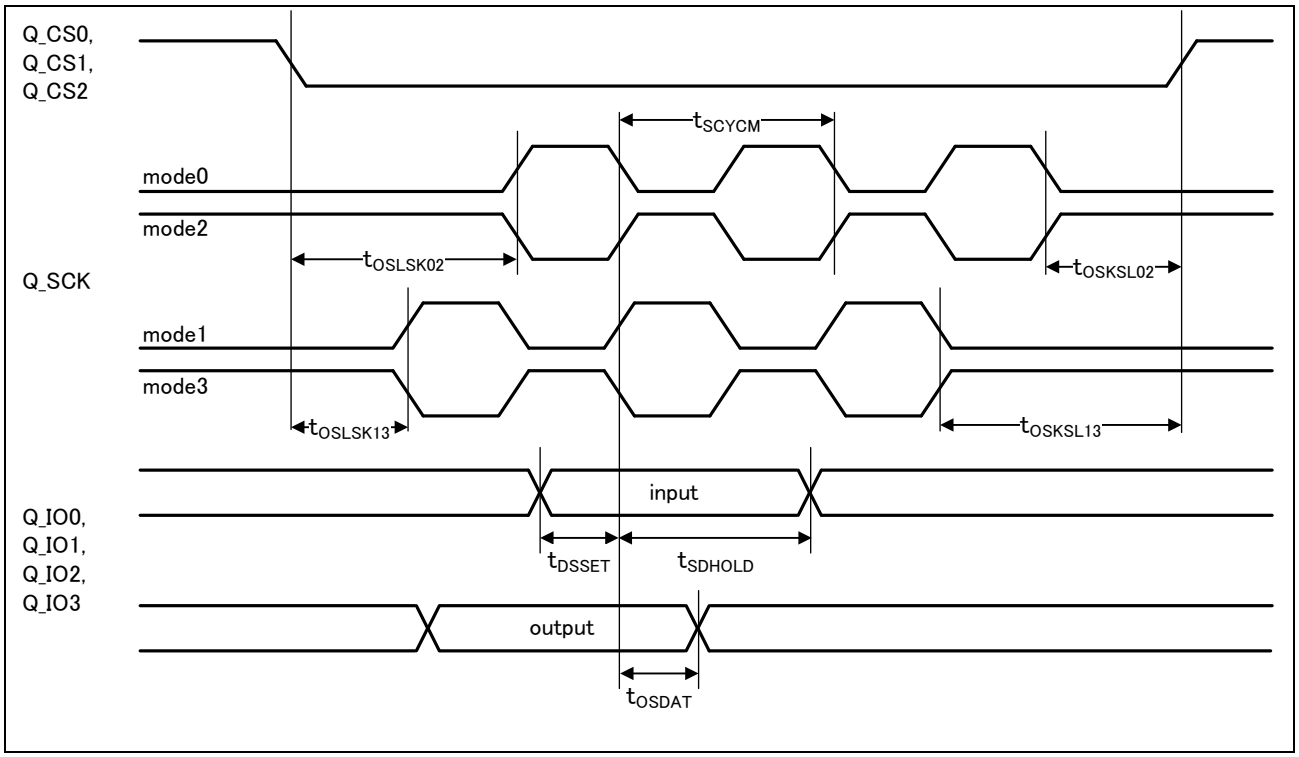
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output frequency	f_{MCYC}	I2SCK	-	-	12.288	MHz	
Output clock pulse width	t_{MHW}	I2SCK	-	45	55	%	
	t_{MLW}			45	55	%	
I2SCK→I2SWS delay time	t_{DFS}	I2SCK, I2SWS	-	0	24.0	ns	
I2SCK→I2SDO delay time*	t_{DDO}	I2SCK, I2SDO	-	0	24.0	ns	
I2SDI→I2SCK setup time	t_{HSDI}	I2SCK, I2SDI	-	25.0	-	ns	
I2SDI→I2SCK hold time	t_{HDI}		-	0	-	ns	
Input signal rise time	t_{FI}	I2SDI	-	-	5	ns	
Input signal fall time	t_{FI}		-	-	5	ns	

*: Except for the first bit of transmission frame

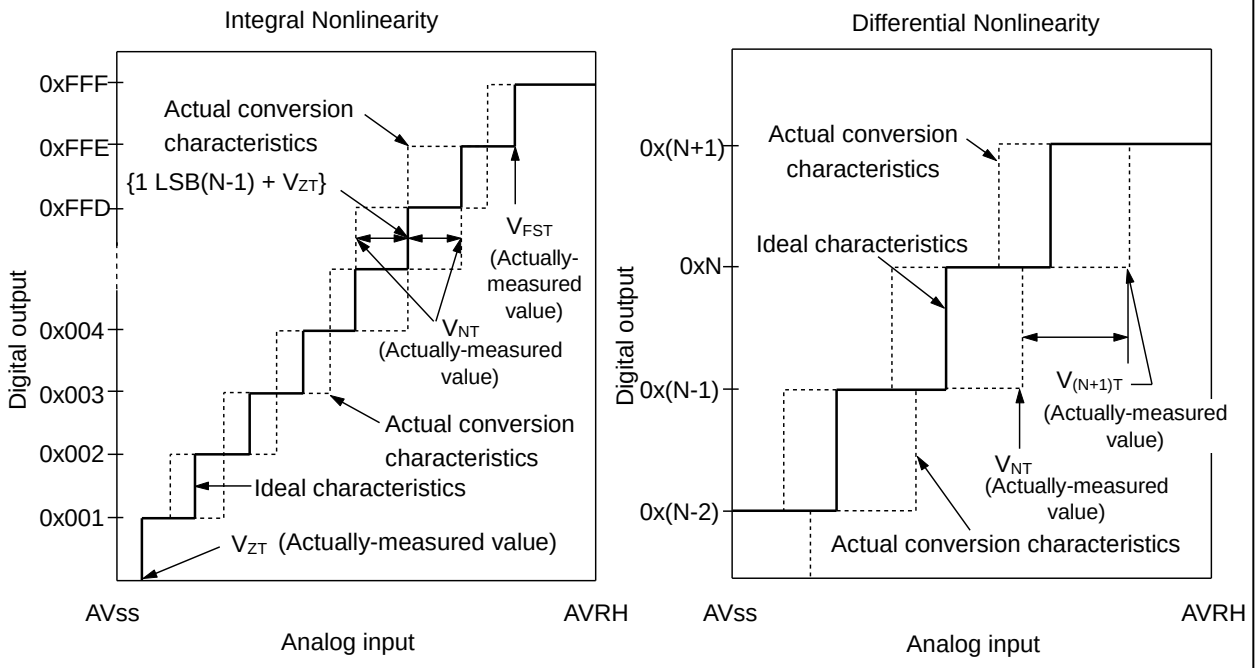
Notes:

- *When the external load capacitance C_L = 20 pF*
- *When I2SWS = 48 kHz, I2MCLK = 256 × I2SWS*
  Frame synchronization signal (I2SWS) is settable to 48 kHz, 32 kHz, 16 kHz.
  See Chapter7-2: I²S (Inter-IC Sound bus) Interface in FM4 Family Peripheral Manual Communication Macro Part (002-04862) for the details.


Q_CS0,
Q_CS1,
Q_CS2
tSCYCM
mode0
mode2
tOSLSK02
tOSKSL02
Q_SCK
mode1
mode3
tOSLSK13
tOSKSL13
input
Q_IO0,
Q_IO1,
Q_IO2,
Q_IO3
tDSSET
tSDHOLD
output
tOSDAT

Definition of 12-bit A/D Converter Terms

- Resolution: Analog variation that is recognized by an A/D converter.
- Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.
- Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

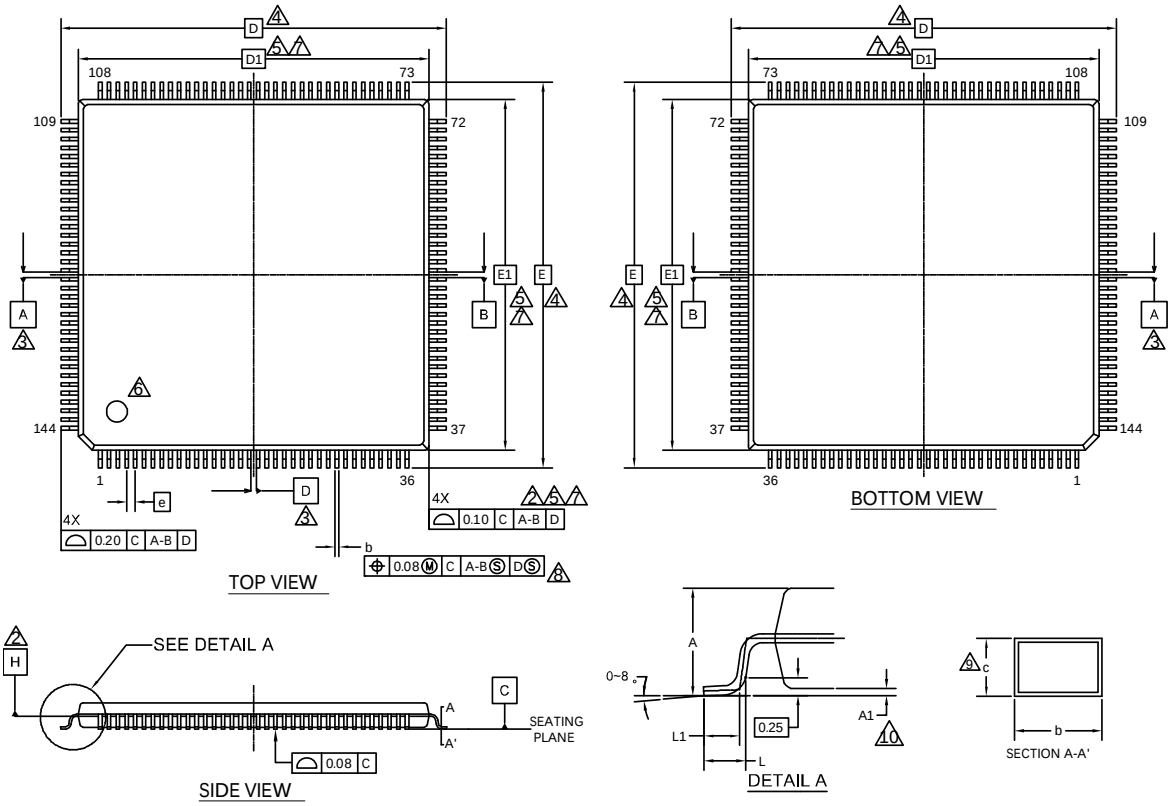
$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N: A/D converter digital output value.
V_{ZT}: Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST}: Voltage at which the digital output changes from 0xFFE to 0xFFF.
V_{NT}: Voltage at which the digital output changes from 0x(N − 1) to 0xN.

14. Package Dimensions

Package Type	Package Code
LQFP 144	LQS 144



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.17	0.22	0.27
c	0.09	—	0.20
D	22.00 BSC		
D1	20.00 BSC		
e	0.50 BSC		
E	22.00 BSC		
E1	20.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

PACKAGE OUTLINE, 144 LEAD LQFP
20.0X20.0X1.7 MM LQS144 Rev**

002-13015 **

15. Major Changes

Spansion Publication Number: S6E2C3_DS709-00012

Page	Section	Change Results
Revision 0.1		
-	-	Initial release
Revision 1.0		
11 13 87 88	2. Features 3. Product Lineup 10. Block Diagram 12. Memory Map	Deleted HDM-CEC/Remote Control Receiver.
16-18	5. Pin Assignments	Deleted the pins of HDM-CEC/Remote Control Receiver.(CEC0,CEC1) Revised the pin name of I2S. (MI2S*_0→MI2S*0_0) Deleted the pin of IGTRG0_0.
20-71	6. Pin Descriptions	Deleted the pins of HDM-CEC/Remote Control Receiver.(CEC0,CEC1) Revised the pin name of I2S. (MI2S*_0→MI2S*0_0) Revised the pin number of PF7 in LQFP216.(91→90) revised the pin number of X1. (73, 58, 50, P5→107, 87, 71, P13) Revised the pin number of X0A. (107, 87, 71, P13→73, 58, 50, P5)
72-79	7. I/O Circuit Type	Revised IOH/IOL of Type S.(IOH=-12mA→-10mA, IOL=12mA→10mA) Added the case of using I2C in Type E, F, G, L, N, S.
94-101	13. Pin Status In Each CPU State	Deleted X and Y in Pin Status Type.
102-103	14.1. Absolute Maximum Ratings	Added 10mA type.
104-107	14.2. Recommended Operating Conditions	Added AVRL in Analog reference voltage. Revised the leakage current in Maximum leakage current at operating
108-117	14.3.1. Current Rating	Revised the maximum current of each category.
118-119	14.3.2. Pin Characteristics	Added the characteristic of external bus in H level input voltage (hysteresis input). Added the characteristic of 10 mA type.
122	14.4.5. Operating Conditions of USB PLL・I2S PLL (in the case of using main clock for input clock of PLL)	Revised the maximum of I2S PLL macro oscillation clock frequency. (307.2 MHz→384 MHz)
186	14.5.12-bit A/D Converter	Revised the minimum of Sampling time. Revised the characteristic of State transition time to operation permission Added AVRL in Analog reference voltage.
194	14.8.2. Interrupt of Low-Voltage Detection	Revised the SVHI values in Conditions

NOTE: Please see “Document History” about later revised information.