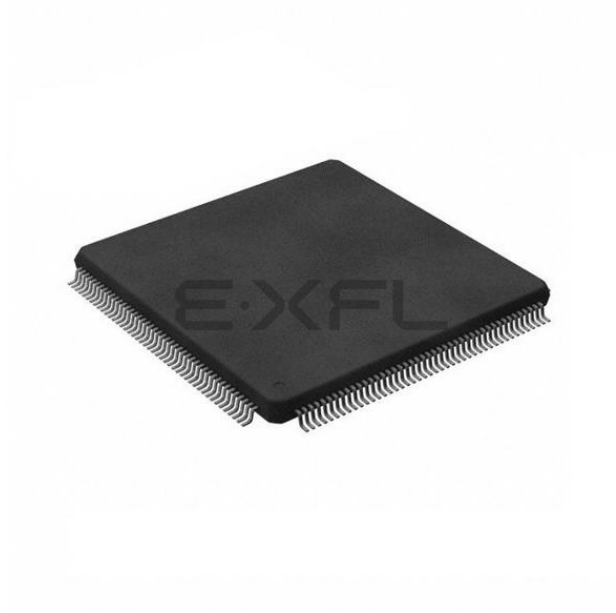

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CSIO, EBI/EMI, I²C, LINbus, SD, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	152
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2c39j0agv2000a

Notes:

- *All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use.*
- *See 12.4.3 Built-In CR Oscillation Characteristics for the accuracy of the built-in CR.*

2. Packages

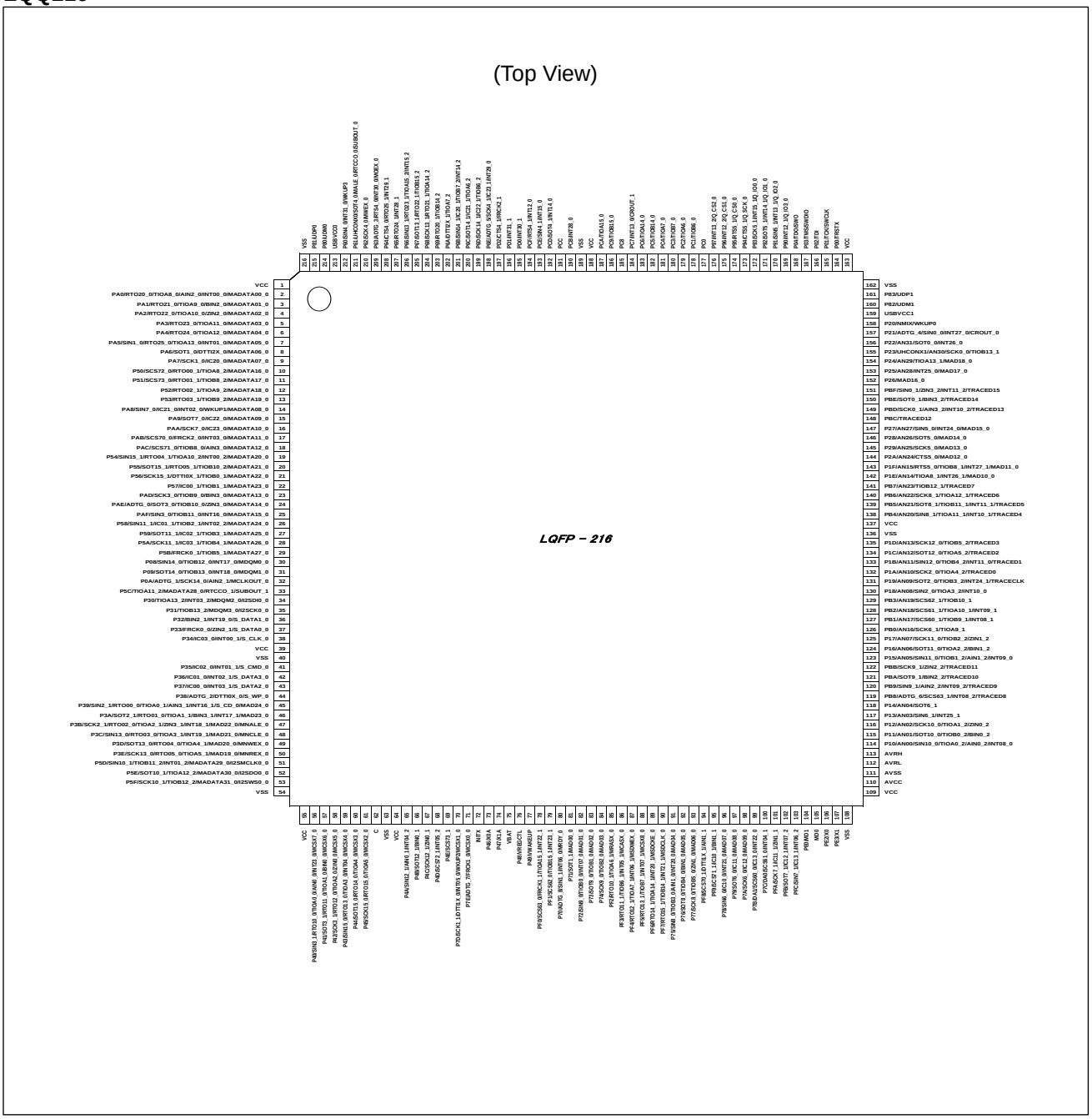
Package \ Product Name	S6E2C38H0A S6E2C39H0A S6E2C3AH0A	S6E2C38J0A S6E2C39J0A S6E2C3AJ0A	S6E2C38L0A S6E2C39L0A S6E2C3AL0A
LQFP: LQS144 (0.5-mm pitch)	❍	-	-
LQFP: LQP176 (0.5-mm pitch)	-	❍	-
BGA : LBE192 (0.8-mm pitch)	-	❍	-
LQFP: LQQ216 (0.4-mm pitch)	-	-	❍

❍: Supported

Note:

- *See 14. Package Dimensions for detailed information on each package.*

LQQ216



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
50	40	35	L1	P3E SCK13_0 (SCL13_0) RTO05_0 (PPG04_0) TIOA5_1 MAD19_0 MNREX_0	G	I
51	41	-	L2	P5D SIN10_1 TIOB11_2 INT01_2 MADATA29_0 I2SMCLK0_0	E	K
52	42	-	L3	P5E SOT10_1 (SDA10_1) TIOA12_2 MADATA30_0 I2SDO0_0	E	I
53	43	-	M2	P5F SCK10_1 (SCL10_1) TIOB12_2 MADATA31_0 I2SWS0_0	E	I
54	44	36	M1	VSS	-	-
55	45	37	N1	VCC	-	-
56	46	38	N2	P40 SIN3_1 RTO10_0 (PPG10_0) TIOA0_0 AIN0_0 INT23_0 MCSX7_0	G	K
57	47	39	N3	P41 SOT3_1 (SDA3_1) RTO11_0 (PPG10_0) TIOA1_0 BIN0_0 MCSX6_0	G	I
58	48	40	M3	P42 SCK3_1 (SCL3_1) RTO12_0 (PPG12_0) TIOA2_0 ZIN0_0 MCSX5_0	G	I

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
125	101	85	J11	P17 AN07 SCK11_0 (SCL11_0) TIOB2_2 ZIN1_2	F	L
126	102	-	J10	PB0 AN16 SCK6_1 (SCL6_1) TIOA9_1	F	L
127	103	-	J9	PB1 AN17 SCS60_1 TIOB9_1 INT08_1	F	M
128	104	-	H10	PB2 AN18 SCS61_1 TIOA10_1 INT09_1	F	M
129	105	-	J14	PB3 AN19 SCS62_1 TIOB10_1	F	L
130	106	86	H9	P18 AN08 SIN2_0 TIOA3_2 INT10_0	F	M
131	107	87	H12	P19 AN09 SOT2_0 (SDA2_0) TIOB3_2 INT24_1 TRACECLK	F	O
132	108	88	H14	P1A AN10 SCK2_0 (SCL2_0) TIOA4_2 TRACED0	F	N
133	109	89	G14	P1B AN11 SIN12_0 TIOB4_2 INT11_0 TRACED1	F	O
134	110	90	H13	P1C AN12 SOT12_0 (SDA12_0) TIOA5_2 TRACED2	F	N

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
158	128	104	C13	P20 NMIX WKUP0	I	F
159	129	105	E14	USBVCC1	-	-
160	130	106	D14	P82 UDM1	H	R
161	131	107	C14	P83 UDP1	H	R
162	132	108	B14	VSS	-	-
163	133	109	A13	VCC	-	-
164	134	110	B13	P00 TRSTX	E	G
165	135	111	A12	P01 TCK SWCLK	E	G
166	136	112	C12	P02 TDI	E	G
167	137	113	B12	P03 TMS SWDIO	E	G
168	138	114	B11	P04 TDO SWO	E	G
169	139	-	C11	P90 INT12_1 Q_IO3_0	S	K
170	140	-	D11	P91 SIN5_1 INT13_1 Q_IO2_0	S	K
171	141	-	B10	P92 SOT5_1 (SDA5_1) INT14_1 Q_IO1_0	S	K
172	142	-	C10	P93 SCK5_1 (SCL5_1) INT15_1 Q_IO0_0	S	K
173	143	-	D10	P94 CTS5_1 Q_SCK_0	S	I
174	144	-	B9	P95 RTS5_1 Q_CS0_0	S	I
175	-	-	-	P96 INT12_2 Q_CS1_0	S	K
176	-	-	-	P97 INT13_2 Q_CS2_0	S	K
177	145	115	C9	PC0	K	V

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Debugger	TRACED12	Trace data output pin of HTM	148	-	-	-
	TRACED13		149	-	-	-
	TRACED14		150	-	-	-
	TRACED15		151	-	-	-
	TRSTX	JTAG test reset Input pin	164	134	110	B13
External bus	MAD00_0	External bus interface address bus	81	66	56	J6
	MAD01_0		82	67	57	L8
	MAD02_0		83	68	58	K8
	MAD03_0		84	69	59	J8
	MAD04_0		91	76	60	K9
	MAD05_0		92	77	61	P10
	MAD06_0		93	78	62	N10
	MAD07_0		96	79	63	L10
	MAD08_0		97	80	64	K10
	MAD09_0		98	81	65	M10
	MAD10_0		142	116	92	G10
	MAD11_0		143	117	93	G9
	MAD12_0		144	118	94	F10
	MAD13_0		145	119	95	F11
	MAD14_0		146	120	96	F12
	MAD15_0		147	121	97	F13
	MAD16_0		152	122	98	E10
	MAD17_0		153	123	99	E11
	MAD18_0		154	124	100	E12
	MAD19_0		50	40	35	L1
	MAD20_0		49	39	34	K4
	MAD21_0		48	38	33	K3
	MAD22_0		47	37	32	K2
	MAD23_0		46	36	31	K1
	MAD24_0		45	35	30	J2
	MCSX0_0	External bus interface chip select output pin	71	56	48	M5
	MCSX1_0		70	55	47	L5
	MCSX2_0		61	51	43	N4
	MCSX3_0		60	50	42	M4
	MCSX4_0		59	49	41	L4
	MCSX5_0		58	48	40	M3
	MCSX6_0		57	47	39	N3
	MCSX7_0		56	46	38	N2
	MCSX8_0		88	73	-	P9

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	P30	General-purpose I/O port 3	34	24	-	G6
	P31		35	25	-	H4
	P32		36	26	21	H2
	P33		37	27	22	J1
	P34		38	28	23	H3
	P35		41	31	26	H6
	P36		42	32	27	J5
	P37		43	33	28	J4
	P38		44	34	29	J3
	P39		45	35	30	J2
	P3A		46	36	31	K1
	P3B		47	37	32	K2
	P3C		48	38	33	K3
	P3D		49	39	34	K4
	P3E		50	40	35	L1
	P40	General-purpose I/O port 4	56	46	38	N2
	P41		57	47	39	N3
	P42		58	48	40	M3
	P43		59	49	41	L4
	P44		60	50	42	M4
	P45		61	51	43	N4
	P46		73	58	50	P5
	P47		74	59	51	P6
	P48		76	61	53	N6
	P49		77	62	54	M6
	P4A		65	-	-	-
	P4B		66	-	-	-
	P4C		67	-	-	-
	P4D		68	-	-	-
	P4E		69	-	-	-

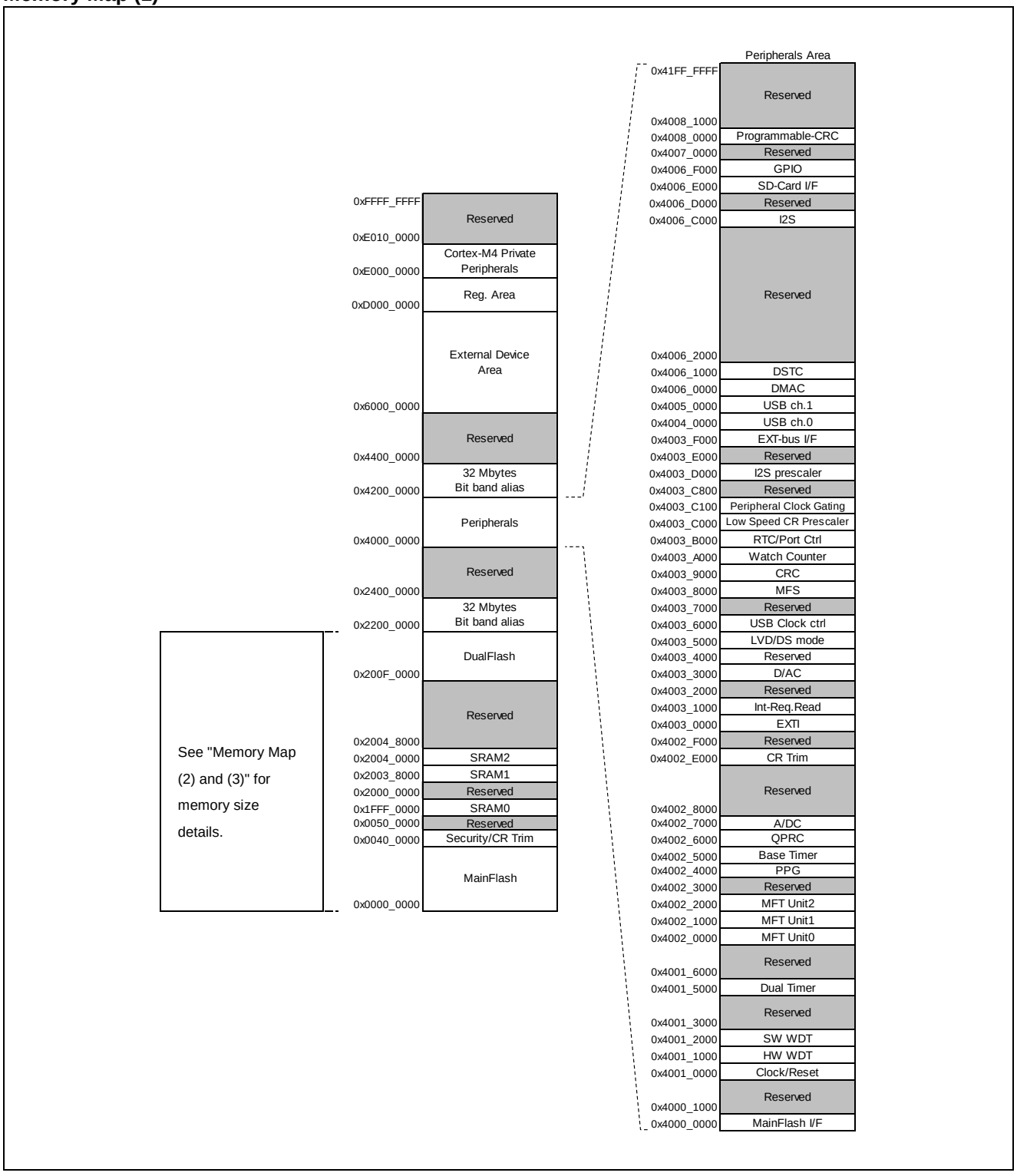
Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	P50	General-purpose I/O port 5	10	10	-	E2
	P51		11	11	-	E3
	P52		12	12	-	E4
	P53		13	-	-	-
	P54		19	-	-	-
	P55		20	-	-	-
	P56		21	-	-	-
	P57		22	-	-	-
	P58		26	-	-	-
	P59		27	-	-	-
	P5A		28	-	-	-
	P5B		29	-	-	-
	P5C		33	-	-	-
	P5D		51	41	-	L2
	P5E		52	42	-	L3
	P5F		53	43	-	M2
	P60	General-purpose I/O port 6	212	172	140	B3
	P61		211	171	139	C4
	P62		210	170	138	B4
	P63		209	169	137	C5
	P64		208	168	-	B5
	P65		207	167	-	E6
	P66		206	-	-	-
	P67		205	-	-	-
	P68		204	-	-	-
	P69		203	-	-	-
	P6A		202	-	-	-
	P6B		201	-	-	-
	P6C		200	-	-	-
	P6D		199	-	-	-
	P6E		198	166	136	D6

9. Memory Size

See Memory size in 1. Product Lineup to confirm the memory size.

10. Memory Map

Memory Map (1)



11. Pin Status in Each CPU State

The terms used for pin status have the following meanings:

- INITX = 0

  This is the period when the INITX pin is at the L level.

- INITX = 1

  This is the period when the INITX pin is at the H level.

- SPL = 0

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 0.

- SPL = 1

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 1.

- Input enabled

  Indicates that the input function can be used.

- Internal input fixed at 0

  This is the status that the input function cannot be used. Internal input is fixed at L.

- Hi-Z

  Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.

- Setting disabled

  Indicates that the setting is disabled.

- Maintain previous state

  Maintains the state that was immediately prior to entering the current mode.
  If a built-in peripheral function is operating, the output follows the peripheral function.
  If the pin is being used as a port, that output is maintained.

- Analog input is enabled

  Indicates that the analog input is enabled.

- Trace output

  Indicates that the trace function can be used.

- GPIO selected

  In Deep standby mode, pins switch to the general-purpose I/O port.

- Setting prohibition

  Prohibition of a setting by specification limitation

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC Mode or Deep Standby Stop mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
J	Analog output selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled	Maintain previous state	*2	*3	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	External interrupt enable selected					Maintain previous state	Maintain previous state			
	Resource other than above selected						Hi-Z/internal input fixed at 0			
	GPIO selected									
K	External interrupt enable selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled			Hi-Z/internal input fixed at 0			
	GPIO selected									
L	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	GPIO selected									

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC Mode or Deep Standby Stop mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
Q	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z/ WKUP input enabled	WKUP input enabled
	External interrupt enable selected							GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled			Hi-Z/internal input fixed at 0			
	GPIO selected									
R	GPIO selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	USB I/O pin	Setting disabled	Setting disabled	Setting disabled	Hi-Z at trans-mission/ input enabled/ internal input fixed at 0 at reception	Hi-Z at trans-mission/ input enabled/ internal input fixed at 0 at reception	Hi-Z at trans-mission/ input enabled/ internal input fixed at 0 at reception	Hi-Z/ input enabled	Hi-Z/ input enabled	Hi-Z/ input enabled

*1: Oscillation is stopped at sub Timer mode, sub CR Timer mode, RTC mode, Stop mode, Deep Standby RTC mode, and Deep Standby Stop mode.

*2: Maintain previous state at Timer mode. GPIO selected internal input fixed at 0 at RTC mode, Stop mode.

*3: Maintain previous state at Timer mode. Hi-Z/internal input fixed at 0 at RTC mode, Stop mode.

*4: It shows the case selected by EPFR14.E_SPLC register.

Package thermal resistance and maximum permissible power for each package are shown below.
The operation is guaranteed maximum permissible power or less for semiconductor devices.

Table for Package Thermal Resistance and Maximum Permissible Power

Package	Printed Circuit Board	Thermal Resistance θ_{JA} (°C/W)	Maximum Permissible Power (mW)	
			T_A = +85°C	T_A = +105°C
LQS144 (0.5-mm pitch)	Single-layered both sides	48	833	417
	4 layers	33	1212	606
LQP176 (0.5-mm pitch)	Single-layered both sides	45	889	444
	4 layers	31	1290	645
LQQ216 (0.4-mm pitch)	Single-layered both sides	46	870	435
	4 layers	32	1250	625
LBE192 (0.8-mm pitch)	Single-layered both sides	-	-	-
	4 layers	35	1143	571

WARNING:

1. *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.*
2. *Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.*
3. *No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet.*
4. *Users considering application outside the listed conditions are advised to contact their representatives beforehand.*

Table 12-3 Typical and Maximum Current Consumption in Normal Operation (PLL), Code with Data Accessing Running from Flash Memory (Flash 0 Wait-cycle Mode and Read Access 0 Wait)

Parameter	Symbol	Pin Name	Conditions		Frequency*4	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation *6,*7 (PLL)	*5	72 MHz	71	161	mA	*3 When all peripheral clocks are on
					60 MHz	62	150	mA	
					48 MHz	51	138	mA	
					36 MHz	40	125	mA	
					24 MHz	29	112	mA	
					12 MHz	17	98	mA	
					8 MHz	13	93	mA	
					4 MHz	8.4	88.5	mA	
				*5	72 MHz	46	132	mA	*3 When all peripheral clocks are off
					60 MHz	41	125	mA	
					48 MHz	34	118	mA	
					36 MHz	27	110	mA	
					24 MHz	20	102	mA	
					12 MHz	12	93	mA	
					8 MHz	9.4	89.7	mA	
					4 MHz	6.5	86.4	mA	

*1: T_A = +25°C, V_{CC} = 3.3 V

*2: T_J = +125°C, V_{CC} = 5.5 V

*3: When all ports are fixed

*4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK

*5: When operating flash 0 wait-cycle mode and read access 0 wait (FRWTR.RWT = 00, FBFCR.SD = 000)

*6: With data access to a MainFlash memory.

*7: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

12.4.4 Operating Conditions of Main PLL (in the Case of Using Main Clock for Input Clock of PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (lock up time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiplication rate	-	13	-	100	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	200	-	400	MHz	
Main PLL clock frequency*2	f_{CLKPLL}	-	-	200	MHz	

*1: Time from when the PLL starts operating until the oscillation stabilizes

*2: For more information about Main PLL clock (CLKPLL), see Chapter 2-1: Clock in FM4 Family Peripheral Manual Main Part (002-04856).

12.4.5 Operating Conditions of USB PLL・I²S PLL (in the Case of Using Main Clock for Input Clock of PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (lock up time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiplication rate	-	13	-	100	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	200	-	400	MHz	USB
				384	MHz	I²S
USB clock frequency *2	f_{CLKPLL}	-	-	50	MHz	After the M frequency division
I²S clock frequency *3	f_{CLKPLL}	-	-	12.288	MHz	After the M frequency division

*1: Time from when the PLL starts operating until the oscillation stabilizes

*2: For more information about USB/Ethernet clock, see Chapter 2-2: USB/Ethernet Clock Generation in FM4 Family Peripheral Manual Communication Macro Part (002-04862).

*3: For more information about I²S clock, see Chapter 7-1: I²S Clock Generation in FM4 Family Peripheral Manual Communication Macro Part (002-04862).

High-Speed Mode

■Clock CLK (All values are referred to V_{IH} and V_{IL})

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Clock frequency Data Transfer Mode	f_{PP}	S_CLK	C_{CARD} ≤ 10 pF (1 card)	0	50	MHz
Clock low time	t_{WL}	S_CLK		7	-	ns
Clock high time	t_{WH}	S_CLK		7	-	ns
Clock rise time	t_{TLH}	S_CLK		-	3	ns
Clock fall time	t_{THL}	S_CLK		-	3	ns

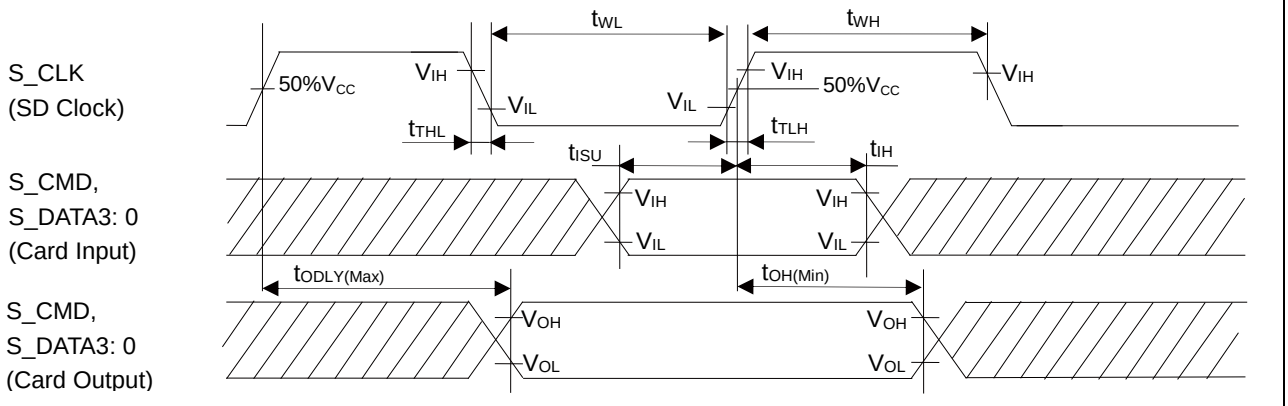
■Card Inputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Input set-up time	t_{ISU}	S_CMD, S_DATA3: 0	C_{CARD} ≤ 10 pF (1 card)	6	-	ns
Input hold time	t_{IH}	S_CMD, S_DATA3: 0		2	-	ns

■Card Outputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Output delay time during data transfer mode	t_{ODLY}	S_CMD, S_DATA3: 0	C_L ≤ 40 pF (1 card)	0	14	ns
Output hold time	t_{OH}	S_CMD, S_DATA3: 0	C_L ≥ 15 pF (1 card)	2.5	-	ns
Total system capacitance for each line*	C_L	-	1 card	-	40	pF

*: In order to satisfy severe timing, host shall drive only one card.



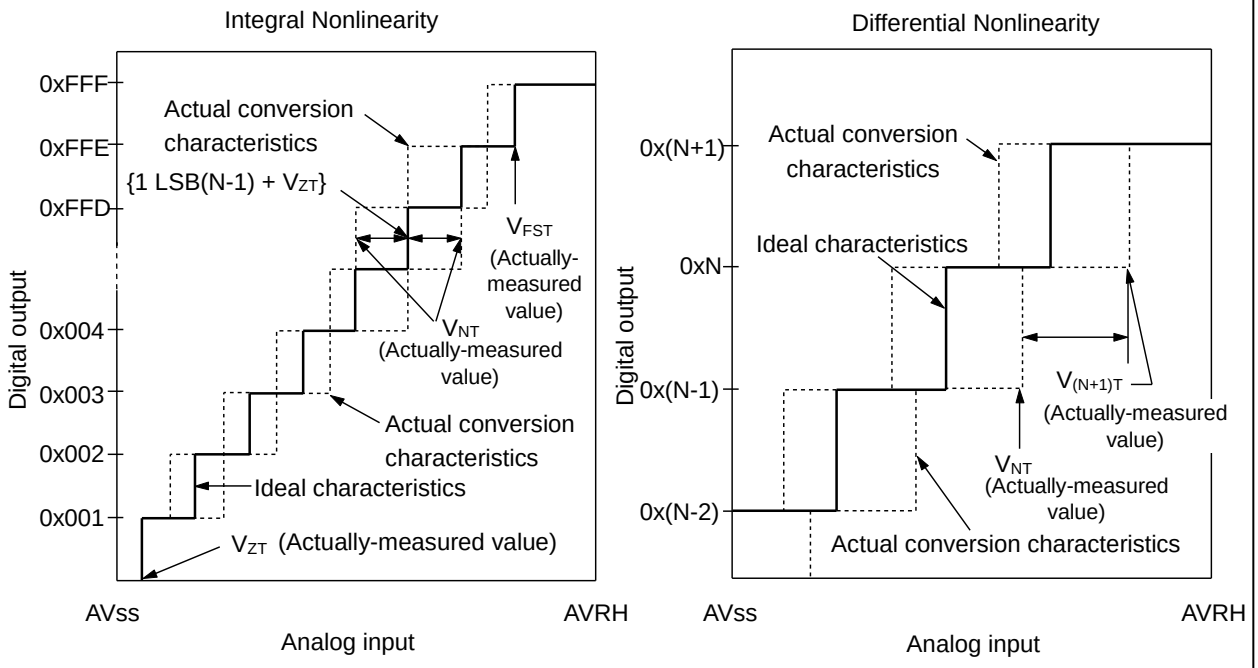
High-Speed Mode

Notes:

- *The Card Input corresponds to the Host Output and the Card Output corresponds to the Host Input because this model is the Host.*
- *For more information about clock frequency (f_{PP}), see Chapter 15: SD card Interface in FM4 Family Peripheral Manual Main Part (002-04856).*

Definition of 12-bit A/D Converter Terms

- Resolution: Analog variation that is recognized by an A/D converter.
- Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.
- Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N: A/D converter digital output value.
V_{ZT}: Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST}: Voltage at which the digital output changes from 0xFFE to 0xFFF.
V_{NT}: Voltage at which the digital output changes from 0x(N − 1) to 0xN.

12.6 12-bit D/A Converter

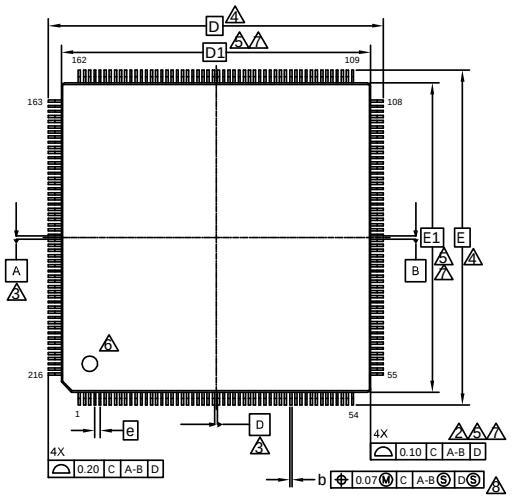
Electrical Characteristics for the D/A Converter

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V)

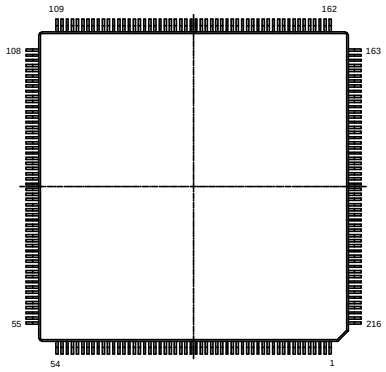
Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	DAx	-	-	12	bit	
Conversion time	t_{C20}		0.56	0.69	0.81	µs	Load 20 pF
	t_{C100}		2.79	3.42	4.06	µs	Load 100 pF
Integral nonlinearity *	INL		- 16	-	+ 16	LSB	
Differential nonlinearity *	DNL		- 0.98	-	+ 1.5	LSB	
Output voltage offset	V_{OFF}		-	-	+ 10	mV	When setting 0x000
			- 20.0	-	+ 1.4	mV	When setting 0xFFF
Analog output impedance	R_O		3.10	3.80	4.50	kΩ	D/A operation
			2.0	-	-	MΩ	When D/A stop
Power supply current *	IDDA	AVCC	260	330	410	µs	D/A 1ch operation AV_{CC} = 3.3 V
			400	510	620	µs	D/A 1ch operation AV_{CC} = 5.0 V
	IDSA		-	-	14	µs	When D/A stop

*: During no load

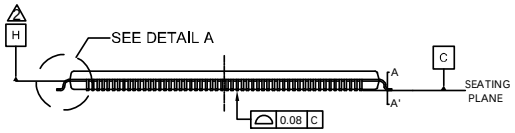
Package Type	Package Code
LQFP 216	LQQ 216



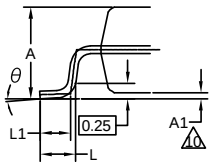
TOP VIEW



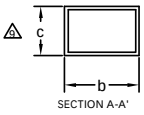
BOTTOM VIEW



SIDE VIEW



DETAIL A



SECTION A-A'

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.13	0.18	0.23
c	0.09	—	0.20
D	26.00 BSC.		
D1	24.00 BSC.		
e	0.40 BSC		
E	26.00 BSC.		
E1	24.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-15153 **

PACKAGE OUTLINE, 216 LEAD LQFP
24.0X24.0X1.7 MM LQQ216 REV**

Document History

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Document Number: 002-04988

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	AKIH	04/22/2015	New Spec.
*A	5126421	HITK	02/05/2016	Company name and layout design change. Added the note of TAP pin. Updated Package Code and Dimensions (LQFP-144, LQFP-176, LQFP-216).
*B	5634625	YSKA	02/20/2017	Deleted CAN in communications interfaces. (Page 1) Deleted CAN(RX0_2, TX0_2) in LQQ216 pin assignments (Page 12) Deleted RX2_0 in P7D in “4. Pin Descriptions” (Page 20) Updated 12.4.8 Power-On Reset Timing. Changed parameter from “Power Supply rise time(t_{VCCR})[ms]” to “Power ramp rate(dV/dt)[mV/us]” and add some comments. (Page 113) Modified CSIO timing typo (12.4.12 CSIO(SPI) Timing) Deleted “SPI=1, MS=0” in the titles and added MS=0,1 in the schematic (Page 134-141, 150-157) Modified RTC description(Features, Real-Time Clock(RTC)) Deleted “second , or day of the week” in the Interrupt function.(Page 3) Modifications related to the VBAT in the following chapter. “7. Handling Devices” Notes on Power-on (Page 76) “11. Pin Status in Each CPU State” List of VBAT Domain Pin Status (Page 90) “12.3.1 Current Rating” Table12-9. Typical and Maximum Current Consumption in Deep Standby STOP Mode, Deep Standby RTC Mode and VBAT (Page 105) Deleted MPNs below from “13. Ordering Information” (Page 190) S6E2C38H0AGV20000, S6E2C38J0AGB10000, S6E2C38J0AGV20000, S6E2C38L0AGL20000, S6E2C39H0AGV20000, S6E2C39J0AGB10000, S6E2C39J0AGV20000, S6E2C39L0AGL20000, S6E2C3AH0AGV20000, S6E2C3AJ0AGB10000, S6E2C3AJ0AGV20000, S6E2C3AL0AGL20000 Added MPNs below to “13. Ordering Information” (Page 190) S6E2C38H0AGV2000A, S6E2C38J0AGB1000A, S6E2C38J0AGV2000A, S6E2C38L0AGL2000A, S6E2C39H0AGV2000A, S6E2C39J0AGB1000A, S6E2C39J0AGV2000A, S6E2C39L0AGL2000A, S6E2C3AH0AGV2000A, S6E2C3AJ0AGB1000A, S6E2C3AJ0AGV2000A, S6E2C3AL0AGL2000A Deleted Baud rate spec for High-Speed Synchronous Serial in “12.4.12 CSIO(SPI) Timing”(Page 142-148) Modified the expression of the “Built-in CR” and add Note in the “1. Product Lineup”(Page 8) Modified typo(SCLKx_0 -> SCKx_0)(Page 126, 128, 130, 132) Change the name from “USB Function” to “USB Device” (Page 1, 8, 58) Added Maximum Access size in “Features”(Page 1) Updated IO circuit (type A) (Page 62)