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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CSIO, EBI/EMI, I²C, LINbus, SD, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	120
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2c3ah0agv2000a

Multi-function Serial Interface (Max 16 channels)

- Separate 64 byte receive and transmit FIFO buffers for channels 0 to 7.
- Operation mode is selectable for each channel from the following:
  - UART
  - CSIO (SPI)
  - LIN
  - I^2C
- UART
  - Full-duplex double buffer
  - Selection with or without parity supported
  - Built-in dedicated baud rate generator
  - External clock available as a serial clock
  - Various error detect functions available (parity errors, framing errors, and overrun errors)
- CSIO (SPI)
  - Full-duplex double buffer
  - Built-in dedicated baud rate generator
  - Overrun error detect function available
  - Serial chip select function (ch 6 and ch 7 only)
  - Supports high-speed SPI (ch 4 and ch 6 only)
  - Data length 5 to 16-bit
- LIN
  - LIN protocol Rev.2.1 supported
  - Full-duplex double buffer
  - Master/slave mode supported
  - LIN break field generation (can change to 13- to 16-bit length)
  - LIN break delimiter generation (can change to 1- to 4-bit length)
  - Various error detect functions available (parity errors, framing errors, and overrun errors)
- I^2C
  - Standard mode (Max 100 kbps)/Fast mode (Max 400 kbps) supported
  - Fast mode Plus (Fm+) (Max 1000 kbps, only for ch 3 = ch A and ch 7 = ch B) supported

DMA Controller (Eight channels)

DMA controller has an independent bus, so the CPU and DMA controller can process simultaneously.

- Eight independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32-bit (4 GB)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: bytes/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

DSTC (Descriptor System data Transfer Controller; 256 Channels)

The DSTC can transfer data at high-speed without going via the CPU. The DSTC adopts the descriptor system and, following the specified contents of the descriptor that has already been constructed on the memory, can access directly the memory/peripheral device and perform the data-transfer operation.

It supports the software activation, the hardware activation, and the chain activation functions.

A/D Converter (Max 32 channels)

- 12-bit A/D Converter
  - Successive approximation type
  - Built-in three units
  - Conversion time: 0.5 µs at 5 V
  - Priority conversion available (priority at two levels)
  - Scanning conversion mode
  - Built-in FIFO for conversion data storage (for SCAN conversion: 16 steps, for priority conversion: 4 steps)

D/A Converter (Max 2 Channels)

- R-2R type
- 12-bit resolution

Base Timer (Max 16 Channels)

Operation mode is selected from the following for each channel:

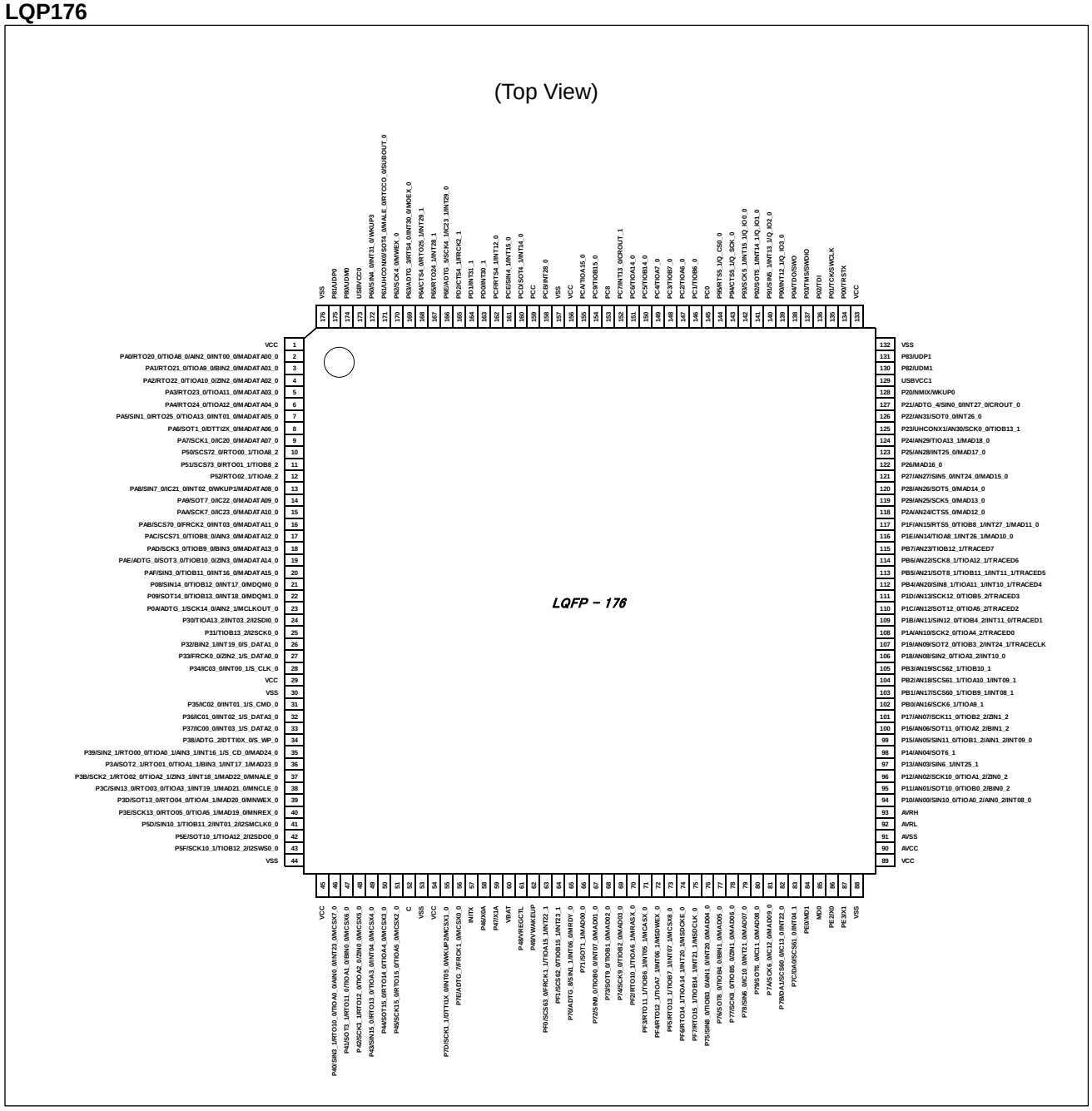
- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

General Purpose I/O Port

This series can use its pins as general purpose I/O ports when they are not used for external bus or peripherals; moreover, the port relocate function is built in. It can set the I/O port to which the peripheral function can be allocated.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in port-relocate function
- Up to 120 high-speed general-purpose I/O ports in 144 pin package
- Some pins 5V tolerant I/O.
  See 4. Pin Descriptions and 5. I/O Circuit Type for the corresponding pins.

LQP176



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
42	32	27	J5	P36 IC01_0 INT02_1 S_DATA3_0	L	K
43	33	28	J4	P37 IC00_0 INT03_1 S_DATA2_0	L	K
44	34	29	J3	P38 ADTG_2 DTTI0X_0 S_WP_0	E	I
45	35	30	J2	P39 SIN2_1 RTO00_0 (PPG00_0) TIOA0_1 AIN3_1 INT16_1 S_CD_0 MAD24_0	G	K
46	36	31	K1	P3A SOT2_1 (SDA2_1) RTO01_0 (PPG00_0) TIOA1_1 BIN3_1 INT17_1 MAD23_0	G	K
47	37	32	K2	P3B SCK2_1 (SCL2_1) RTO02_0 (PPG02_0) TIOA2_1 ZIN3_1 INT18_1 MAD22_0 MNALE_0	G	K
48	38	33	K3	P3C SIN13_0 RTO03_0 (PPG02_0) TIOA3_1 INT19_1 MAD21_0 MNCLE_0	G	K
49	39	34	K4	P3D SOT13_0 (SDA13_0) RTO04_0 (PPG04_0) TIOA4_1 MAD20_0 MNWEX_0	G	I

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
50	40	35	L1	P3E SCK13_0 (SCL13_0) RTO05_0 (PPG04_0) TIOA5_1 MAD19_0 MNREX_0	G	I
51	41	-	L2	P5D SIN10_1 TIOB11_2 INT01_2 MADATA29_0 I2SMCLK0_0	E	K
52	42	-	L3	P5E SOT10_1 (SDA10_1) TIOA12_2 MADATA30_0 I2SDO0_0	E	I
53	43	-	M2	P5F SCK10_1 (SCL10_1) TIOB12_2 MADATA31_0 I2SWS0_0	E	I
54	44	36	M1	VSS	-	-
55	45	37	N1	VCC	-	-
56	46	38	N2	P40 SIN3_1 RTO10_0 (PPG10_0) TIOA0_0 AIN0_0 INT23_0 MCSX7_0	G	K
57	47	39	N3	P41 SOT3_1 (SDA3_1) RTO11_0 (PPG10_0) TIOA1_0 BIN0_0 MCSX6_0	G	I
58	48	40	M3	P42 SCK3_1 (SCL3_1) RTO12_0 (PPG12_0) TIOA2_0 ZIN0_0 MCSX5_0	G	I

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
199	-	-	-	P6D SCK14_1 (SCL14_1) IC22_1 TIOB6_2	E	I
200	-	-	-	P6C SOT14_1 (SDA14_1) IC21_1 TIOA6_2	E	I
201	-	-	-	P6B SIN14_1 IC20_1 TIOB7_2 INT14_2	E	K
202	-	-	-	P6A DTTI2X_1 TIOA7_2	E	I
203	-	-	-	P69 RTO20_1 (PPG20_1) TIOB14_2	E	I
204	-	-	-	P68 SCK13_1 (SCL13_0) RTO21_1 (PPG20_1) TIOA14_2	E	I
205	-	-	-	P67 SOT13_1 (SDA13_1) RTO22_1 (PPG22_1) TIOB15_2	E	I
206	-	-	-	P66 SIN13_1 RTO23_1 (PPG22_1) TIOA15_2 INT15_2	E	K
207	167	-	E6	P65 RTO24_1 (PPG24_1) INT28_1	E	K
208	168	-	B5	P64 CTS4_0 RTO25_1 (PPG24_1) INT29_1	I	K
209	169	137	C5	P63 ADTG_3 RTS4_0 INT30_0 MOEX_0	L	K

Signal Descriptions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.

Use the extended port function register (EPFR) to select the pin.

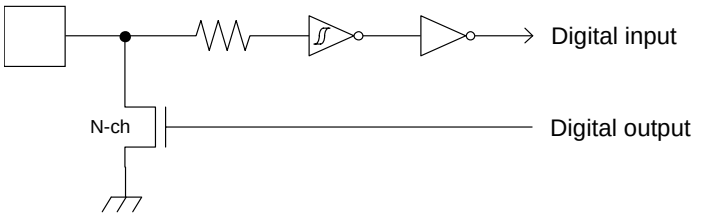
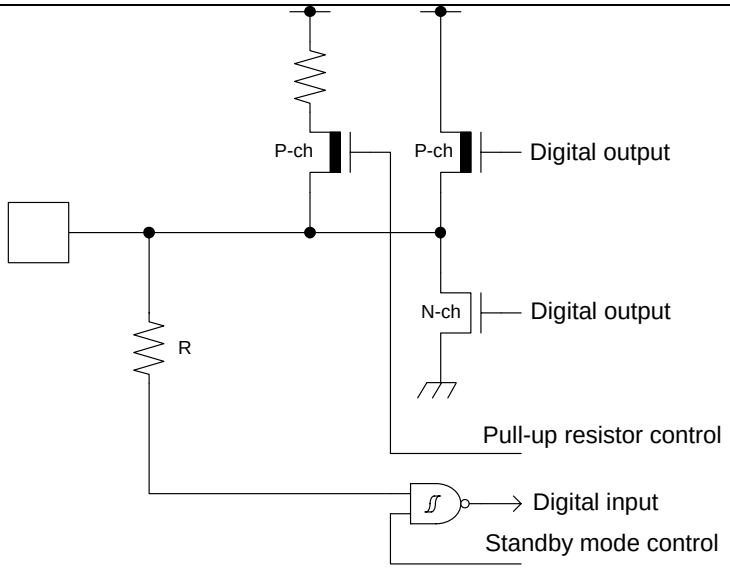
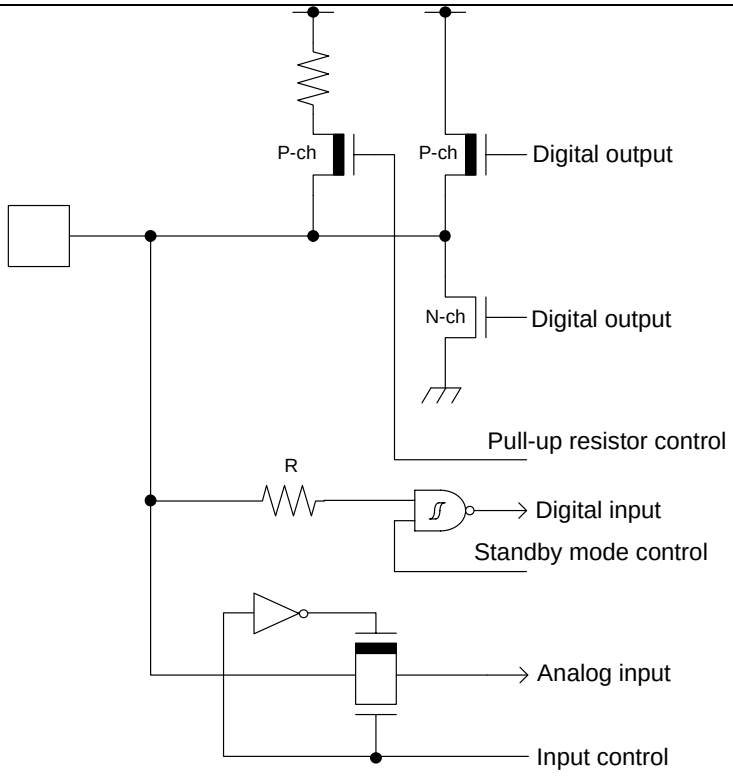
Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
A/D converter	ADTG_0	A/D converter external trigger input pin	24	19	16	F6
	ADTG_1		32	23	20	G5
	ADTG_2		44	34	29	J3
	ADTG_3		209	169	137	C5
	ADTG_4		157	127	103	D13
	ADTG_5		198	166	136	D6
	ADTG_6		119	-	-	-
	ADTG_7		71	56	48	M5
	ADTG_8		80	65	55	L6
	AN00	A/D converter analog input pin. ANxx describes A/D converter ch xx.	114	94	78	L11
	AN01		115	95	79	K13
	AN02		116	96	80	K12
	AN03		117	97	81	K14
	AN04		118	98	82	K11
	AN05		123	99	83	J13
	AN06		124	100	84	J12
	AN07		125	101	85	J11
	AN08		130	106	86	H9
	AN09		131	107	87	H12
	AN10		132	108	88	H14
	AN11		133	109	89	G14
	AN12		134	110	90	H13
	AN13		135	111	91	H11
	AN14		142	116	92	G10
	AN15		143	117	93	G9
	AN16		126	102	-	J10
	AN17		127	103	-	J9
	AN18		128	104	-	H10
	AN19		129	105	-	J14
	AN20		138	112	-	G13
	AN21		139	113	-	F14
	AN22		140	114	-	G12
	AN23		141	115	-	G11
	AN24		144	118	94	F10
	AN25		145	119	95	F11
	AN26		146	120	96	F12
	AN27		147	121	97	F13
	AN28		153	123	99	E11
	AN29		154	124	100	E12
	AN30		155	125	101	E13
	AN31		156	126	102	D12

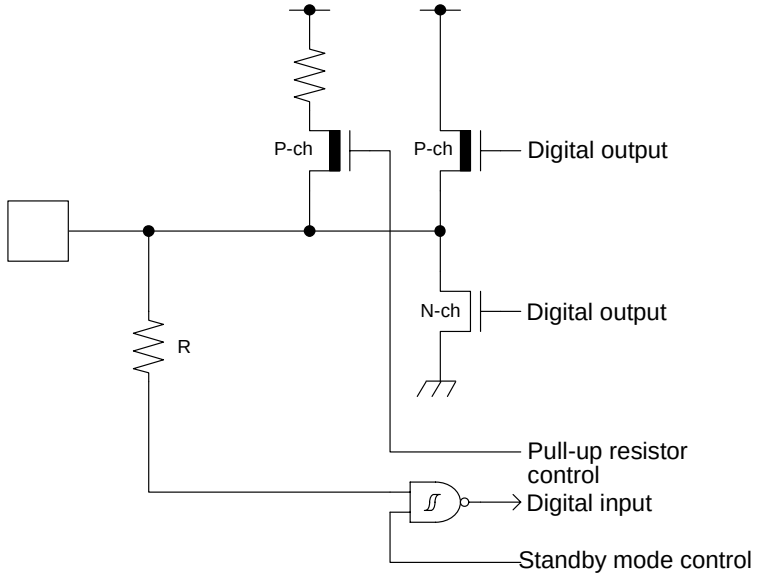
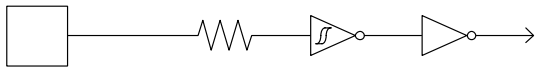
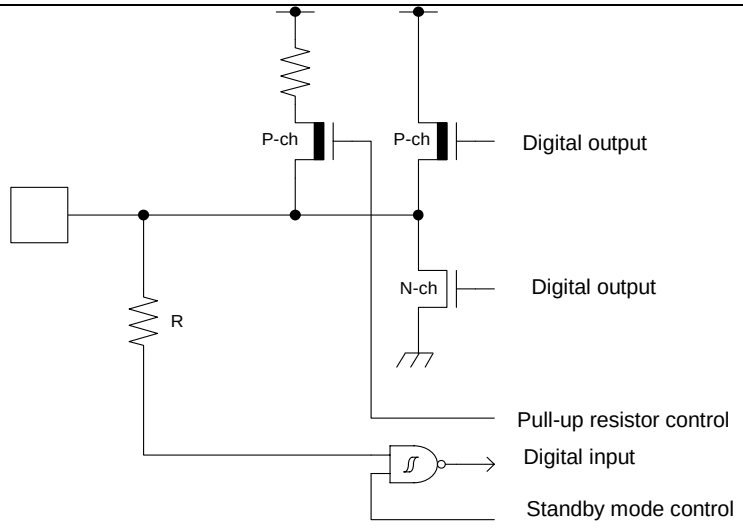
Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Base Timer 0	TIOA0_0	Base Timer ch 0 TIOA pin	56	46	38	N2
	TIOA0_1		45	35	30	J2
	TIOA0_2		114	94	78	L11
	TIOB0_0	Base Timer ch 0 TIOB pin	82	67	57	L8
	TIOB0_1		21	-	-	-
	TIOB0_2		115	95	79	K13
Base Timer 1	TIOA1_0	Base Timer ch 1 TIOA pin	57	47	39	N3
	TIOA1_1		46	36	31	K1
	TIOA1_2		116	96	80	K12
	TIOB1_0	Base Timer ch 1 TIOB pin	83	68	58	K8
	TIOB1_1		22	-	-	-
	TIOB1_2		123	99	83	J13
Base Timer 2	TIOA2_0	Base Timer ch 2 TIOA pin	58	48	40	M3
	TIOA2_1		47	37	32	K2
	TIOA2_2		124	100	84	J12
	TIOB2_0	Base Timer ch 2 TIOB pin	84	69	59	J8
	TIOB2_1		26	-	-	-
	TIOB2_2		125	101	85	J11
Base Timer 3	TIOA3_0	Base Timer ch 3 TIOA pin	59	49	41	L4
	TIOA3_1		48	38	33	K3
	TIOA3_2		130	106	86	H9
	TIOB3_0	Base Timer ch 3 TIOB pin	91	76	60	K9
	TIOB3_1		27	-	-	-
	TIOB3_2		131	107	87	H12
Base Timer 4	TIOA4_0	Base Timer ch 4 TIOA pin	60	50	42	M4
	TIOA4_1		49	39	34	K4
	TIOA4_2		132	108	88	H14
	TIOB4_0	Base Timer ch 4 TIOB pin	92	77	61	P10
	TIOB4_1		28	-	-	-
	TIOB4_2		133	109	89	G14
Base Timer 5	TIOA5_0	Base Timer ch 5 TIOA pin	61	51	43	N4
	TIOA5_1		50	40	35	L1
	TIOA5_2		134	110	90	H13
	TIOB5_0	Base Timer ch 5 TIOB pin	93	78	62	N10
	TIOB5_1		29	-	-	-
	TIOB5_2		135	111	91	H11
Base Timer 6	TIOA6_0	Base Timer ch 6 TIOA pin	179	147	117	D9
	TIOA6_1		85	70	-	N8
	TIOA6_2		200	-	-	-
	TIOB6_0	Base Timer ch 6 TIOB pin	178	146	116	B8
	TIOB6_1		86	71	-	M8
	TIOB6_2		199	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	P00	General-purpose I/O port 0	164	134	110	B13
	P01		165	135	111	A12
	P02		166	136	112	C12
	P03		167	137	113	B12
	P04		168	138	114	B11
	P08		30	21	18	G3
	P09		31	22	19	G4
	P0A		32	23	20	G5
	P10	General-purpose I/O port 1	114	94	78	L11
	P11		115	95	79	K13
	P12		116	96	80	K12
	P13		117	97	81	K14
	P14		118	98	82	K11
	P15		123	99	83	J13
	P16		124	100	84	J12
	P17		125	101	85	J11
	P18		130	106	86	H9
	P19		131	107	87	H12
	P1A		132	108	88	H14
	P1B		133	109	89	G14
	P1C		134	110	90	H13
	P1D		135	111	91	H11
	P1E		142	116	92	G10
	P1F		143	117	93	G9
	P20	General-purpose I/O port 2	158	128	104	C13
	P21		157	127	103	D13
	P22		156	126	102	D12
	P23		155	125	101	E13
	P24		154	124	100	E12
	P25		153	123	99	E11
	P26		152	122	98	E10
	P27		147	121	97	F13
	P28		146	120	96	F12
	P29		145	119	95	F11
	P2A		144	118	94	F10

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Serial 12	SIN12_0	Multi-function serial interface ch 12 input pin	133	109	89	G14
	SIN12_1		65	-	-	-
	SOT12_0 (SDA12_0)	Multi-function serial interface ch 12 output pin. This pin operates as SOT12 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA12 when it is used in an I²C (operation mode 4).	134	110	90	H13
	SOT12_1 (SDA12_1)		66	-	-	-
	SCK12_0 (SCL12_0)	Multi-function serial interface ch 12 clock I/O pin. This pin operates as SCK12 when it is used in a CSIO (operation mode 2) and as SCL12 when it is used in an I²C (operation mode 4).	135	111	91	H11
	SCK12_1 (SCL12_1)		67	-	-	-
Multi-Function Serial 13	SIN13_0	Multi-function serial interface ch 13 input pin	48	38	33	K3
	SIN13_1		206	-	-	-
	SOT13_0 (SDA13_0)	Multi-function serial interface ch 13 output pin. This pin operates as SOT13 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA13 when it is used in an I²C (operation mode 4).	49	39	34	K4
	SOT13_1 (SDA13_1)		205	-	-	-
	SCK13_0 (SCL13_0)	Multi-function serial interface ch 13 clock I/O pin. This pin operates as SCK13 when it is used in a CSIO (operation mode 2) and as SCL13 when it is used in an I²C (operation mode 4).	50	40	35	L1
	SCK13_1 (SCL13_1)		204	-	-	-
Multi-Function Serial 14	SIN14_0	Multi-function serial interface ch 14 input pin	30	21	18	G3
	SIN14_1		201	-	-	-
	SOT14_0 (SDA14_0)	Multi-function serial interface ch 14 output pin. This pin operates as SOT14 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA14 when it is used in an I²C (operation mode 4).	31	22	19	G4
	SOT14_1 (SDA14_1)		200	-	-	-
	SCK14_0 (SCL14_0)	Multi-function serial interface ch 14 clock I/O pin. This pin operates as SCK14 when it is used in a CSIO (operation mode 2) and as SCL14 when it is used in an I²C (operation mode 4).	32	23	20	G5
	SCK14_1 (SCL14_1)		199	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Timer 2	DTTI2X_0	Input signal controlling waveform generator outputs RTO20 to RTO25 of Multi-Function Timer 1.	8	8	8	D3
	DTTI2X_1		202	-	-	-
	FRCK2_0	16-bit free-run timer ch 2 external clock input pin	17	16	13	F3
	FRCK2_1		197	165	135	C6
	IC20_0	16-bit input capture input pin of Multi-Function Timer 2. ICxx describes channel number.	9	9	9	D4
	IC20_1		201	-	-	-
	IC21_0		14	13	10	E5
	IC21_1		200	-	-	-
	IC22_0		15	14	11	F1
	IC22_1		199	-	-	-
	IC23_0		16	15	12	F2
	IC23_1		198	166	136	D6
	RTO20_0 (PPG20_0)	Waveform generator output pin of Multi-Function Timer 2. This pin operates as PPG20 when it is used in PPG2 output modes.	2	2	2	B2
	RTO20_1 (PPG20_1)		203	-	-	-
	RTO21_0 (PPG20_0)	Waveform generator output pin of Multi-Function Timer 2. This pin operates as PPG20 when it is used in PPG2 output modes.	3	3	3	C2
	RTO21_1 (PPG20_1)		204	-	-	-
	RTO22_0 (PPG22_0)	Waveform generator output pin of Multi-Function Timer 2. This pin operates as PPG22 when it is used in PPG2 output modes.	4	4	4	C3
	RTO22_1 (PPG22_1)		205	-	-	-
	RTO23_0 (PPG22_0)	Waveform generator output pin of Multi-Function Timer 2. This pin operates as PPG22 when it is used in PPG2 output modes.	5	5	5	D5
	RTO23_1 (PPG22_1)		206	-	-	-
	RTO24_0 (PPG24_0)	Waveform generator output pin of Multi-Function Timer 2. This pin operates as PPG24 when it is used in PPG2 output modes.	6	6	6	D2
	RTO24_1 (PPG24_1)		207	167	-	E6
	RTO25_0 (PPG24_0)	Waveform generator output pin of Multi-Function Timer 2. This pin operates as PPG24 when it is used in PPG2 output modes.	7	7	7	D1
	RTO25_1 (PPG24_1)		208	168	-	B5

Type	Circuit	Remarks
C		• Open drain output • CMOS level hysteresis input
E		• CMOS level output • CMOS level hysteresis input • Pull-up resistor control • Standby mode control • Pull-up resistor: approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.
F		• CMOS level output • CMOS level hysteresis input • Input control • Analog input • Pull-up resistor control • Standby mode control • Pull-up resistor: approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.

Type	Circuit	Remarks
I		・ CMOS level output ・ CMOS level hysteresis input ・ 5V tolerant ・ Pull-up resistor control ・ Standby mode control ・ Pull-up resistor: approximately 50 kΩ ・ I_{OH} = -4 mA, I_{OL} = 4 mA ・ Available to control of PZR registers (pseudo-open drain control) ・ For PZR registers, refer to GPIO in the “FM4 Family Peripheral Manual Main Part (002-04856)”.
J		CMOS level hysteresis input
K		・ CMOS level output ・ TTL level hysteresis input ・ Pull-up resistor control ・ Standby mode control ・ Pull-up resistor: approximately 50 kΩ ・ I_{OH} = -4mA, I_{OL} = 4mA

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC Mode or Deep Standby Stop mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
J	Analog output selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled	Maintain previous state	*2	*3	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	External interrupt enable selected					Maintain previous state	Maintain previous state			
	Resource other than above selected						Hi-Z/internal input fixed at 0			
	GPIO selected									
K	External interrupt enable selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled			Hi-Z/internal input fixed at 0			
	GPIO selected									
L	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	GPIO selected									

Package thermal resistance and maximum permissible power for each package are shown below.
The operation is guaranteed maximum permissible power or less for semiconductor devices.

Table for Package Thermal Resistance and Maximum Permissible Power

Package	Printed Circuit Board	Thermal Resistance θ_{JA} (°C/W)	Maximum Permissible Power (mW)	
			T_A = +85°C	T_A = +105°C
LQS144 (0.5-mm pitch)	Single-layered both sides	48	833	417
	4 layers	33	1212	606
LQP176 (0.5-mm pitch)	Single-layered both sides	45	889	444
	4 layers	31	1290	645
LQQ216 (0.4-mm pitch)	Single-layered both sides	46	870	435
	4 layers	32	1250	625
LBE192 (0.8-mm pitch)	Single-layered both sides	-	-	-
	4 layers	35	1143	571

WARNING:

1. *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.*
2. *Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.*
3. *No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet.*
4. *Users considering application outside the listed conditions are advised to contact their representatives beforehand.*

Calculation Method of Power Dissipation (Pd)

The power dissipation is shown in the following formula.

$$Pd = V_{CC} \times I_{CC} + \Sigma (I_{OL} \times V_{OL}) + \Sigma ((V_{CC}-V_{OH}) \times (-I_{OH}))$$

I_{OL}: L level output current
I_{OH}: H level output current
V_{OL}:L level output voltage
V_{OH}:H level output voltage

I_{CC} is the current drawn by the device.
It can be analyzed as follows.

$$I_{CC} = I_{CC}(INT) + \Sigma I_{CC}(IO)$$

I_{CC} (INT): Current drawn by internal logic and memory, etc. through the regulator

ΣI_{CC} (IO): Sum of current (I/O switching current) drawn by the output pin

For I_{CC} (INT), it can be anticipated by (1) Current Rating in 12.3. DC Characteristics (This rating value does not include I_{CC} (IO) for a value at pin fixed).
For Icc (IO), it depends on system used by customers.
The calculation formula is shown below.

$$I_{CC}(IO) = (C_{INT} + C_{EXT}) \times V_{CC} \times f_{SW}$$

C_{INT}: Pin internal load capacitance
C_{EXT}: External load capacitance of output pin
f_{SW}: Pin switching frequency

Parameter	Symbol	Conditions	Capacitance Value
Pin internal load capacitance	C_{INT}	4 mA type	1.93 pF
		8 mA type	3.45 pF
		12 mA type	3.42 pF

Calculate I_{CC} (Max) as follows when the power dissipation can be evaluated by yourself:

Measure current value I_{CC} (Typ) at normal temperature (+25°C).

Add maximum leakage current value I_{CC} (leak_max) at operating on a value in (1).

$$I_{CC}(Max) = I_{CC}(Typ) + I_{CC}(leak\_max)$$

Parameter	Symbol	Conditions	Current Value
Maximum leakage current at operating	I_{CC} (leak_max)	T_J = +125°C	79.2 mA
		T_J = +105°C	39.4 mA
		T_J = +85°C	26.5 mA

Table 12-7 Typical and Maximum Current Consumption in Sleep Operation (Other Than PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK/2

Parameter	Symbol	Pin Name	Conditions	Frequency*4	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCS}	VCC	Sleep operation*5 (main oscillation)	4 MHz	3.4	82.6	mA	*3 When all peripheral clocks are on
					2.5	81.7	mA	*3 When all peripheral clocks are off
			Sleep operation (built-in High-speed CR)	4 MHz	2.5	81.7	mA	*3 When all peripheral clocks are on
					1.7	80.9	mA	*3 When all peripheral clocks are off
			Sleep operation*6 (sub oscillation)	32 kHz	0.75	79.97	mA	*3 When all peripheral clocks are on
					0.74	79.96	mA	*3 When all peripheral clocks are off
			Sleep operation (built-in low-speed CR)	100 kHz	0.79	80.01	mA	*3 When all peripheral clocks are on
					0.76	79.98	mA	*3 When all peripheral clocks are off

*1: T_A = +25°C, V_{CC} = 3.3 V

*2: T_J = +125°C, V_{CC} = 5.5 V

*3: When all ports are fixed.

*4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK/2

*5: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

*6: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)

When Using Synchronous Serial Chip Select (SCINV = 1, CSLVL = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	ns
SCS↓→SCK↓ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↑→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS↓→SOT delay time	t_{DSE}		-	40	-	40	ns
SCS↑→SOT delay time	t_{DEE}		0	-	0	-	ns

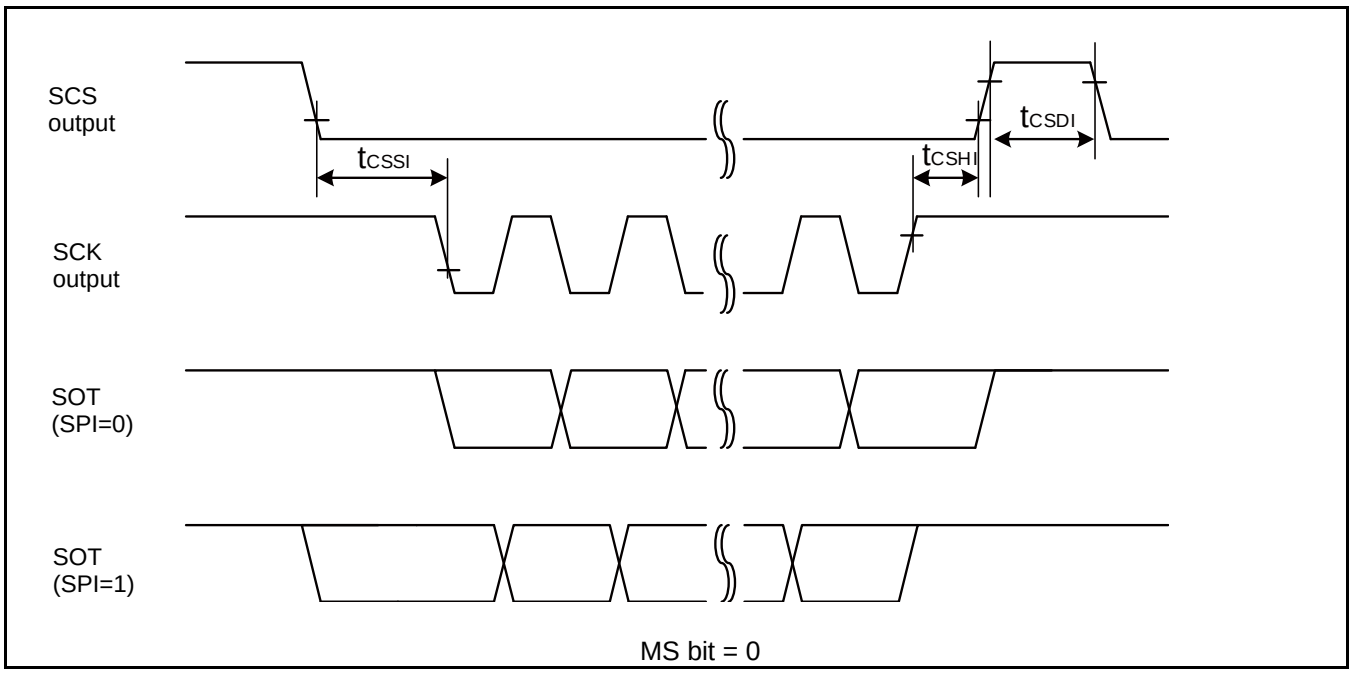
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

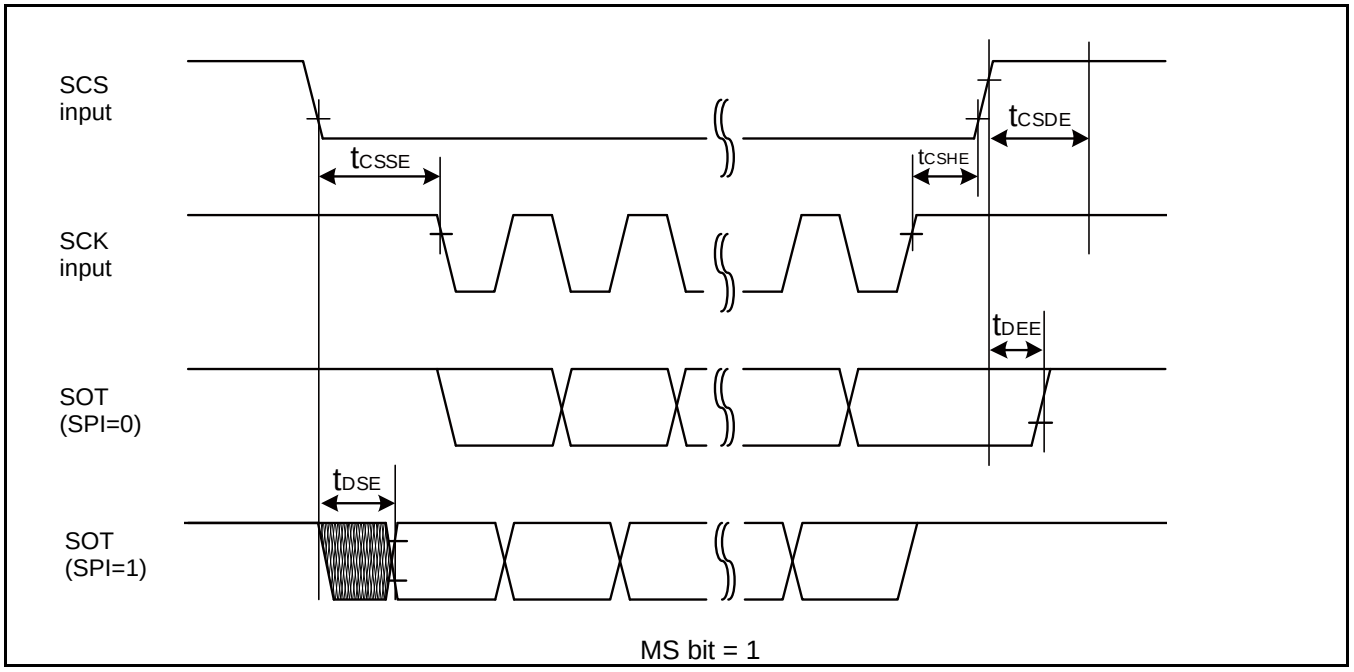
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.*
- *For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0

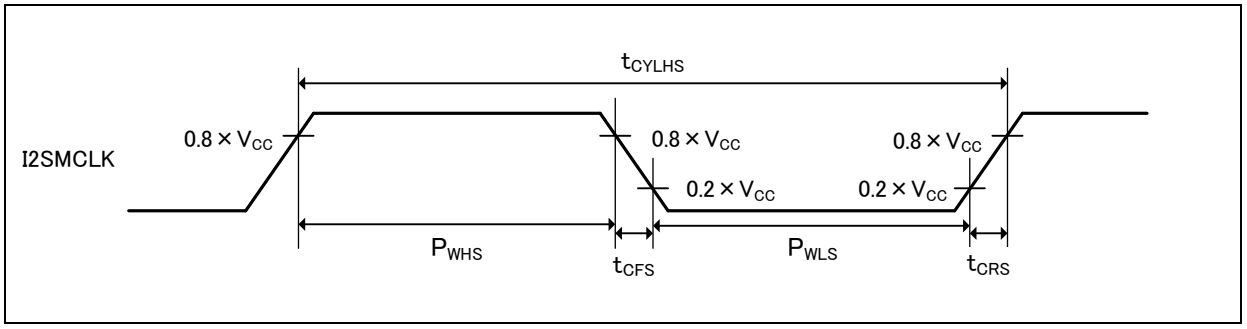


MS bit = 1

I2SMCLK Input Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{CHS}	I2SMCK	-	-	25	MHz	
Input clock cycle	t_{CYLHS}	-	-	40	-	ns	
Input clock pulse width	-	-	P_{WHS}/t_{CYLHS} P_{WLS}/t_{CYLHS}	45	55	%	When using external clock
Input clock rise time and fall time	t_{CFS} t_{CRS}	-	-	-	5	ns	When using external clock



I2SMCLK Output Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output frequency	f_{CHS}	I2SMCK	-	-	12.288	MHz	

15. Major Changes

Spansion Publication Number: S6E2C3_DS709-00012

Page	Section	Change Results
Revision 0.1		
-	-	Initial release
Revision 1.0		
11 13 87 88	2. Features 3. Product Lineup 10. Block Diagram 12. Memory Map	Deleted HDM-CEC/Remote Control Receiver.
16-18	5. Pin Assignments	Deleted the pins of HDM-CEC/Remote Control Receiver.(CEC0,CEC1) Revised the pin name of I2S. (MI2S*_0→MI2S*0_0) Deleted the pin of IGTRG0_0.
20-71	6. Pin Descriptions	Deleted the pins of HDM-CEC/Remote Control Receiver.(CEC0,CEC1) Revised the pin name of I2S. (MI2S*_0→MI2S*0_0) Revised the pin number of PF7 in LQFP216.(91→90) revised the pin number of X1. (73, 58, 50, P5→107, 87, 71, P13) Revised the pin number of X0A. (107, 87, 71, P13→73, 58, 50, P5)
72-79	7. I/O Circuit Type	Revised IOH/IOL of Type S.(IOH=-12mA→-10mA, IOL=12mA→10mA) Added the case of using I2C in Type E, F, G, L, N, S.
94-101	13. Pin Status In Each CPU State	Deleted X and Y in Pin Status Type.
102-103	14.1. Absolute Maximum Ratings	Added 10mA type.
104-107	14.2. Recommended Operating Conditions	Added AVRL in Analog reference voltage. Revised the leakage current in Maximum leakage current at operating
108-117	14.3.1. Current Rating	Revised the maximum current of each category.
118-119	14.3.2. Pin Characteristics	Added the characteristic of external bus in H level input voltage (hysteresis input). Added the characteristic of 10 mA type.
122	14.4.5. Operating Conditions of USB PLL・I2S PLL (in the case of using main clock for input clock of PLL)	Revised the maximum of I2S PLL macro oscillation clock frequency. (307.2 MHz→384 MHz)
186	14.5.12-bit A/D Converter	Revised the minimum of Sampling time. Revised the characteristic of State transition time to operation permission Added AVRL in Analog reference voltage.
194	14.8.2. Interrupt of Low-Voltage Detection	Revised the SVHI values in Conditions

NOTE: Please see “Document History” about later revised information.