

Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

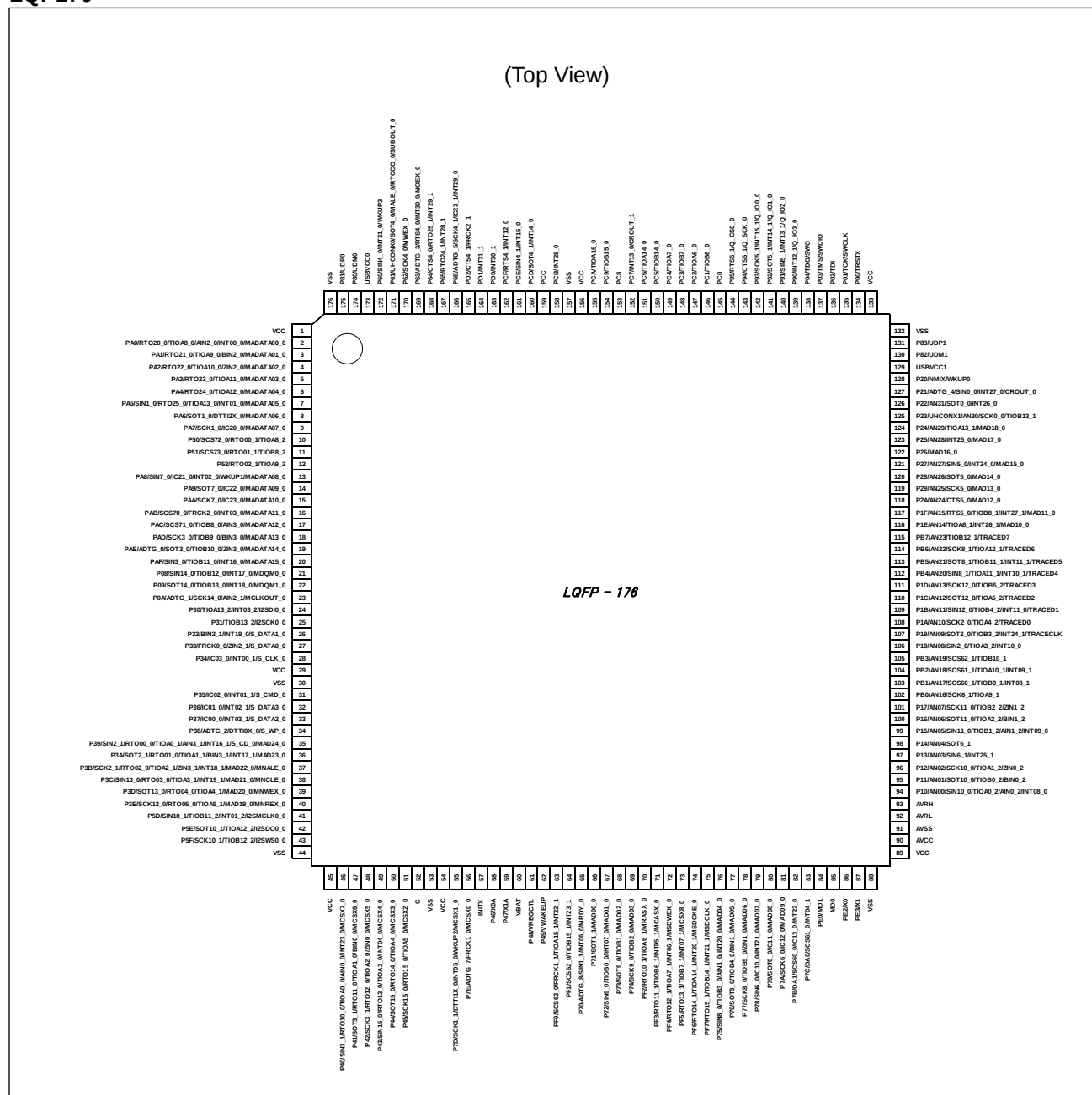
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

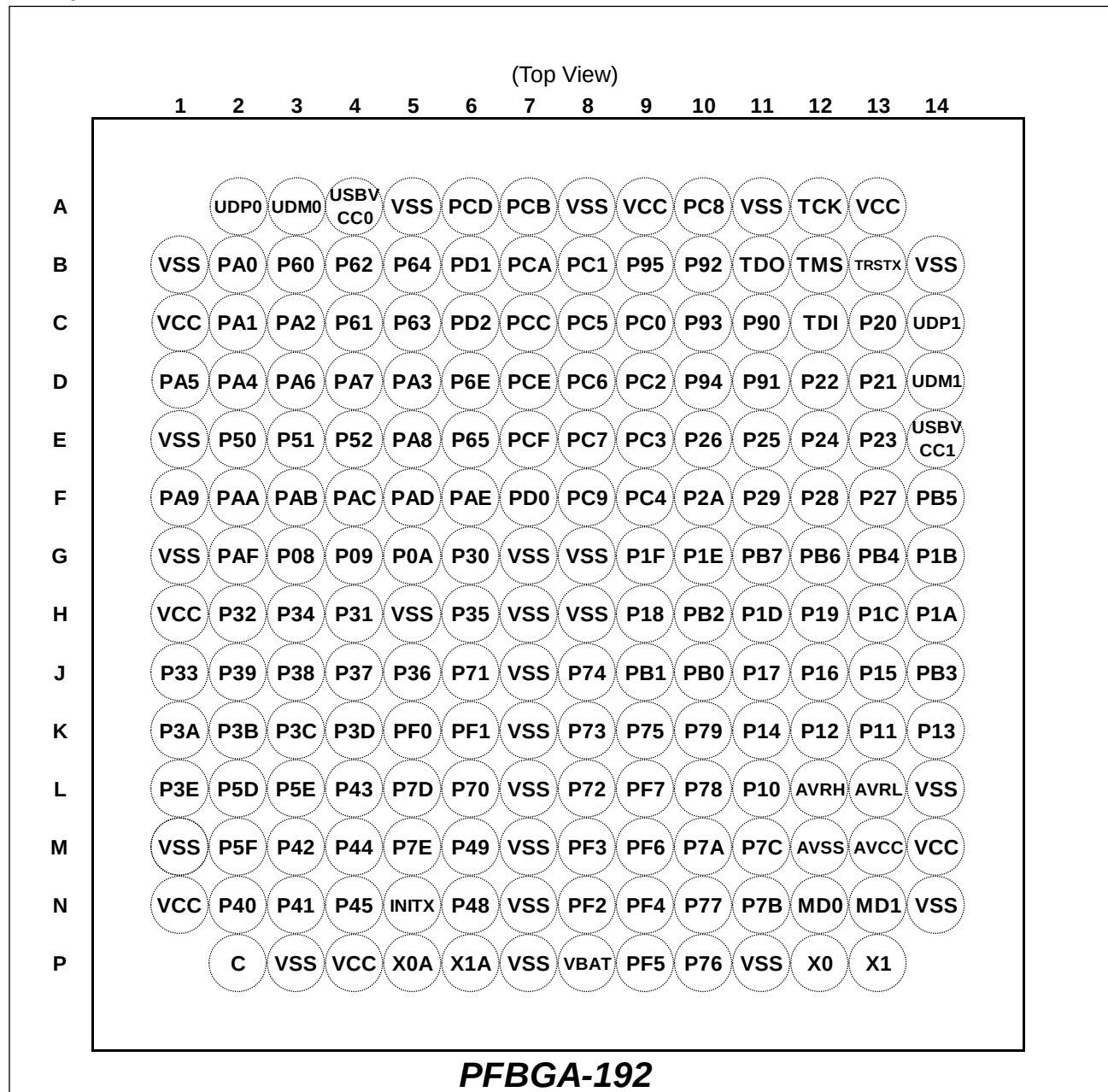
Details

Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CSIO, EBI/EMI, I ² C, LINbus, SD, SPI, UART/USART, USB
Peripherals	DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	152
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	192-LFBGA
Supplier Device Package	192-FBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2c3aj0agb1000a

LQP176



LBE192



Note:

- The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
125	101	85	J11	P17	F	L
				AN07		
				SCK11_0 (SCL11_0)		
				TIOB2_2		
				ZIN1_2		
126	102	-	J10	PB0	F	L
				AN16		
				SCK6_1 (SCL6_1)		
				TIOA9_1		
127	103	-	J9	PB1	F	M
				AN17		
				SCS60_1		
				TIOB9_1		
				INT08_1		
128	104	-	H10	PB2	F	M
				AN18		
				SCS61_1		
				TIOA10_1		
				INT09_1		
129	105	-	J14	PB3	F	L
				AN19		
				SCS62_1		
				TIOB10_1		
130	106	86	H9	P18	F	M
				AN08		
				SIN2_0		
				TIOA3_2		
				INT10_0		
131	107	87	H12	P19	F	O
				AN09		
				SOT2_0 (SDA2_0)		
				TIOB3_2		
				INT24_1		
				TRACECLK		
132	108	88	H14	P1A	F	N
				AN10		
				SCK2_0 (SCL2_0)		
				TIOA4_2		
				TRACED0		
133	109	89	G14	P1B	F	O
				AN11		
				SIN12_0		
				TIOB4_2		
				INT11_0		
				TRACED1		
134	110	90	H13	P1C	F	N
				AN12		
				SOT12_0 (SDA12_0)		
				TIOA5_2		
				TRACED2		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
210	170	138	B4	P62	L	I
				SCK4_0 (SCL4_0)		
				MWEX_0		
211	171	139	C4	P61	L	I
				UHCONX0		
				SOT4_0 (SDA4_0)		
				MALE_0		
				RTCCO_0		
				SUBOUT_0		
212	172	140	B3	P60	I	Q
				SIN4_0		
				INT31_0		
				WKUP3		
213	173	141	A4	USBVCC0	-	-
214	174	142	A3	P80	H	R
				UDM0		
215	175	143	A2	P81	H	R
				UDP0		
216	176	144	B1	VSS	-	-
-	-	-	E1		-	-
-	-	-	G1		-	-
-	-	-	P7		-	-
-	-	-	P11		-	-
-	-	-	L14		-	-
-	-	-	A11		-	-
-	-	-	A5		-	-
-	-	-	N7		-	-
-	-	-	M7		-	-
-	-	-	L7		-	-
-	-	-	K7		-	-
-	-	-	J7		-	-
--	-	-	G7		-	-
-	-	-	H7		-	-
-	-	-	H8		-	-
-	-	-	G8		-	-

Signal Descriptions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.

Use the extended port function register (EPFR) to select the pin.

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
A/D converter	ADTG_0	A/D converter external trigger input pin	24	19	16	F6
	ADTG_1		32	23	20	G5
	ADTG_2		44	34	29	J3
	ADTG_3		209	169	137	C5
	ADTG_4		157	127	103	D13
	ADTG_5		198	166	136	D6
	ADTG_6		119	-	-	-
	ADTG_7		71	56	48	M5
	ADTG_8		80	65	55	L6
	AN00	A/D converter analog input pin. ANxx describes A/D converter ch xx.	114	94	78	L11
	AN01		115	95	79	K13
	AN02		116	96	80	K12
	AN03		117	97	81	K14
	AN04		118	98	82	K11
	AN05		123	99	83	J13
	AN06		124	100	84	J12
	AN07		125	101	85	J11
	AN08		130	106	86	H9
	AN09		131	107	87	H12
	AN10		132	108	88	H14
	AN11		133	109	89	G14
	AN12		134	110	90	H13
	AN13		135	111	91	H11
	AN14		142	116	92	G10
	AN15		143	117	93	G9
	AN16		126	102	-	J10
	AN17		127	103	-	J9
	AN18		128	104	-	H10
	AN19		129	105	-	J14
	AN20		138	112	-	G13
	AN21		139	113	-	F14
	AN22		140	114	-	G12
	AN23		141	115	-	G11
	AN24		144	118	94	F10
	AN25		145	119	95	F11
	AN26		146	120	96	F12
	AN27		147	121	97	F13
	AN28		153	123	99	E11
	AN29		154	124	100	E12
	AN30		155	125	101	E13
	AN31		156	126	102	D12

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	P50	General-purpose I/O port 5	10	10	-	E2
	P51		11	11	-	E3
	P52		12	12	-	E4
	P53		13	-	-	-
	P54		19	-	-	-
	P55		20	-	-	-
	P56		21	-	-	-
	P57		22	-	-	-
	P58		26	-	-	-
	P59		27	-	-	-
	P5A		28	-	-	-
	P5B		29	-	-	-
	P5C		33	-	-	-
	P5D		51	41	-	L2
	P5E		52	42	-	L3
	P5F		53	43	-	M2
	P60	General-purpose I/O port 6	212	172	140	B3
	P61		211	171	139	C4
	P62		210	170	138	B4
	P63		209	169	137	C5
	P64		208	168	-	B5
	P65		207	167	-	E6
	P66		206	-	-	-
	P67		205	-	-	-
	P68		204	-	-	-
	P69		203	-	-	-
	P6A		202	-	-	-
	P6B		201	-	-	-
	P6C		200	-	-	-
	P6D		199	-	-	-
	P6E		198	166	136	D6

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Serial 15	SIN15_0	Multi-function serial interface ch 15 input pin	59	49	41	L4
	SIN15_1		19	-	-	-
	SOT15_0 (SDA15_0)	Multi-function serial interface ch 15 output pin.	60	50	42	M4
	SOT15_1 (SDA15_1)	This pin operates as SOT15 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA15 when it is used in an I ² C (operation mode 4).	20	-	-	-
	SCK15_0 (SCL15_0)	Multi-function serial interface ch 15 clock I/O pin.	61	51	43	N4
	SCK15_1 (SCL15_1)	This pin operates as SCK15 when it is used in a CSIO (operation mode 2) and as SCL15 when it is used in an I ² C (operation mode 4).	21	-	-	-

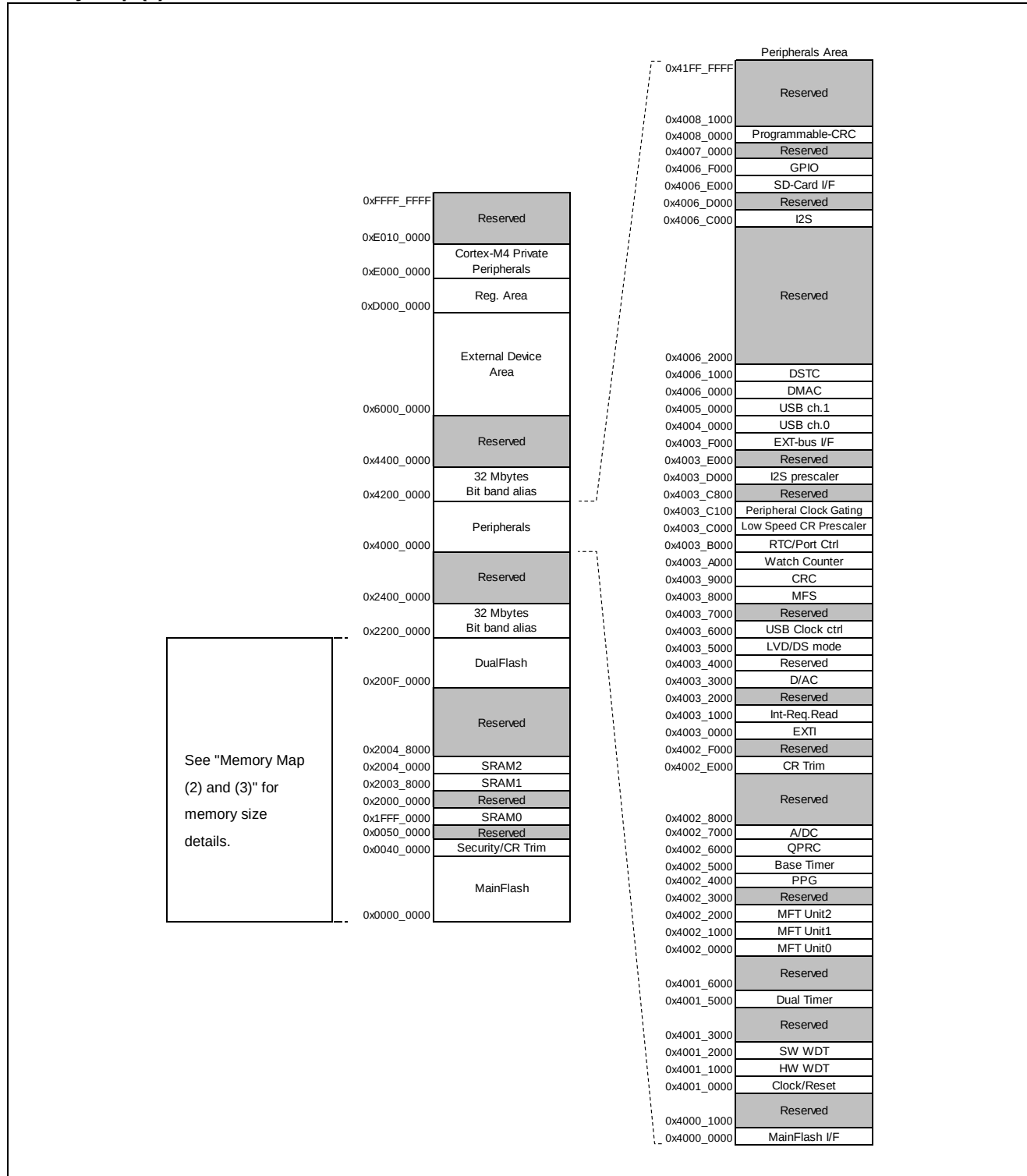
Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Timer 0	DTTIOX_0	Input signal controlling waveform generator outputs RTO00 to RTO05 of Multi-Function Timer 0.	44	34	29	J3
	DTTIOX_1		21	-	-	-
	FRCK0_0	16-bit free-run timer ch 0 external clock input pin	37	27	22	J1
	FRCK0_1		29	-	-	-
	IC00_0	16-bit input capture input pin of Multi-Function Timer 0. ICxx describes channel number.	43	33	28	J4
	IC00_1		22	-	-	-
	IC01_0		42	32	27	J5
	IC01_1		26	-	-	-
	IC02_0		41	31	26	H6
	IC02_1		27	-	-	-
	IC03_0		38	28	23	H3
	IC03_1		28	-	-	-
	RTO00_0 (PPG00_0)	Waveform generator output pin of Multi-Function Timer 0.	45	35	30	J2
	RTO00_1 (PPG00_1)	This pin operates as PPG00 when it is used in PPG0 output modes.	10	10	-	E2
	RTO01_0 (PPG00_0)	Waveform generator output pin of Multi-Function Timer 0.	46	36	31	K1
	RTO01_1 (PPG00_1)	This pin operates as PPG00 when it is used in PPG0 output modes.	11	11	-	E3
	RTO02_0 (PPG02_0)	Waveform generator output pin of Multi-Function Timer 0.	47	37	32	K2
	RTO02_1 (PPG02_1)	This pin operates as PPG02 when it is used in PPG0 output modes.	12	12	-	E4
	RTO03_0 (PPG02_0)	Waveform generator output pin of Multi-Function Timer 0.	48	38	33	K3
	RTO03_1 (PPG02_1)	This pin operates as PPG02 when it is used in PPG0 output modes.	13	-	-	-
	RTO04_0 (PPG04_0)	Waveform generator output pin of Multi-Function Timer 0.	49	39	34	K4
	RTO04_1 (PPG04_1)	This pin operates as PPG04 when it is used in PPG0 output modes.	19	-	-	-
	RTO05_0 (PPG04_0)	Waveform generator output pin of Multi-Function Timer 0.	50	40	35	L1
	RTO05_1 (PPG04_1)	This pin operates as PPG04 when it is used in PPG0 output modes.	20	-	-	-

9. Memory Size

See Memory size in 1. Product Lineup to confirm the memory size.

10. Memory Map

Memory Map (1)



List of VBAT Domain Pin Status

VBAT Pin Status Type	Function Group	Power-on reset*1	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return From Deep Standby Mode State	VBAT RTC Mode State	Return From VBAT RTC Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable	Power Supply Stable	Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1	-	-
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-	-	-
S	GPIO selected	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Setting prohibition	-
	Sub crystal oscillator input pin/ external sub clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Maintain previous state	Maintain previous state
T	GPIO selected	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Setting prohibition	-
	External sub clock input selected	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	Sub crystal oscillator output pin	Hi-Z/ internal input fixed at 0/ or input enable	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state/ When oscillation stops, Hi-Z*2	Maintain previous state/ When oscillation stops, Hi-Z*2	Maintain previous state/ When oscillation stops, Hi-Z*2	Maintain previous state/ When oscillation stops, Hi-Z*2	Maintain previous state	Maintain previous state	Maintain previous state
U	Resource selected	Hi-Z	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected											

*1: When VBAT and VCC power on.

*2: When the SOSCNTL bit in the WTOSCCNT register is 0, the sub crystal oscillator output pin is maintained in the previous state. When the SOSCNTL bit in the WTOSCCNT register is 1, oscillation is stopped at Stop mode and Deep Standby Stop mode

Separate Bus Access Asynchronous SRAM Mode

 (V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MOEX Minimum pulse width	t _{OE}	MOEX	-	MCLK×n-3	-	ns	
MCSX ↓ → Address output delay time	t _{CSL - AV}	MCSX[7: 0], MAD[24: 0]	-	-9	+9	ns	
MOEX ↑ → Address hold time	t _{OE} - AX	MOEX, MAD[24: 0]	-	0	MCLK×m+9	ns	
MCSX ↓ → MOEX ↓ delay time	t _{CSL - OEL}	MOEX, MCSX[7: 0]	-	MCLK×m-9	MCLK×m+9	ns	
MOEX ↑ → MCSX ↑ time	t _{OE} - CSH		-	0	MCLK×m+9	ns	
MCSX ↓ → MDQM ↓ delay time	t _{CSL - RDQML}	MCSX, MDQM[3: 0]	-	MCLK×m-9	MCLK×m+9	ns	
Data set up → MOEX ↑ time	t _{DS - OE}	MOEX, MADATA[31: 0]	-	20	-	ns	
MOEX ↑ → Data hold time	t _{DH - OE}	MOEX, MADATA[31: 0]	-	0	-	ns	
MWEX Minimum pulse width	t _{WE}	MWEX	-	MCLK×n-3	-	ns	
MWEX ↑ → Address output delay time	t _{WE} - AX	MWEX, MAD[24: 0]	-	0	MCLK×m+9	ns	
MCSX ↓ → MWEX ↓ delay time	t _{CSL - WEL}	MWEX, MCSX[7: 0]	-	MCLK×n-9	MCLK×n+9	ns	
MWEX ↑ → MCSX ↑ delay time	t _{WE} - CSH		-	0	MCLK×m+9	ns	
MCSX ↓ → MDQM ↓ delay time	t _{CSL - WDQML}	MCSX, MDQM[3: 0]	-	MCLK×n-9	MCLK×n+9	ns	
MCSX ↓ → Data output time	t _{CSL - DX}	MCSX, MADATA[31: 0]	-	MCLK-9	MCLK+9	ns	
MWEX ↑ → Data hold time	t _{WE} - DX	MWEX, MADATA[31: 0]	-	0	MCLK×m+9	ns	

Note:

- When the external load capacitance C_L = 30 pF (m = 0 to 15, n = 1 to 16)

12.4.12 CSIO (SPI) Timing

Synchronous Serial (SPI = 0, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V _{CC} < 4.5 V		V _{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-		-	8	-	8	Mbps
Serial clock cycle time	t _{SCYC}	SCKx	Internal shift clock operation	4t _{CYCP}	-	4t _{CYCP}	-	ns
SCK↓→SOT delay time	t _{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↑ setup time	t _{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK↑→SIN hold time	t _{SHIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t _{SLSH}	SCKx		2t _{CYCP} - 10	-	2t _{CYCP} - 10	-	ns
Serial clock H pulse width	t _{SHSL}	SCKx	External shift clock operation	t _{CYCP} + 10	-	t _{CYCP} + 10	-	ns
SCK↓→SOT delay time	t _{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↑ setup time	t _{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK↑→SIN hold time	t _{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK fall time	t _F	SCKx		-	5	-	5	ns
SCK rise time	t _R	SCKx		-	5	-	5	ns

Notes:

- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- These characteristics only guarantee the same relocate port number; for example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance C_L = 30 pF.

Synchronous Serial (SPI = 0, SCINV = 1)

 (V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V _{CC} < 4.5 V		V _{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t _{SCYC}	SCKx	Internal shift clock operation	4t _{CYCP}	-	4t _{CYCP}	-	ns
SCK↑→SOT delay time	t _{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↓ setup time	t _{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK↓→SIN hold time	t _{SLIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t _{LSLH}	SCKx		2t _{CYCP} - 10	-	2t _{CYCP} - 10	-	ns
Serial clock H pulse width	t _{SHSL}	SCKx	External shift clock operation	t _{CYCP} + 10	-	t _{CYCP} + 10	-	ns
SCK↑→SOT delay time	t _{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↓ setup time	t _{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK↓→SIN hold time	t _{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK fall time	t _F	SCKx		-	5	-	5	ns
SCK rise time	t _R	SCKx		-	5	-	5	ns

Notes:

- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- These characteristics only guarantee the same relocate port number; for example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance C_L = 30 pF.

When Using Synchronous Serial Chip Select (SCINV = 0, CSLVL = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V _{CC} < 4.5 V		V _{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↓ setup time	t _{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↓ hold time	t _{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t _{CSDI}		(*3)-50 +5t _{CYCP}	(*3)+50 +5t _{CYCP}	(*3)-50 +5t _{CYCP}	(*3)+50 +5t _{CYCP}	ns
SCS↑→SCK↓ setup time	t _{CSSE}	External shift clock operation	3t _{CYCP} +30	-	3t _{CYCP} +30	-	ns
SCK↑→SCS↓ hold time	t _{CSHE}		0	-	0	-	ns
SCS deselect time	t _{CSDE}		3t _{CYCP} +30	-	3t _{CYCP} +30	-	ns
SCS↑→SOT delay time	t _{DSE}		-	40	-	40	ns
SCS↓→SOT delay time	t _{DDE}		0	-	0	-	ns

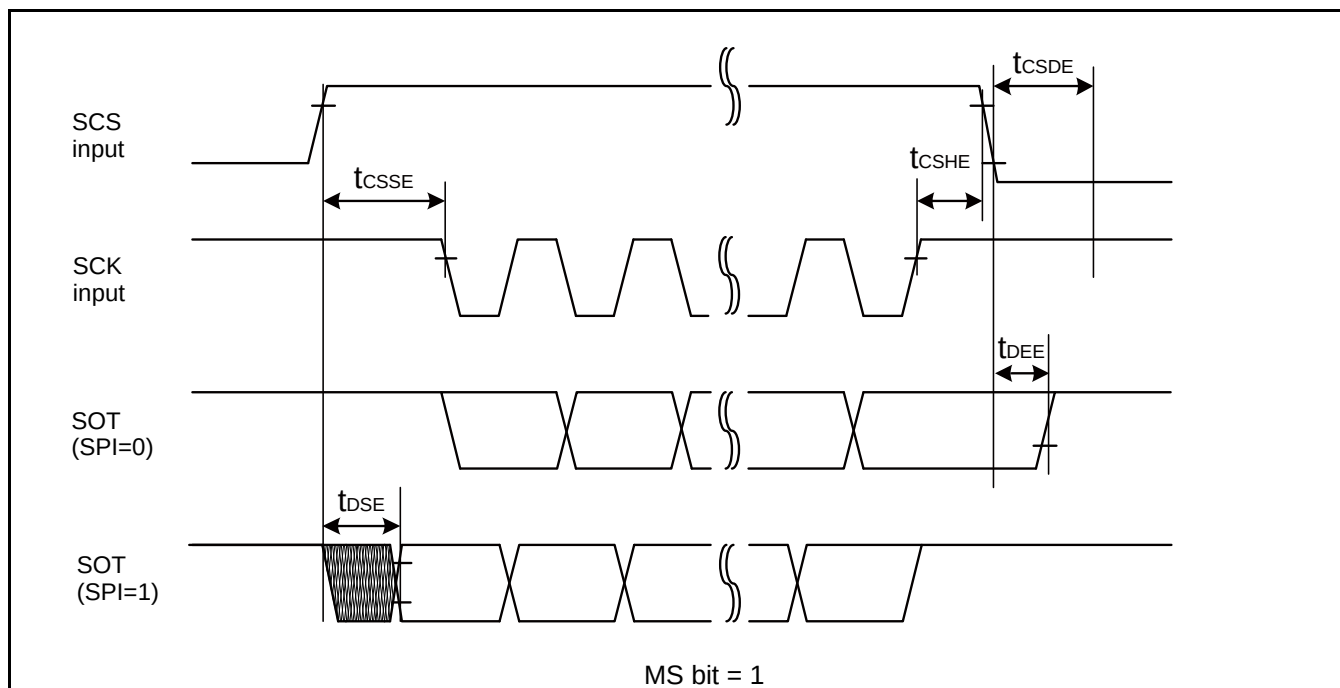
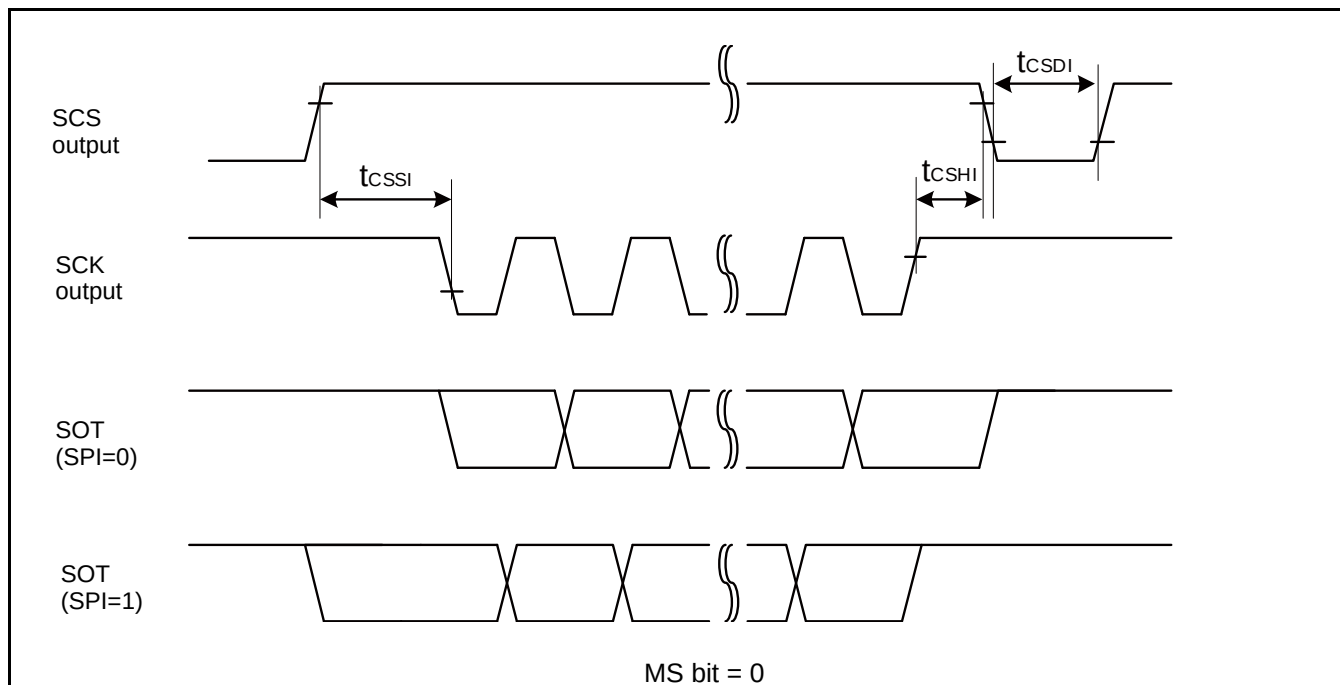
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

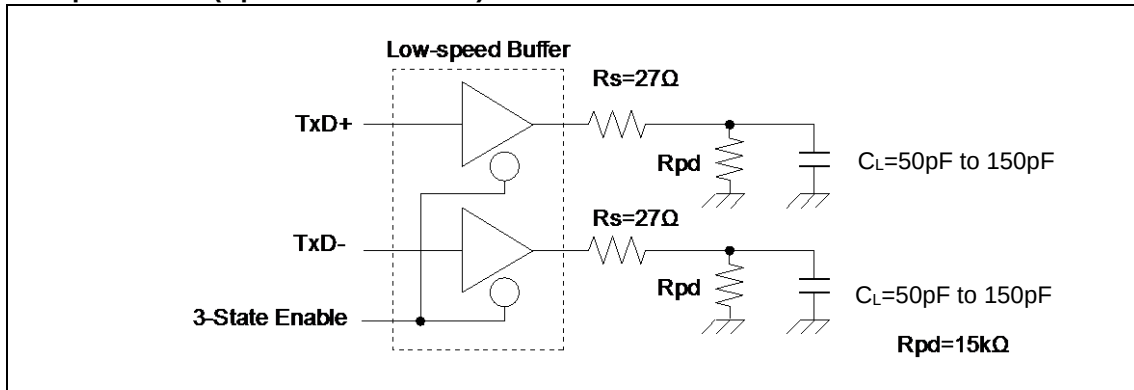
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

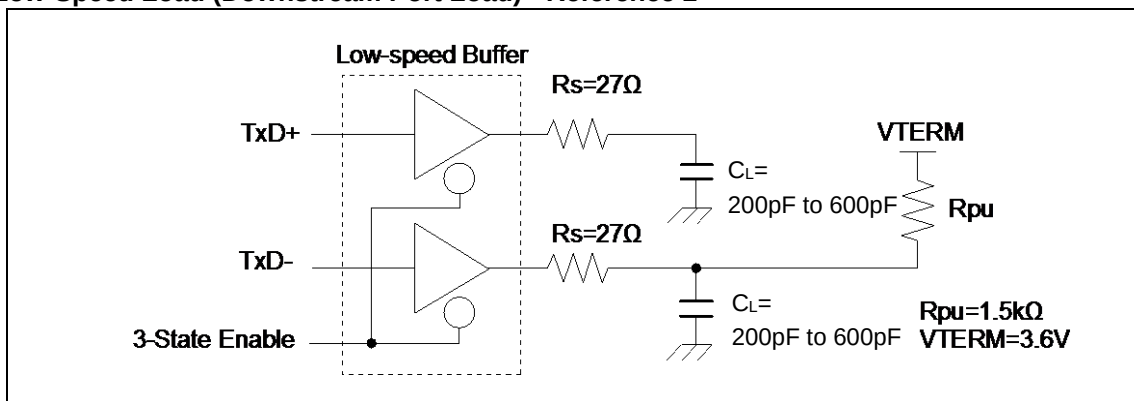
- t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).
- When the external load capacitance C_L = 30 pF.



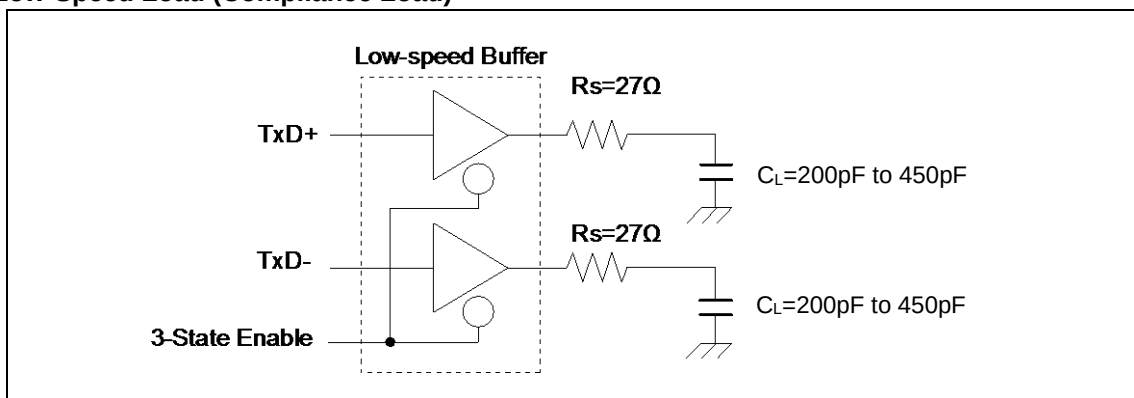
Low-Speed Load (Upstream Port Load) - Reference 1



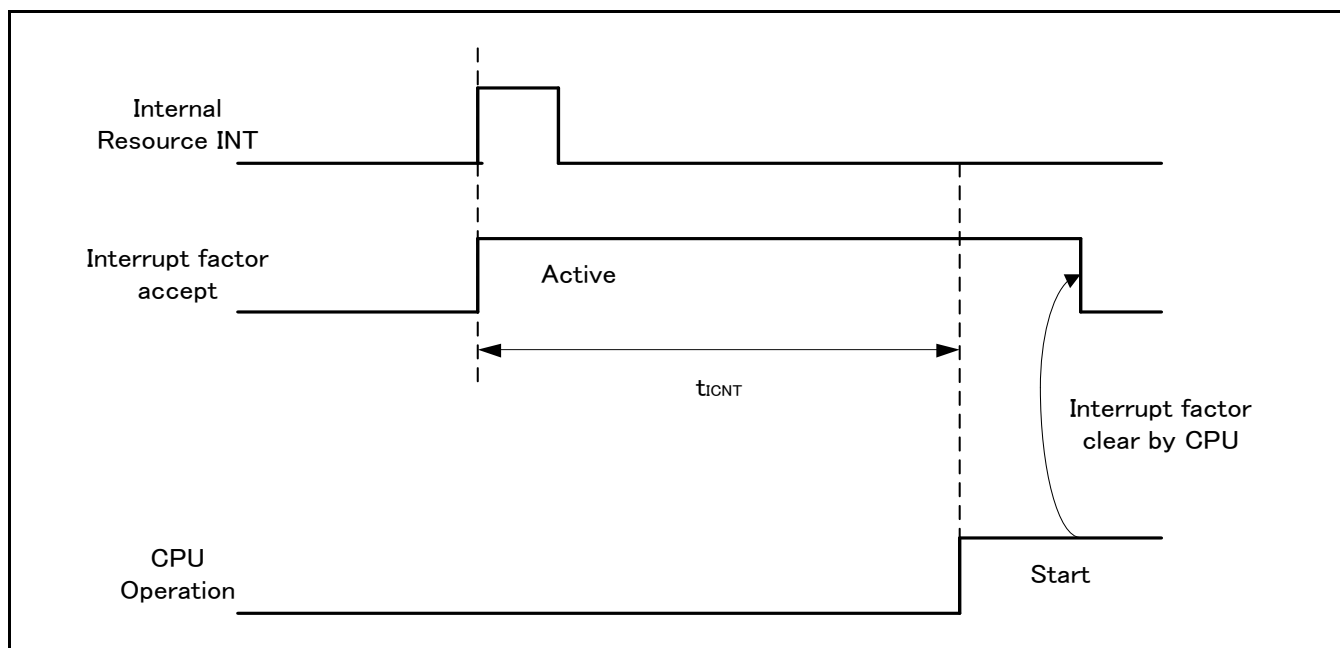
Low-Speed Load (Downstream Port Load) - Reference 2



Low-Speed Load (Compliance Load)



Example of Standby Recovery Operation (when in Internal Resource Interrupt Recovery*)



*: Depending on the standby mode, interrupt from the internal resource is not included in the recovery cause.

Notes:

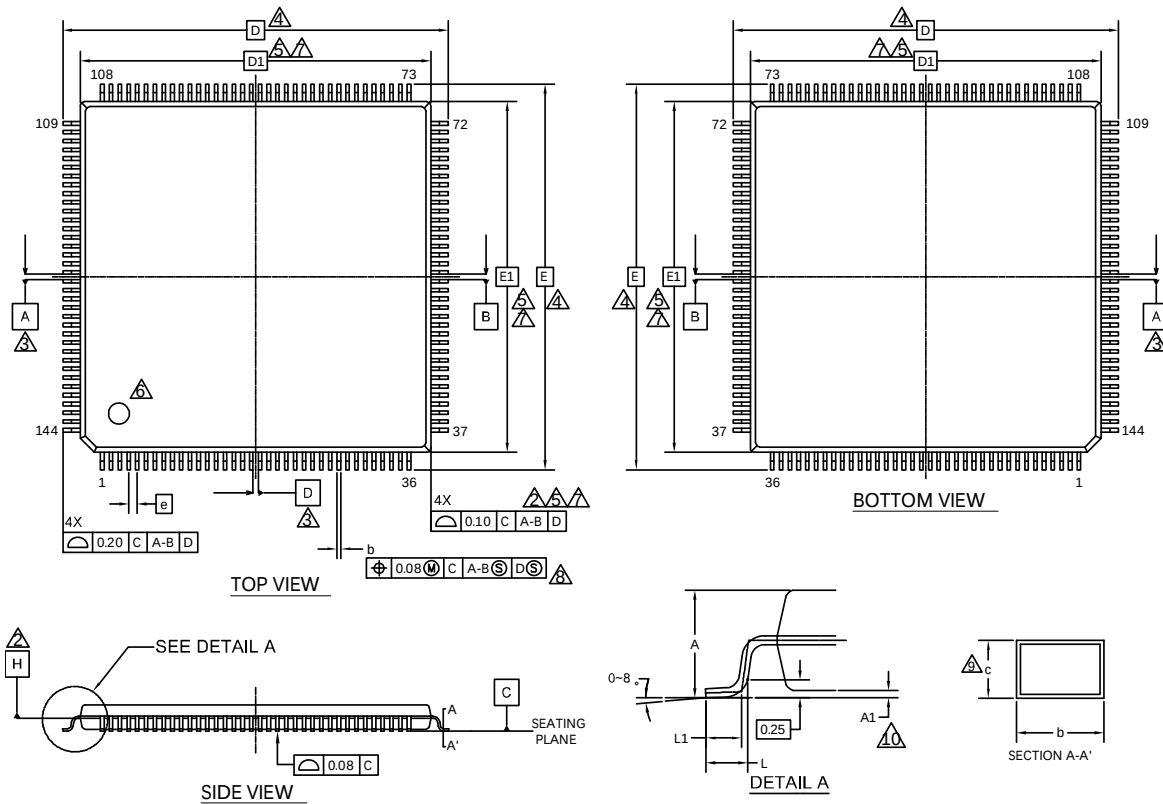
- The return factor is different in each low-power consumption mode. See Chapter 6: Low Power Consumption Mode and Operations of Standby Modes in FM4 Family Peripheral Manual Main Part (002-04856).
- The recovery process is unique for each operating mode. See Chapter 6: Low Power Consumption Mode in FM4 Family Peripheral Manual Main Part (002-04856).

13. Ordering Information

Part number	Flash	RAM	Crypto	Package
S6E2C38H0AGV2000A	1 MB	128 KB	N/A	Plastic • LQFP (0.5-mm pitch), 144 pin (LQS144)
S6E2C39H0AGV2000A	1.5 MB	192 KB	N/A	
S6E2C3AH0AGV2000A	2 MB	256 KB	N/A	
S6E2C38J0AGV2000A	1 MB	128 KB	N/A	Plastic • LQFP (0.65-mm pitch), 176 pin (LQP176)
S6E2C39J0AGV2000A	1.5 MB	192 KB	N/A	
S6E2C3AJ0AGV2000A	2 MB	256 KB	N/A	
S6E2C38J0AGB1000A	1 MB	128 KB	N/A	Plastic • LQFP (0.8-mm pitch), 192 pin (LBE192)
S6E2C39J0AGB1000A	1.5 MB	192 KB	N/A	
S6E2C3AJ0AGB1000A	2 MB	256 KB	N/A	
S6E2C38L0AGL2000A	1 MB	128 KB	N/A	Plastic • LQFP (0.4-mm pitch), 216 pin (LQQ216)
S6E2C39L0AGL2000A	1.5 MB	192 KB	N/A	
S6E2C3AL0AGL2000A	2 MB	256 KB	N/A	

14. Package Dimensions

Package Type	Package Code
LQFP 144	LQS 144



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.17	0.22	0.27
c	0.09	—	0.20
D	22.00 BSC		
D1	20.00 BSC		
e	0.50 BSC		
E	22.00 BSC		
E1	20.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

NOTES

- ALL DIMENSIONS ARE IN MILLIMETERS
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE.
- DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

