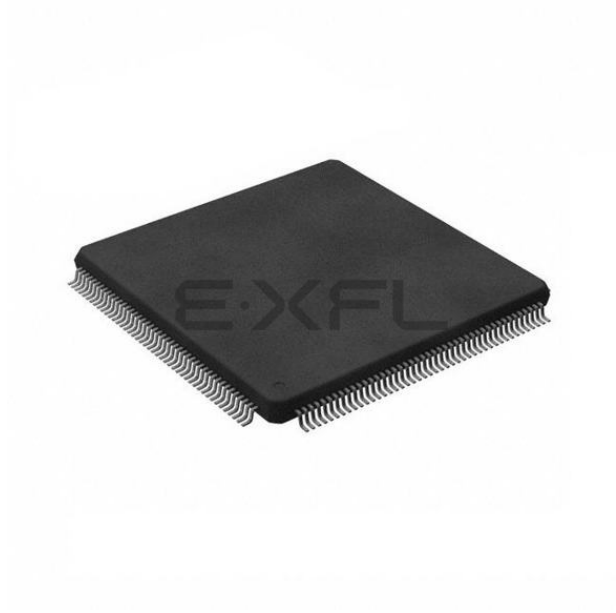

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CSIO, EBI/EMI, I²C, LINbus, SD, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	152
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2c3aj0agv2000a

Peripheral Clock Gating

The system can reduce the current consumption of the total system with gating the operation clocks of peripheral functions not used.

VBAT

The consumption power during the RTC operation can be reduced by supplying the power supply independent from the RTC (calendar circuit)/32 kHz oscillation circuit. The following circuits can also be used.

- RTC
- 32-kHz oscillation circuit
- Power-on circuit
- Back up register: 32 bytes
- Port circuit

Debug

- Serial wire JTAG debug port (SWJ-DP)
- Embedded trace macrocells (ETM) provide comprehensive debug and trace facilities.
- AHB trace macrocells (HTM)

Unique ID

Unique value of the device (41-bit) is set.

Power Supply

- Four power supplies
  - Wide range voltage:
    VCC = 2.7 V to 5.5 V
  - Power supply for USB ch 0 I/O:
    USBVCC0 = 3.0 V to 3.6 V (when USB is used)
    = 2.7 V to 5.5 V (when GPIO is used)
  - Power supply for USB ch 1 I/O:
    USBVCC1 = 3.0 V to 3.6 V (when USB is used)
    = 2.7 V to 5.5 V (when GPIO is used)
  - Power supply for VBAT:
    VBAT = 1.65 V to 5.5 V

Table of Contents

1. Product Lineup

Memory Size

Product Name		S6E2C38H/J/L	S6E2C39H/J/L	S6E2C3AH/J/L
On-chip flash memory		1024 Kbytes	1536 Kbytes	2048 Kbytes
On-chip	SRAM	128 Kbytes	192 Kbytes	256 Kbytes
	SRAM0	64 Kbytes	128 Kbytes	192 Kbytes
	SRAM1	32 Kbytes	32 Kbytes	32 Kbytes
	SRAM2	32 Kbytes	32 Kbytes	32 Kbytes

Function

Product Name			S6E2C38H0A S6E2C39H0A S6E2C3AH0A	S6E2C38J0A S6E2C39J0A S6E2C3AJ0A	S6E2C38L0A S6E2C39L0A S6E2C3AL0A
Pin count			144	176/192	216
CPU			Cortex-M4F, MPU, NVIC 128 ch		
	Freq.		200 MHz		
Power supply voltage range			2.7V to 5.5V		
USB2.0 (device/host)			2 ch		
DMAC			8ch		
DSTC			256 ch		
External bus interface			Addr: 25-bit (Max), Data: 8-/16-bit CS: 9 (Max), SRAM, NOR flash NAND flash	Addr: 25-bit (Max), Data: 8-/16-bit CS: 9 (Max), SRAM, NOR flash , NAND flash SDRAM	Addr: 25-bit (Max), Data: 8-/16-/32-bit CS: 9 (Max), SRAM, NOR flash , NAND flash, SDRAM
Multi-function serial interface (UART/CSIO/LIN/I^{2}C)			16ch (Max) ch 0 to ch 7 : FIFO, ch 8 to ch 15 : No FIFO		
Base timer (PWC/Reload timer/PWM/PPG)			16 ch (Max)		
MF timer	A/D activation compare	6 ch	3 units (Max)		
	Input capture	4 ch			
	Free-run timer	3 ch			
	Output compare	6 ch			
	Waveform generator	3 ch			
	PPG	3 ch			
SD card interface			1 unit		
I^{2}S			-	1 unit	
High-speed quad SPI			-	1 unit	
QPRC			4 ch (Max)		
Dual timer			1 unit		
Real-time clock			1 unit		
Watch counter			1 unit		
CRC accelerator			Yes (fixed, programmable)		
Watchdog timer			1 ch (SW) + 1 ch (HW)		
External interrupts			32 pins (Max)+ NMI × 1		
I/O ports			120 pins (Max)	152 pins (Max)	190 pins (Max)
12-bit A/D converter			24 ch (3 units)	32 ch (3 units)	
12-bit D/A converter			2 units (Max)		
CSV (clock supervisor)			Yes		
LVD (low-voltage detector)			2 ch		
Built-in CR	High-speed		4 MHz		
	Low-speed		100 kHz		
Debug function			SWJ-DP/ETM/HTM		
Unique ID			Yes		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
10	10	-	E2	P50 SCS72_0 RTO00_1 (PPG00_1) TIOA8_2 MADATA16_0	E	I
11	11	-	E3	P51 SCS73_0 RTO01_1 (PPG00_1) TIOB8_2 MADATA17_0	E	I
12	12	-	E4	P52 RTO02_1 (PPG02_1) TIOA9_2 MADATA18_0	E	I
13	-	-	-	P53 RTO03_1 (PPG02_1) TIOB9_2 MADATA19_0	E	I
14	13	10	E5	PA8 SIN7_0 IC21_0 INT02_0 WKUP1 MADATA08_0	I	Q
15	14	11	F1	PA9 SOT7_0 (SDA7_0) IC22_0 MADATA09_0	N	I
16	15	12	F2	PAA SCK7_0 (SCL7_0) IC23_0 MADATA10_0	N	I
17	16	13	F3	PAB SCS70_0 FRCK2_0 INT03_0 MADATA11_0	E	K
18	17	14	F4	PAC SCS71_0 TIOB8_0 AIN3_0 MADATA12_0	E	I
19	-	-	-	P54 SIN15_1 RTO04_1 (PPG04_1) TIOA10_2 INT00_2 MADATA20_0	E	K

Notes on Power-on

Turn power on/off in the following order or at the same time. The device operates normally after all power on.

VBAT only Power-on is possible when VBAT and VCC turns Power-on and Hibernation control is setting and then VCC turns Power-off. About Hibernation control, see Chapter 7-2: VBAT Domain(B) in FM4 Family Peripheral Manual Main Part(002-04856).

Turning on:	VBAT → VCC → USBVCC0
	VBAT → VCC → USBVCC1
	VCC → AVCC → AVRH
Turning off:	AVRH → AVCC → VCC
	USBVCC1 → VCC → VBAT
	USBVCC0 → VCC → VBAT

Serial Communication

There is a possibility of receiving incorrect data as a result of noise or other issues introduced by the serial communication. Take care to design the printed circuit board to minimize noise.

Consider the case of introducing error as a result of noise, perform error detection such as by applying a checksum of data at the end. If an error is detected, retransmit the data.

Differences in Characteristics within the Product Line

The electric characteristics including power consumption, ESD, latch-up, noise, and oscillation differ among members of the product line because chip layout and memory structures are not the same; for example, different sizes, flash versus ROM, etc. If you are switching to a different product of the same series, please make sure to evaluate the electric characteristics.

Pull-Up Function of 5 V Tolerant I/O

Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5 V tolerant I/O.

Pin Doubled as Debug Function

The pin doubled as TDO/TMS/TDI/TCK/TRSTX, SWO/SWDIO/SWCLK should be used as output only. Do not use as input.

Peripheral Address Map

Start Address	End Address	Bus	Peripherals
0x4000_0000	0x4000_0FFF	AHB	MainFlash I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/reset control
0x4001_1000	0x4001_1FFF		Hardware watchdog timer
0x4001_2000	0x4001_2FFF		Software watchdog timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual-timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-Function Timer unit 0
0x4002_1000	0x4002_1FFF		Multi-Function Timer unit 1
0x4002_2000	0x4002_2FFF		Multi-Function Timer unit 2
0x4002_3000	0x4002_3FFF		Reserved
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base timer
0x4002_6000	0x4002_6FFF		Quadrature position/revolution counter
0x4002_7000	0x4002_7FFF		A/D converter
0x4002_8000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Internal CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF	APB2	External interrupt controller
0x4003_1000	0x4003_1FFF		Interrupt request batch-read function
0x4003_2000	0x4003_2FFF		Reserved
0x4003_3000	0x4003_3FFF		D/A converter
0x4003_4000	0x4003_4FFF		Reserved
0x4003_5000	0x4003_57FF		Low voltage detector
0x4003_5800	0x4003_5FFF		Deep standby mode Controller
0x4003_6000	0x4003_6FFF		USB clock generator
0x4003_7000	0x4003_7FFF		Reserved
0x4003_8000	0x4003_8FFF		Multi-function serial interface
0x4003_9000	0x4003_9FFF		CRC
0x4003_A000	0x4003_AFFF		Watch counter
0x4003_B000	0x4003_BFFF		RTC/port control
0x4003_C000	0x4003_C0FF		Low-speed CR prescaler
0x4003_C100	0x4003_C7FF		Peripheral clock gating
0x4003_C800	0x4003_CFFF		Reserved
0x4003_D000	0x4003_DFFF		I^2S prescaler
0x4003_E000	0x4003_EFFF		Reserved
0x4003_F000	0x4003_FFFF		External memory interface
0x4004_0000	0x4004_FFFF	AHB	USB ch 0
0x4005_0000	0x4005_FFFF		USB ch 1
0x4006_0000	0x4006_0FFF		DMAC register
0x4006_1000	0x4006_1FFF		DSTC register
0x4006_2000	0x4006_BFFF		Reserved
0x4006_C000	0x4006_CFFF		I^2S
0x4006_D000	0x4006_DFFF		Reserved
0x4006_E000	0x4006_EFFF		SD card I/F
0x4006_F000	0x4006_FFFF		GPIO
0x4007_0000	0x4007_FFFF		Reserved
0x4008_0000	0x4008_0FFF		Programmable-CRC
0x4008_1000	0x41FF_FFFF		Reserved
0x200E_0000	0x200E_FFFF		Workflash I/F register
0xD000_0000	0xDFFF_FFFF		High-speed quad SPI control register

List of VBAT Domain Pin Status

VBAT Pin Status Type	Function Group	Power-on reset*1	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return From Deep Standby Mode State	VBAT RTC Mode State	Return From VBAT RTC Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable	Power Supply Stable	Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1	-	-
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-	-	-
S	GPIO selected	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Setting prohibition	-
	Sub crystal oscillator input pin/ external sub clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Maintain previous state	Maintain previous state
T	GPIO selected	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Setting prohibition	-
	External sub clock input selected	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	Sub crystal oscillator output pin	Hi-Z/ internal input fixed at 0/ or input enable	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state/ When oscillation stops, Hi-Z*2	Maintain previous state/ When oscillation stops, Hi-Z*2	Maintain previous state/ When oscillation stops, Hi-Z*2	Maintain previous state/ When oscillation stops, Hi-Z*2	Maintain previous state	Maintain previous state	Maintain previous state
U	Resource selected	Hi-Z	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected											

*1: When VBAT and VCC power on.

*2: When the SOSCNTL bit in the WTOSCCNT register is 0, the sub crystal oscillator output pin is maintained in the previous state. When the SOSCNTL bit in the WTOSCCNT register is 1, oscillation is stopped at Stop mode and Deep Standby Stop mode

12.2 Recommended Operating Conditions

Parameter		Symbol	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply voltage		V_{CC}	-	2.7 *7	5.5	V	
Power supply voltage (for USB ch 0)		$USBV_{CC}0$	-	3.0	3.6 ($\leq V_{CC}$)	V	*1
				2.7	5.5 ($\leq V_{CC}$)		*2
Power supply voltage (for USB ch 1)		$USBV_{CC}1$	-	3.0	3.6 ($\leq V_{CC}$)	V	*3
				2.7	5.5 ($\leq V_{CC}$)		*4
Power supply voltage (VBAT)		V_{BAT}	-	1.65	5.5	V	
Analog power supply voltage		AV_{CC}	-	2.7	5.5	V	$AV_{CC} = V_{CC}$
Analog reference voltage		AVRH	-	*6	AV_{CC}	V	
		AVRL	-	AV_{SS}	AV_{SS}	V	
Operating temperature	Junction temperature	T_J	-	- 40	+ 125	°C	
	Ambient temperature	T_A	-	-40	*5	°C	

*1: When P81/UDP0 and P80/UDM0 pins are used as USB (UDP0, UDM0)

*2: When P81/UDP0 and P80/UDM0 pins are used as GPIO (P81, P80)

*3: When P83/UDP1 and P82/UDM1 pins are used as USB (UDP1, UDM1)

*4: When P83/UDP1 and P82/UDM1 pins are used as GPIO (P83, P82)

*5: The maximum temperature of the ambient temperature (T_A) can guarantee a range that does not exceed the junction temperature (T_J).

The calculation formula of the ambient temperature (T_A) is:

$T_A (Max) = T_J(Max) - Pd(Max) \times \theta_{JA}$

Pd: Power dissipation (W)
θ_{JA}: Package thermal resistance (°C/W)

$Pd (Max) = V_{CC} \times I_{CC} (Max) + \Sigma (I_{OL} \times V_{OL}) + \Sigma ((V_{CC} - V_{OH}) \times (- I_{OH}))$

I_{OL}: L level output current
I_{OH}: H level output current
V_{OL}: L level output voltage
V_{OH}: H level output voltage

*6: The minimum value of analog reference voltage depends on the value of compare clock cycle (t_{CCK}). See 12.5. 12-bit A/D Converter for the details.

*7: For the voltage range between V_{cc}(min) and the low voltage detection reset (VDH), the MCU must be clocked from either the High-speed CR or the low-speed CR."

Table 12-8 Typical and Maximum Current Consumption in Stop Mode, Timer Mode and RTC Mode

Parameter	Symbol	Pin Name	Conditions	Frequency	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCH}	VCC	Stop mode	-	0.56	3.01	mA	*3, *4 T_A = +25°C
					-	27.03	mA	*3, *4 T_A = +85°C
					-	39.92	mA	*3, *4 T_A = +105°C
	I_{CCT}		Timer mode*5 (main oscillation)	4 MHz	1.40	3.85	mA	*3, *4 T_A = +25°C
					-	27.87	mA	*3, *4 T_A = +85°C
					-	40.76	mA	*3, *4 T_A = +105°C
			Timer mode (built-in High-speed CR)	4 MHz	0.95	3.40	mA	*3, *4 T_A = +25°C
					-	27.42	mA	*3, *4 T_A = +85°C
					-	40.31	mA	*3, *4 T_A = +105°C
			Timer mode*6 (sub oscillation)	32 kHz	0.57	3.02	mA	*3, *4 T_A = +25°C
					-	27.04	mA	*3, *4 T_A = +85°C
					-	39.93	mA	*3, *4 T_A = +105°C
			Timer mode (built-in Low-speed CR)	100 kHz	0.58	3.03	mA	*3, *4 T_A = +25°C
					-	27.05	mA	*3, *4 T_A = +85°C
					-	39.94	mA	*3, *4 T_A = +105°C
	I_{CCR}		RTC mode*6 (sub oscillation)	32 kHz	0.57	3.02	mA	*3, *4 T_A = +25°C
					-	27.04	mA	*3, *4 T_A = +85°C
					-	39.93	mA	*3, *4 T_A = +105°C

*1: V_{CC} = 3.3V

*2: V_{CC} = 5.5V

*3: When all ports are fixed

*4: When LVD is off

*5: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

*6: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)

12.4 AC Characteristics

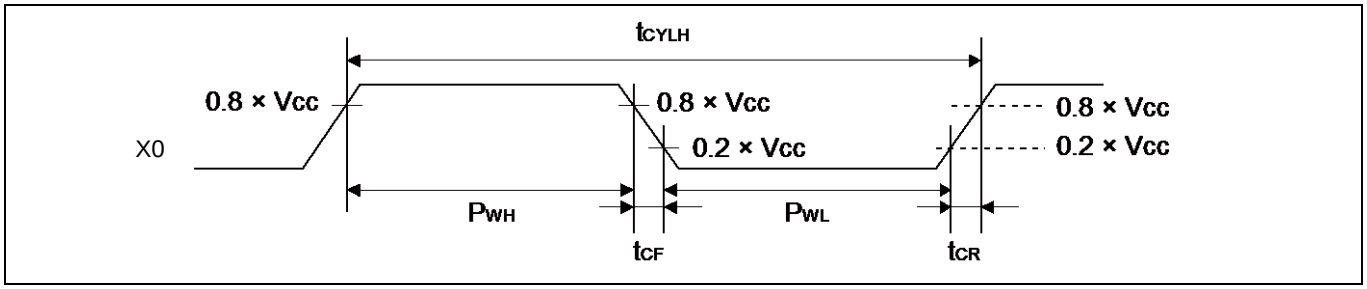
12.4.1 Main Clock Input Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, Ta = -40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{CH}	X0, X1	V_{CC} ≥4.5 V	4	48	MHz	When crystal oscillator is connected
			V_{CC} < 4.5 V	4	20		
			V_{CC} ≥4.5 V	4	48	MHz	When using external clock
			V_{CC} < 4.5 V	4	20		
Input clock cycle	t_{CYLH}		V_{CC} ≥4.5 V	20.83	250	ns	When using external clock
			V_{CC} < 4.5 V	50	250		
Input clock pulse width	-		P_{WH}/t_{CYLH}, P_{WL}/t_{CYLH}	45	55	%	When using external clock
Input clock rise time and fall time	t_{CF}, t_{CR}		-	-	5	ns	When using external clock
Internal operating clock *1 frequency	f_{CC}	-	-	-	200	MHz	Base clock (HCLK/FCLK)
	f_{CP0}	-	-	-	100	MHz	APB0bus clock *2
	f_{CP1}	-	-	-	200	MHz	APB1bus clock *2
	f_{CP2}	-	-	-	100	MHz	APB2bus clock *2
Internal operating clock *1 cycle time	t_{CYCC}	-	-	5	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	10	-	ns	APB0bus clock *2
	t_{CYCP1}	-	-	5	-	ns	APB1bus clock *2
	t_{CYCP2}	-	-	10	-	ns	APB2bus clock *2

*1: For more information about each internal operating clock, see "CHAPTER 2-1: Clock" in FM4 Family Peripheral Manual Main Part (002-04856).

*2: For more about each APB bus to which each peripheral is connected, see 8. Block Diagram in this data sheet.



12.4.8 Power-On Reset Timing

(V_{SS} = 0V)

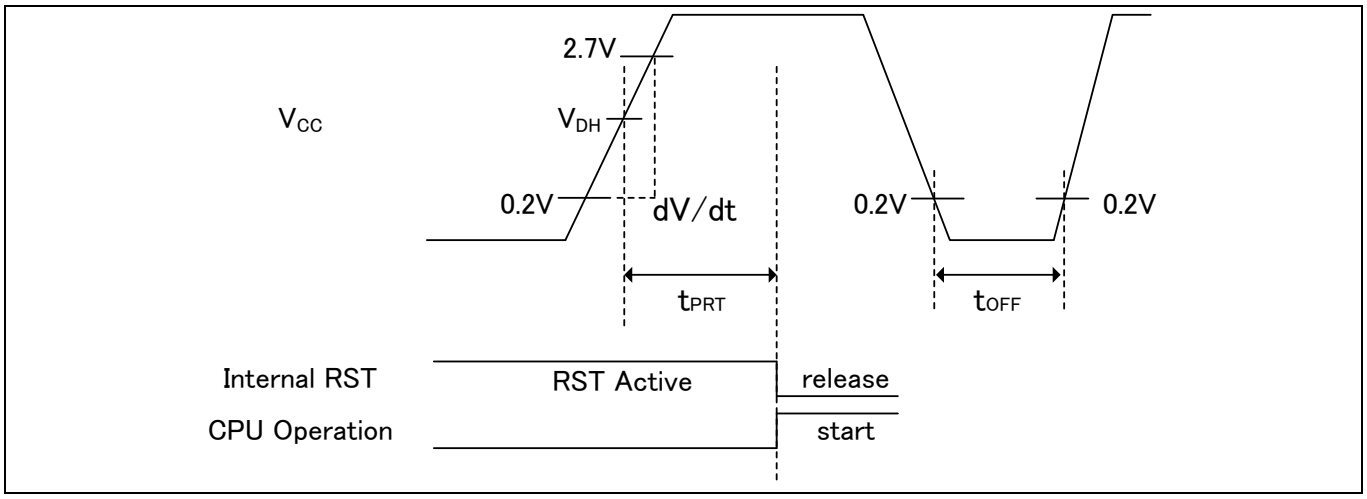
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply shut down time	t_{OFF}	VCC	-	1	-	-	ms	*1
Power ramp rate	dV/dt		V_{CC}: 0.2V to 2.70V	0.6	-	1000	mV/µs	*2
Time until releasing Power-on reset	t_{PRT}		-	0.33	-	0.60	ms	

*1: V_{CC} must be held below 0.2V for a minimum period of t_{OFF}. Improper initialization may occur if this condition is not met.

*2: This dV/dt characteristic is applied at the power-on of cold start (t_{OFF}>1ms).

Note:

- *If t_{OFF} cannot be satisfied designs must assert external reset(INITX) at power-up and at any brownout event per 12. 4. 7.*



Glossary

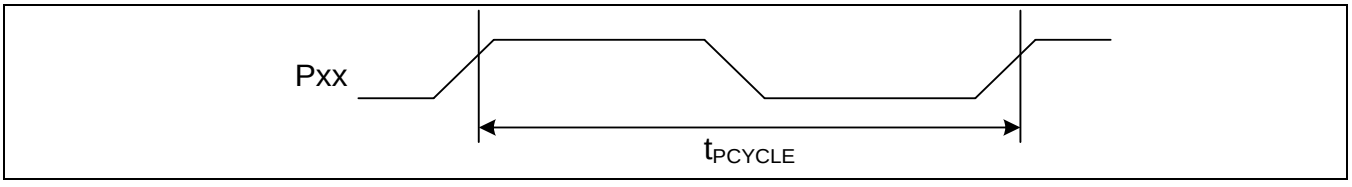
- V_{DH}: detection voltage of Low Voltage detection reset. See “12.8. Low-Voltage Detection Characteristics”.

12.4.9 GPIO Output Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Typ		
Output frequency	t_{PCYCLE}	Pxx*	V_{CC} ≥ 4.5 V	-	50	MHz	
			V_{CC} < 4.5 V	-	32	MHz	

*: GPIO is a target.



12.4.10 External Bus Timing

External Bus Clock Output Characteristics

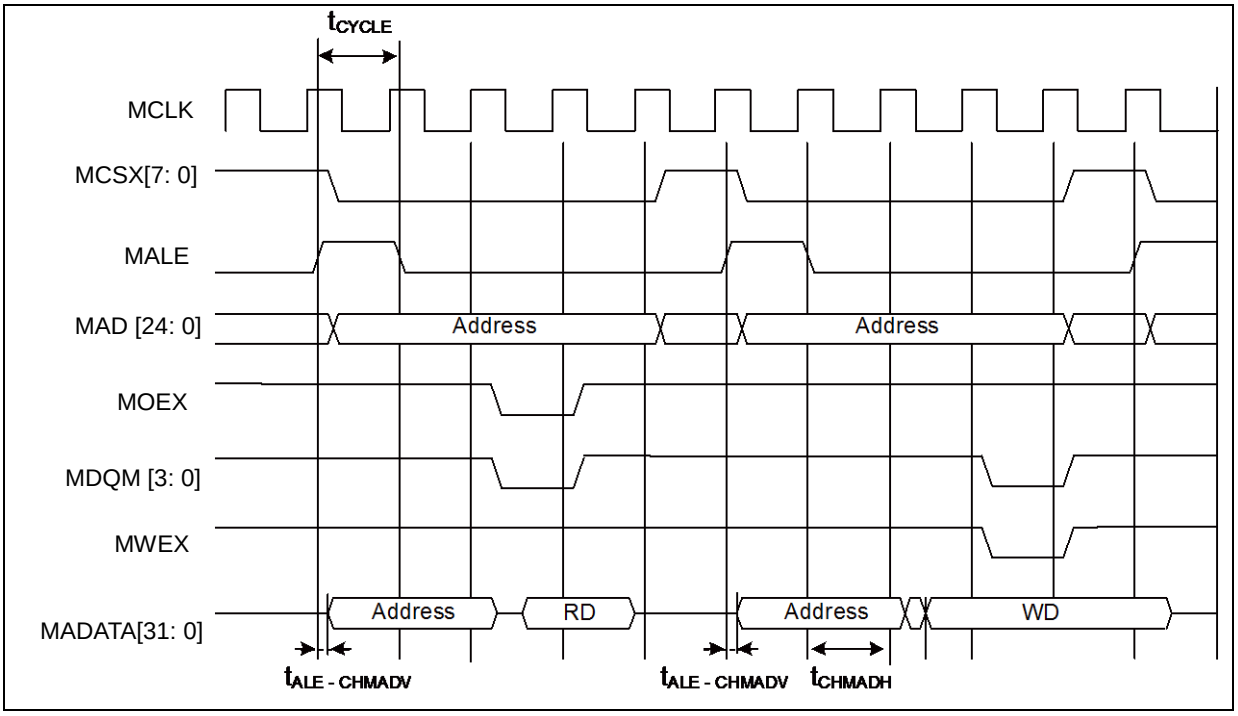
Multiplexed Bus Access Asynchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Multiplexed address delay time	$t_{ALE-CHMADV}$	MALE, MAD[24: 0]	-	0	10	ns	
Multiplexed address hold time	t_{CHMADH}		-	MCLK×n+0	MCLK×n+10	ns	

Note:

- *When the external load capacitance C_L = 30 pF (m = 0 to 15, n = 1 to 16)*



12.4.12 CSIO (SPI) Timing

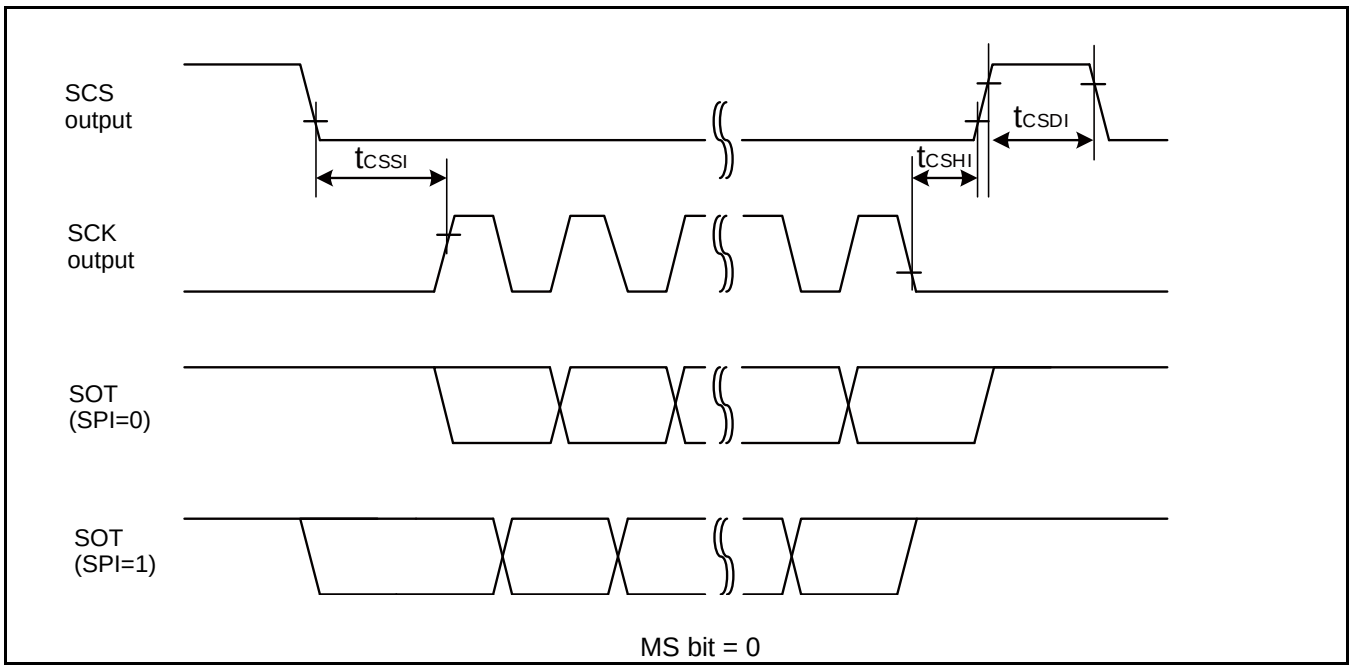
Synchronous Serial (SPI = 0, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

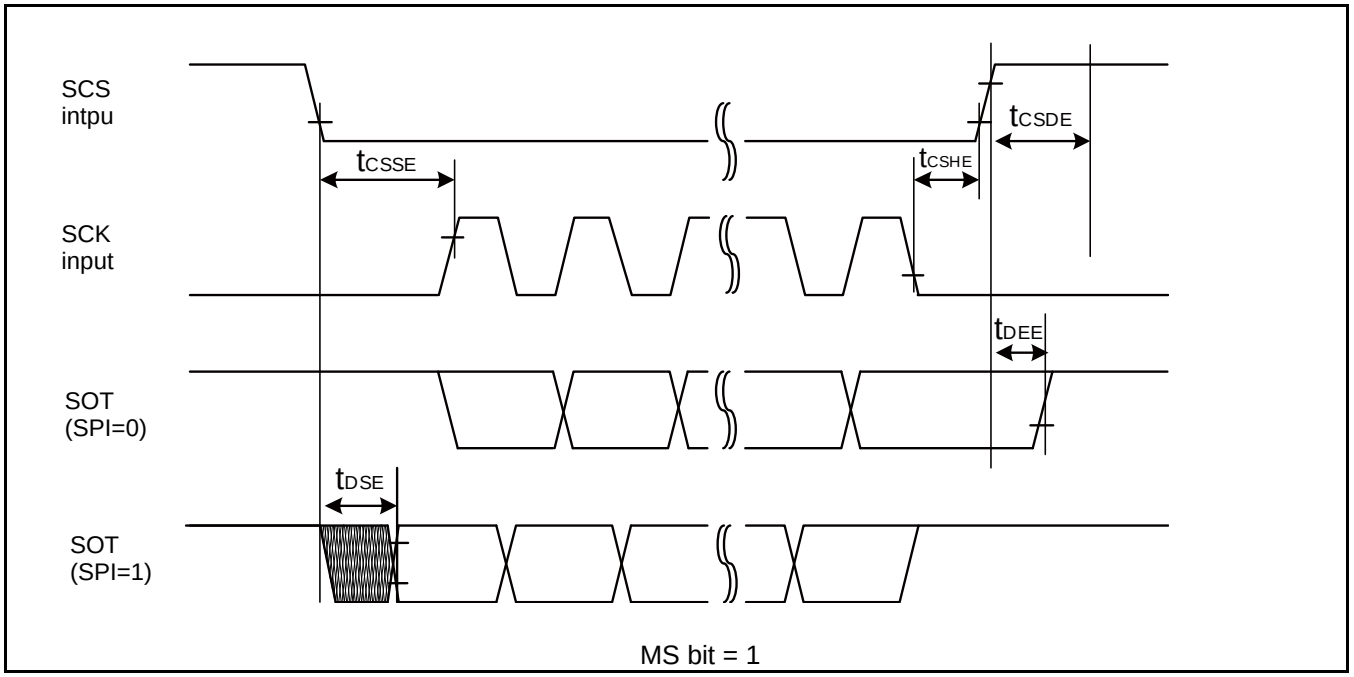
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-		-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK fall time	tF	SCKx		-	5	-	5	ns
SCK rise time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.*
- *These characteristics only guarantee the same relocate port number; for example, the combination of SCKx_0 and SOTx_1 is not guaranteed.*
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0



MS bit = 1

When Using High-Speed Synchronous Serial Chip Select (SCINV = 0, CSLVL = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t_{CSDI}		(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	ns
SCS↑→SCK↓ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCK↑→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCS↑→SOT delay time	t_{DSE}		-	25	-	25	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.*
- *For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*

Slave Mode Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{SCYC}	I2SCK	-	-	12.288	MHz	
Input clock pulse width	t_{SHW}	I2SCK	-	45	55	%	
	t_{SLW}			45	55	%	
I2SWS→I2SCK Setup time	t_{SFI}	I2SCK, I2SWS	-	8	-	ns	
I2SWS→I2SCK Hold time	t_{HFI}	I2SCK, I2SWS	-	0	-	ns	
I2SCK ↑ →I2SDO Delay time*1	t_{DDO}	I2SCK, I2SDO	-	0	32	ns	
I2SCK ↑ →I2SDO Delay time*2	t_{DFB1}		-	0	32	ns	
I2SDI→I2SCK ↓ Setup time	t_{SDI}	I2SCK, I2SDI	-	8	-	ns	
I2SDI→I2SCK ↓ Hold time	t_{HDI}		-	0	-	ns	
Input signal rise time	t_{FI}	I2SCK, I2SWS, I2SDI	-	-	5	ns	
Input signal fall time	t_{FI}		-	-	5	ns	

*1: Except for the first bit of transmission frame

*2: When FSPH bit = 1.

Notes:

- *When the external load capacitance C_L = 20 pF*
- *When I2SWS = 48 kHz, I2MCLK = 256 ×I2SWS*
  Frame synchronization signal (I2SWS) is settable to 48 kHz, 32 kHz, 16 kHz. See Chapter7-2: I^2S (Inter-IC Sound bus) Interface in FM4 Family Peripheral Manual Communication Macro Part (002-04862) for the details.

12.4.20 High-Speed Quad SPI Timing

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock frequency	t_{SCYCM}	Q_SCK_0	C_L = 15 pF, V_{CC} = 3.0 to 3.6V	-	66	MHz	*1
			C_L = 30 pF	-	50	MHz	*2
Enabled CS→ CLK Starting Time (mode0/mode2)	$t_{OSLSK02}$	Q_SCK_0, Q_CS0_0, Q_CS1_0, Q_CS2_0	C_L = 30 pF	$1.5 \times t_{SCYCM}$ - 5	-	ns	
Enabled CS→ CLK Starting Time (mode1/mode3)	$t_{OSLSK13}$			t_{SCYCM} - 5	-	ns	
CLK Last→ Disabled CS Time (mode0/mode2)	$t_{OSKSL02}$			t_{SCYCM}	-	ns	
CLK Last→ Disabled CS Time (mode1/mode3)	$t_{OSKSL13}$			$1.5 \times t_{SCYCM}$	-	ns	
SIO Data output time	t_{OSDAT}	Q_SCK_0, Q_IO0_0, Q_IO1_0, Q_IO2_0, Q_IO3_0	C_L = 15 pF, V_{CC} = 3.0 to 3.6V	0	5	ns	
			C_L = 30 pF	0	5		
SIO Setup	t_{DSSET}		C_L = 30 pF	3	-	ns	*1
				10	-		*2
SIO Hold	t_{SDHOLD}		C_L = 30 pF	$0.5 \times t_{SCYCM}$	-	ns	

*1: When RTM = 1 and mode = 0, 1, 3

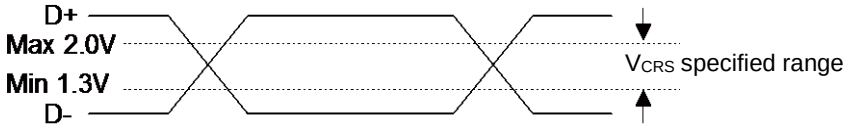
*2: When RTM = 1 and mode = 2 or RTM = 0 and mode = 0, 1, 2, 3

Notes:

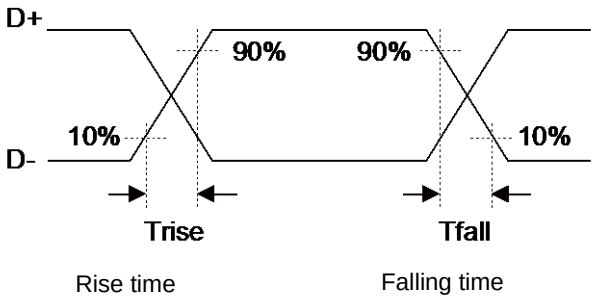
- *See Chapter8-3: High-Speed Quad SPI controller in FM4 Family Peripheral Manual Communication Macro Part (002-04862) for the detail of RTM mode.*
- *When using High-Speed Quad SPI, please set PDSR register to set the pin drive capability for V_{CC} = 3V. See Chapter12: I/O Port in FM4 Family Peripheral Manual Main Part (002-04856) for the details.*

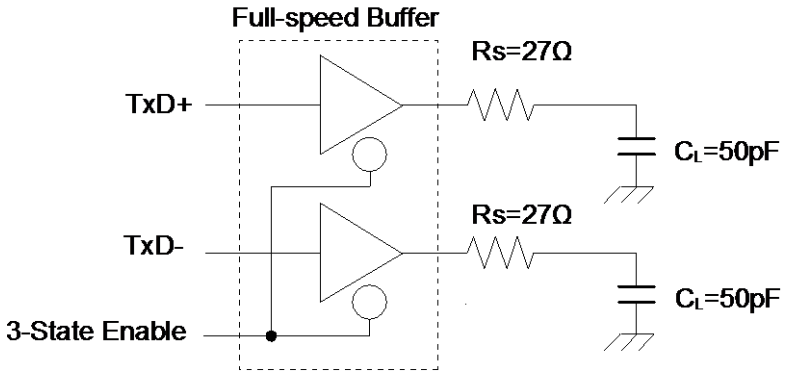
*3: The output drive capability of the driver is below 0.3 V at low state (V_{OL}) (to 3.6 V and 1.5 kΩ load), and 2.8 V or above (to the VSS and 1.5 kΩ load) at high state (V_{OH}).

*4: The cross voltage of the external differential output signal (D +/D −) of USB I/O buffer is within 1.3 V to 2.0 V.

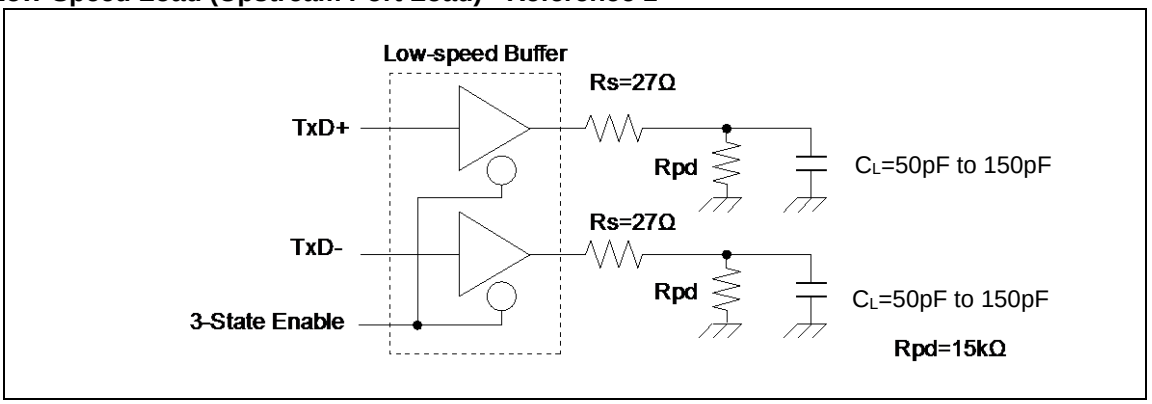


*5: They indicate rise time (Trise) and fall time (Tfall) of the full-speed differential data signal.
They are defined by the time between 10% and 90% of the output signal voltage.
For full-speed buffer, Tr/Tf ratio is regulated as within ± 10% to minimize RFI emission.

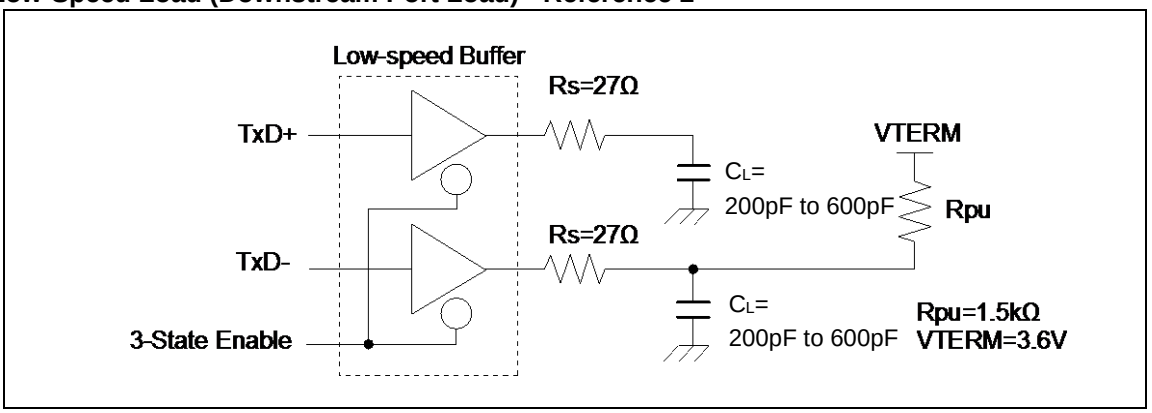




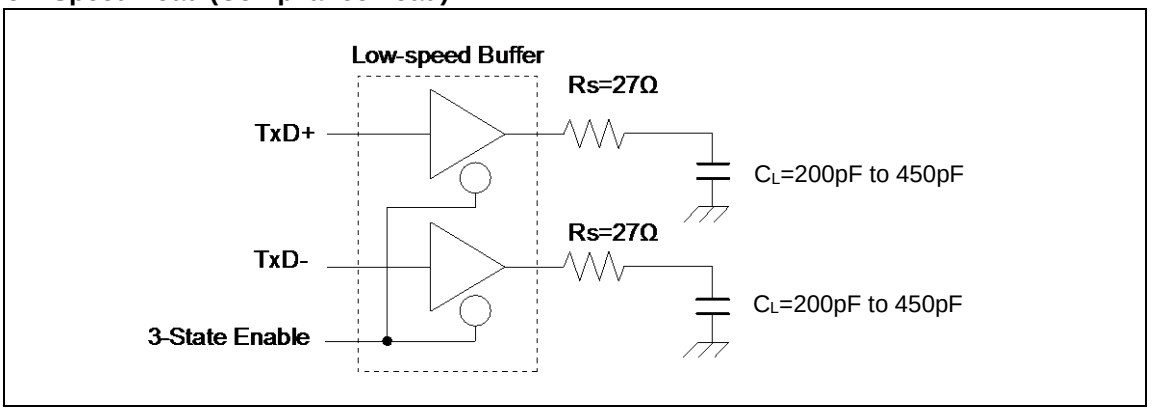
Low-Speed Load (Upstream Port Load) - Reference 1



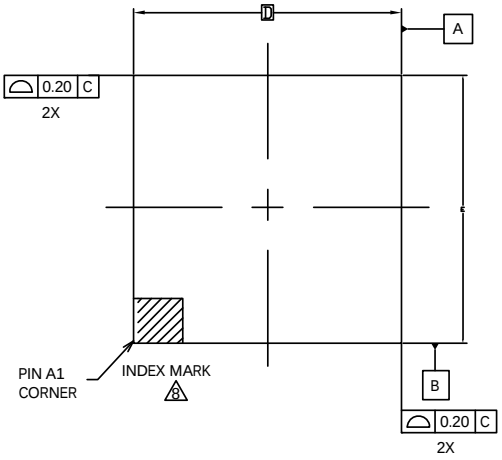
Low-Speed Load (Downstream Port Load) - Reference 2



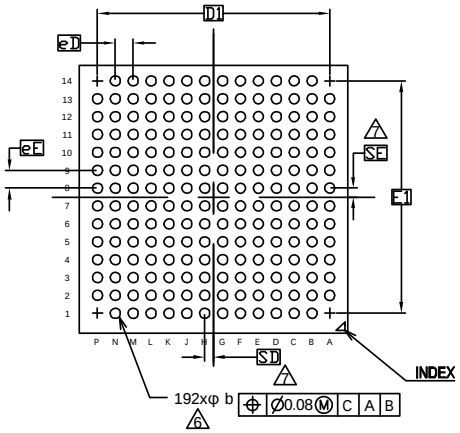
Low-Speed Load (Compliance Load)



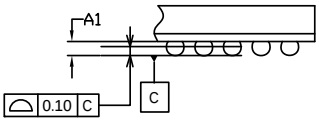
Package Type	Package Code
PFBGA 192	LBE 192



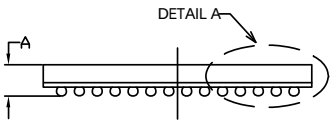
TOP VIEW



BOTTOM VIEW



DETAIL A



SIDE VIEW

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	1.45
A1	0.25	0.35	0.45
D	12.00 BSC		
E	12.00 BSC		
D1	10.40 BSC		
E 1	10.40 BSC		
MD	14		
ME	14		
n	192		
Φb	0.35	0.45	0.55
eD	0.80 BSC		
eE	0.80 BSC		
SD / SE	0.40 BSC		

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS AND TOLERANCES METHODS PER ASME Y14.5-2009. THIS OUTLINE CONFORMS TO JEP95, SECTION 4.5.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-010.
4. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" =0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK. METALLIZED MARK INDENTATION OR OTHER MEANS.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

002-13493 **

PACKAGE OUTLINE, 192 BALL FBGA
12.00X12.00X1.45 MM LBE192 REV**