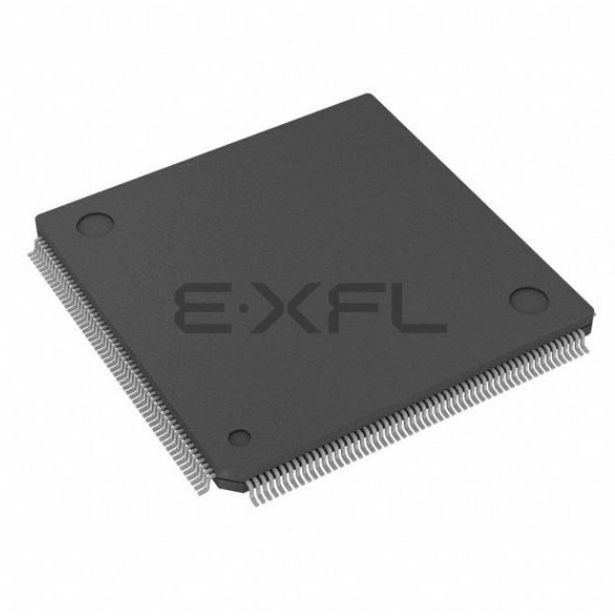

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CSIO, EBI/EMI, I²C, LINbus, SD, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	190
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	216-LQFP
Supplier Device Package	216-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2c3al0agl2000a

Notes:

- *All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use.*
- *See 12.4.3 Built-In CR Oscillation Characteristics for the accuracy of the built-in CR.*

2. Packages

Package \ Product Name	S6E2C38H0A S6E2C39H0A S6E2C3AH0A	S6E2C38J0A S6E2C39J0A S6E2C3AJ0A	S6E2C38L0A S6E2C39L0A S6E2C3AL0A
LQFP: LQS144 (0.5-mm pitch)	❍	-	-
LQFP: LQP176 (0.5-mm pitch)	-	❍	-
BGA : LBE192 (0.8-mm pitch)	-	❍	-
LQFP: LQQ216 (0.4-mm pitch)	-	-	❍

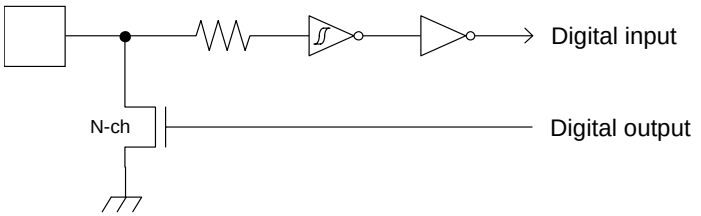
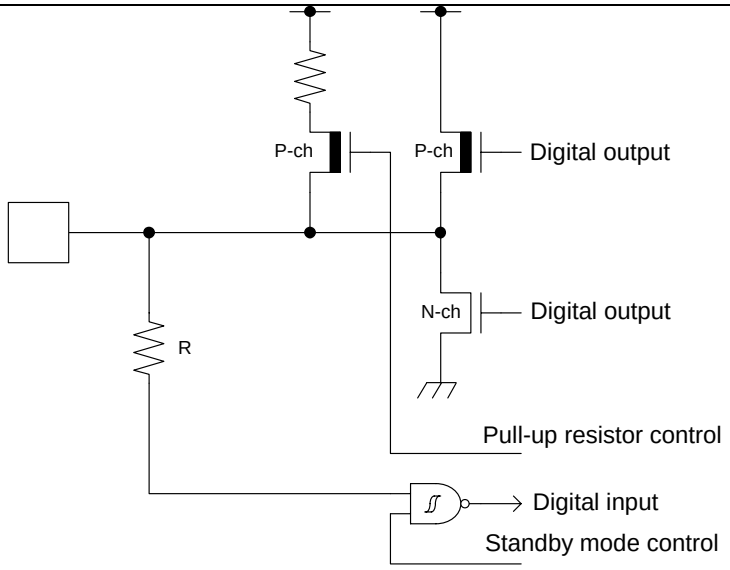
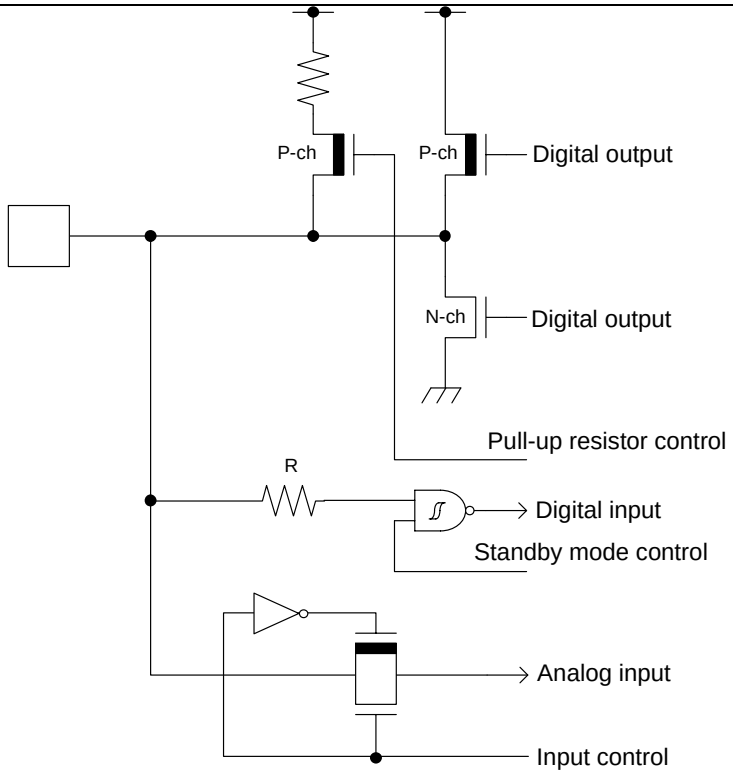
❍: Supported

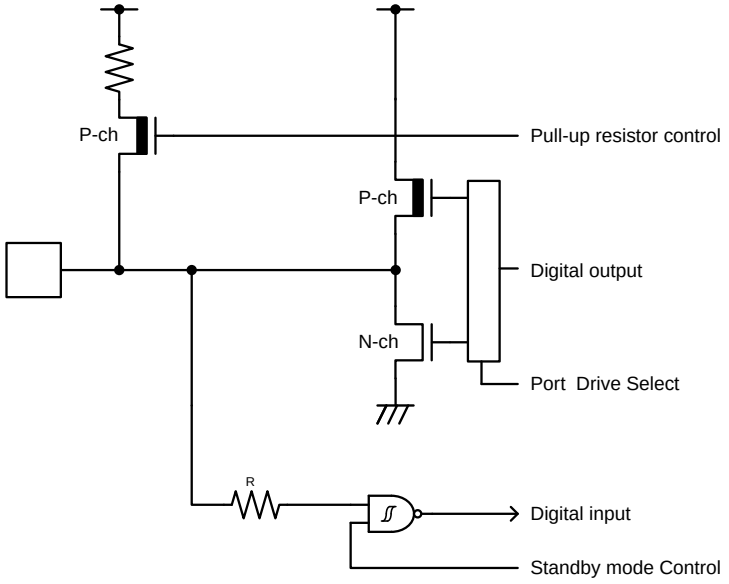
Note:

- *See 14. Package Dimensions for detailed information on each package.*

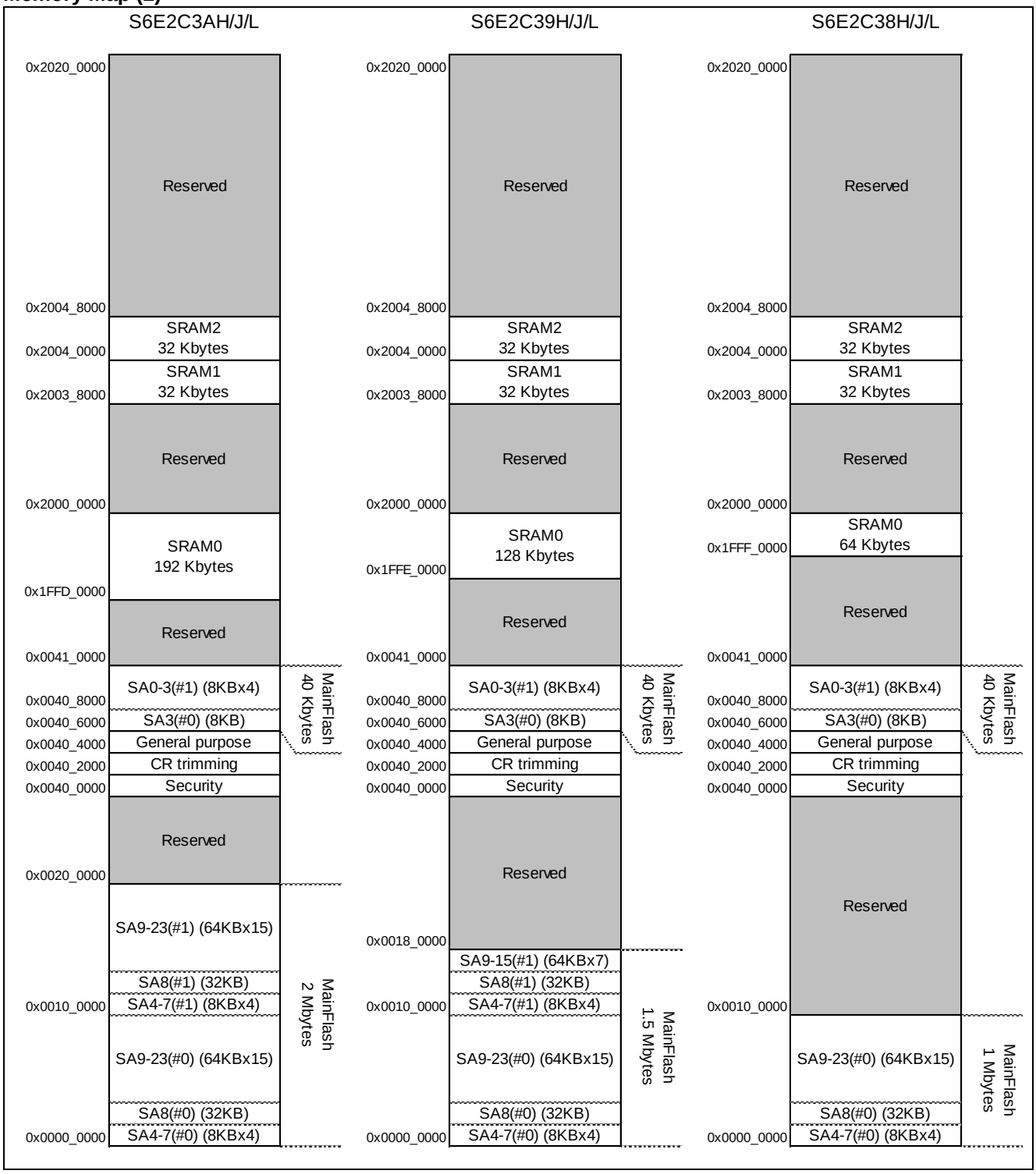
Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
115	95	79	K13	P11 AN01 SOT10_0 (SDA10_0) TIOB0_2 BIN0_2	F	L
116	96	80	K12	P12 AN02 SCK10_0 (SCL10_0) TIOA1_2 ZIN0_2	F	L
117	97	81	K14	P13 AN03 SIN6_1 INT25_1	F	M
118	98	82	K11	P14 AN04 SOT6_1 (SDA6_1)	F	L
119	-	-	-	PB8 ADTG_6 SCS63_1 INT08_2 TRACED8	E	O
120	-	-	-	PB9 SIN9_1 AIN2_2 INT09_2 TRACED9	E	O
121	-	-	-	PBA SOT9_1 (SDA9_1) BIN2_2 TRACED10	E	N
122	-	-	-	PBB SCK9_1 (SCL9_1) ZIN2_2 TRACED11	E	N
123	99	83	J13	P15 AN05 SIN11_0 TIOB1_2 AIN1_2 INT09_0	F	M
124	100	84	J12	P16 AN06 SOT11_0 (SDA11_0) TIOA2_2 BIN1_2	F	L

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	P70	General-purpose I/O port 7	80	65	55	L6
	P71		81	66	56	J6
	P72		82	67	57	L8
	P73		83	68	58	K8
	P74		84	69	59	J8
	P75		91	76	60	K9
	P76		92	77	61	P10
	P77		93	78	62	N10
	P78		96	79	63	L10
	P79		97	80	64	K10
	P7A		98	81	65	M10
	P7B		99	82	66	N11
	P7C		100	83	67	M11
	P7D		70	55	47	L5
	P7E		71	56	48	M5
	P80	General-purpose I/O port 8	214	174	142	A3
	P81		215	175	143	A2
	P82		160	130	106	D14
	P83		161	131	107	C14
	P90	General-purpose I/O port 9	169	139	-	C11
	P91		170	140	-	D11
	P92		171	141	-	B10
	P93		172	142	-	C10
	P94		173	143	-	D10
	P95		174	144	-	B9
	P96		175	-	-	-
	P97		176	-	-	-

Type	Circuit	Remarks
C		• Open drain output • CMOS level hysteresis input
E		• CMOS level output • CMOS level hysteresis input • Pull-up resistor control • Standby mode control • Pull-up resistor: approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.
F		• CMOS level output • CMOS level hysteresis input • Input control • Analog input • Pull-up resistor control • Standby mode control • Pull-up resistor: approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.

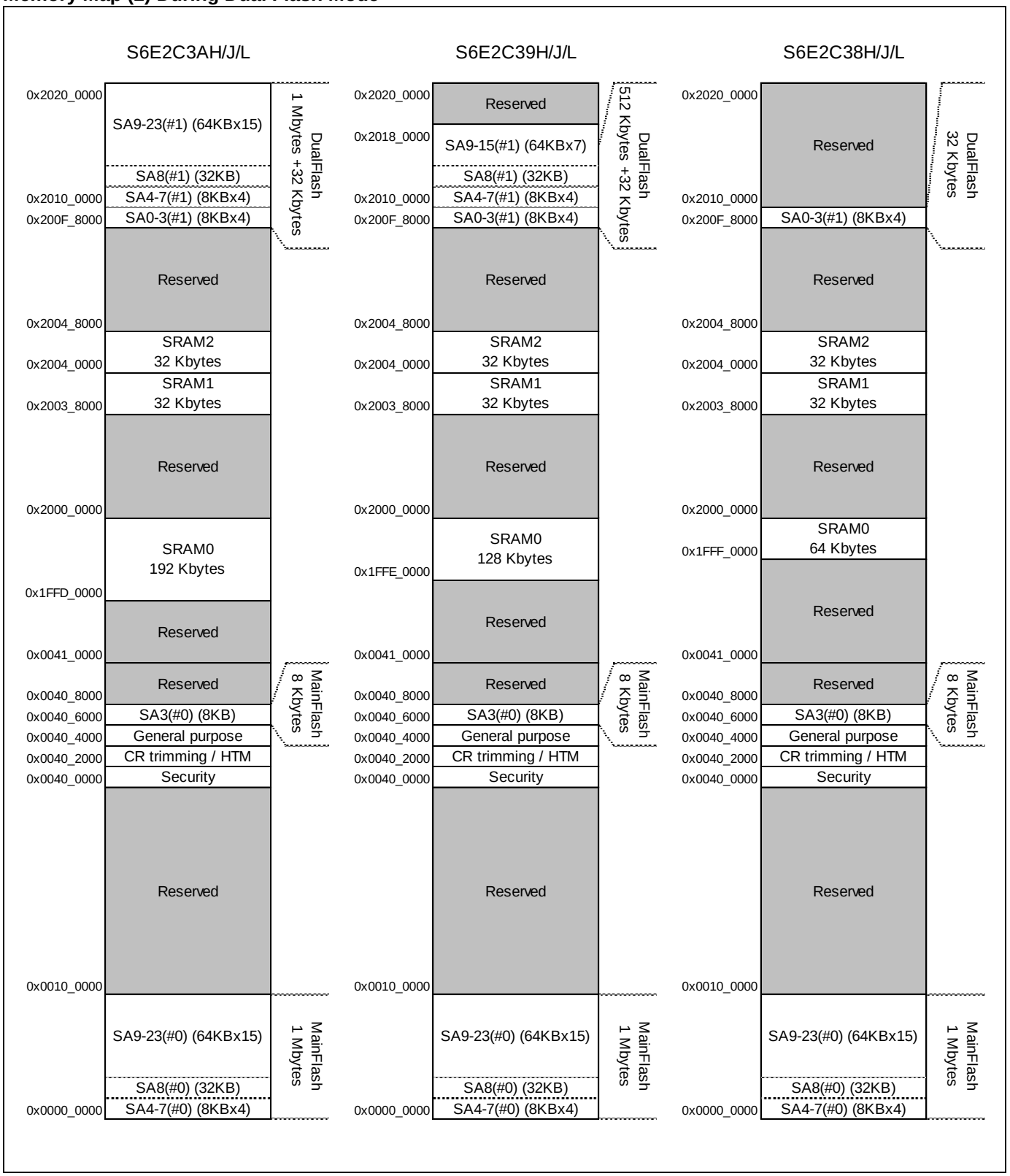
Type	Circuit	Remarks
S		・CMOS level output ・(It is possible to select by port drive capability. Select register [PDSR]) ・CMOS level hysteresis input ・Pull-up resistor control ・Standby mode control ・Pull-up resistor: approximately 50 kΩ ・I_{OH} = -10 mA, I_{OL} = 10 mA (PDSR = 1) ・I_{OH} = -4 mA, I_{OL} = 4 mA (PDSR = 0) ・When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.

Memory Map (2)



*: See S6E2CC/S6E2C5/S6E2C4/S6E2C3/S6E2C2/S6E2C1 Series Flash Programming Manual to confirm the detail of flash Memory.

Memory Map (2) During Dual Flash Mode



Peripheral Address Map

Start Address	End Address	Bus	Peripherals
0x4000_0000	0x4000_0FFF	AHB	MainFlash I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/reset control
0x4001_1000	0x4001_1FFF		Hardware watchdog timer
0x4001_2000	0x4001_2FFF		Software watchdog timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual-timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-Function Timer unit 0
0x4002_1000	0x4002_1FFF		Multi-Function Timer unit 1
0x4002_2000	0x4002_2FFF		Multi-Function Timer unit 2
0x4002_3000	0x4002_3FFF		Reserved
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base timer
0x4002_6000	0x4002_6FFF		Quadrature position/revolution counter
0x4002_7000	0x4002_7FFF		A/D converter
0x4002_8000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Internal CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF	APB2	External interrupt controller
0x4003_1000	0x4003_1FFF		Interrupt request batch-read function
0x4003_2000	0x4003_2FFF		Reserved
0x4003_3000	0x4003_3FFF		D/A converter
0x4003_4000	0x4003_4FFF		Reserved
0x4003_5000	0x4003_57FF		Low voltage detector
0x4003_5800	0x4003_5FFF		Deep standby mode Controller
0x4003_6000	0x4003_6FFF		USB clock generator
0x4003_7000	0x4003_7FFF		Reserved
0x4003_8000	0x4003_8FFF		Multi-function serial interface
0x4003_9000	0x4003_9FFF		CRC
0x4003_A000	0x4003_AFFF		Watch counter
0x4003_B000	0x4003_BFFF		RTC/port control
0x4003_C000	0x4003_C0FF		Low-speed CR prescaler
0x4003_C100	0x4003_C7FF		Peripheral clock gating
0x4003_C800	0x4003_CFFF		Reserved
0x4003_D000	0x4003_DFFF		I^2S prescaler
0x4003_E000	0x4003_EFFF		Reserved
0x4003_F000	0x4003_FFFF		External memory interface
0x4004_0000	0x4004_FFFF	AHB	USB ch 0
0x4005_0000	0x4005_FFFF		USB ch 1
0x4006_0000	0x4006_0FFF		DMAC register
0x4006_1000	0x4006_1FFF		DSTC register
0x4006_2000	0x4006_BFFF		Reserved
0x4006_C000	0x4006_CFFF		I^2S
0x4006_D000	0x4006_DFFF		Reserved
0x4006_E000	0x4006_EFFF		SD card I/F
0x4006_F000	0x4006_FFFF		GPIO
0x4007_0000	0x4007_FFFF		Reserved
0x4008_0000	0x4008_0FFF		Programmable-CRC
0x4008_1000	0x41FF_FFFF		Reserved
0x200E_0000	0x200E_FFFF		Workflash I/F register
0xD000_0000	0xDFFF_FFFF		High-speed quad SPI control register

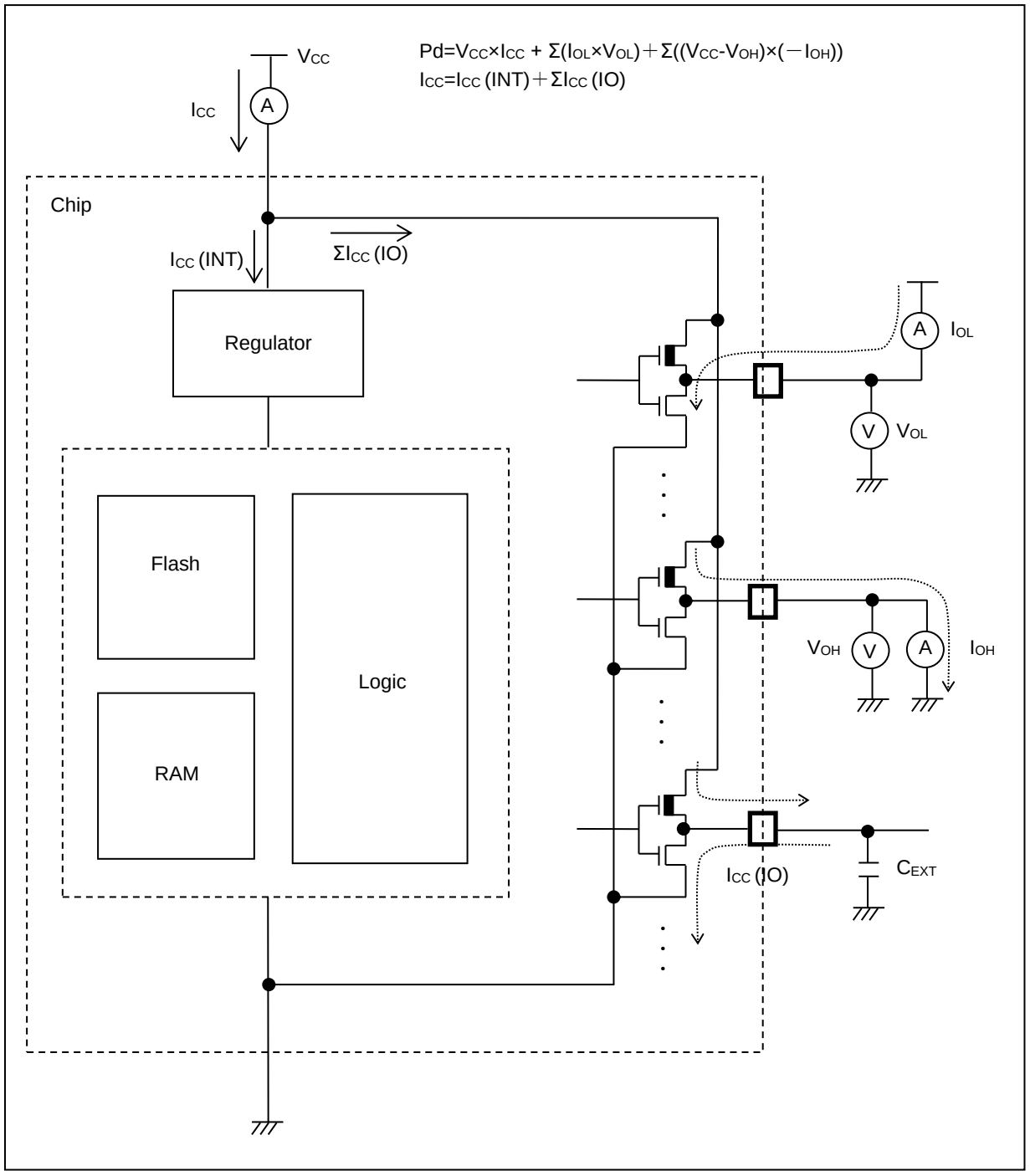
List of VBAT Domain Pin Status

VBAT Pin Status Type	Function Group	Power-on reset*1	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return From Deep Standby Mode State	VBAT RTC Mode State	Return From VBAT RTC Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable	Power Supply Stable	Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1	-	-
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-	-	-
S	GPIO selected	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Setting prohibition	-
	Sub crystal oscillator input pin/ external sub clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Maintain previous state	Maintain previous state
T	GPIO selected	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Setting prohibition	-
	External sub clock input selected	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	Sub crystal oscillator output pin	Hi-Z/ internal input fixed at 0/ or input enable	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state/ When oscillation stops, Hi-Z*2	Maintain previous state/ When oscillation stops, Hi-Z*2	Maintain previous state/ When oscillation stops, Hi-Z*2	Maintain previous state/ When oscillation stops, Hi-Z*2	Maintain previous state	Maintain previous state	Maintain previous state
U	Resource selected	Hi-Z	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected											

*1: When VBAT and VCC power on.

*2: When the SOSCNTL bit in the WTOSCCNT register is 0, the sub crystal oscillator output pin is maintained in the previous state. When the SOSCNTL bit in the WTOSCCNT register is 1, oscillation is stopped at Stop mode and Deep Standby Stop mode

Current Explanation Diagram



12.4.4 Operating Conditions of Main PLL (in the Case of Using Main Clock for Input Clock of PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (lock up time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiplication rate	-	13	-	100	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	200	-	400	MHz	
Main PLL clock frequency*2	f_{CLKPLL}	-	-	200	MHz	

*1: Time from when the PLL starts operating until the oscillation stabilizes

*2: For more information about Main PLL clock (CLKPLL), see Chapter 2-1: Clock in FM4 Family Peripheral Manual Main Part (002-04856).

12.4.5 Operating Conditions of USB PLL・I²S PLL (in the Case of Using Main Clock for Input Clock of PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (lock up time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiplication rate	-	13	-	100	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	200	-	400	MHz	USB
				384	MHz	I²S
USB clock frequency *2	f_{CLKPLL}	-	-	50	MHz	After the M frequency division
I²S clock frequency *3	f_{CLKPLL}	-	-	12.288	MHz	After the M frequency division

*1: Time from when the PLL starts operating until the oscillation stabilizes

*2: For more information about USB/Ethernet clock, see Chapter 2-2: USB/Ethernet Clock Generation in FM4 Family Peripheral Manual Communication Macro Part (002-04862).

*3: For more information about I²S clock, see Chapter 7-1: I²S Clock Generation in FM4 Family Peripheral Manual Communication Macro Part (002-04862).

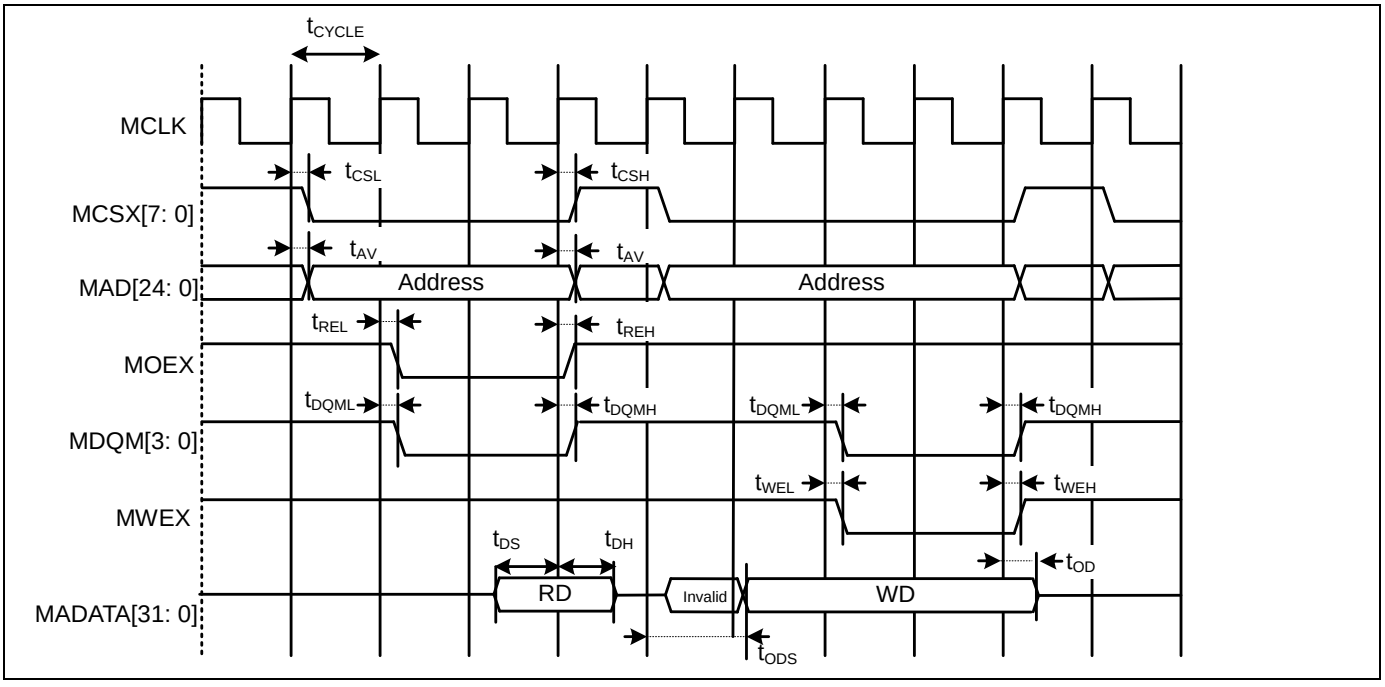
Separate Bus Access Synchronous SRAM Mode

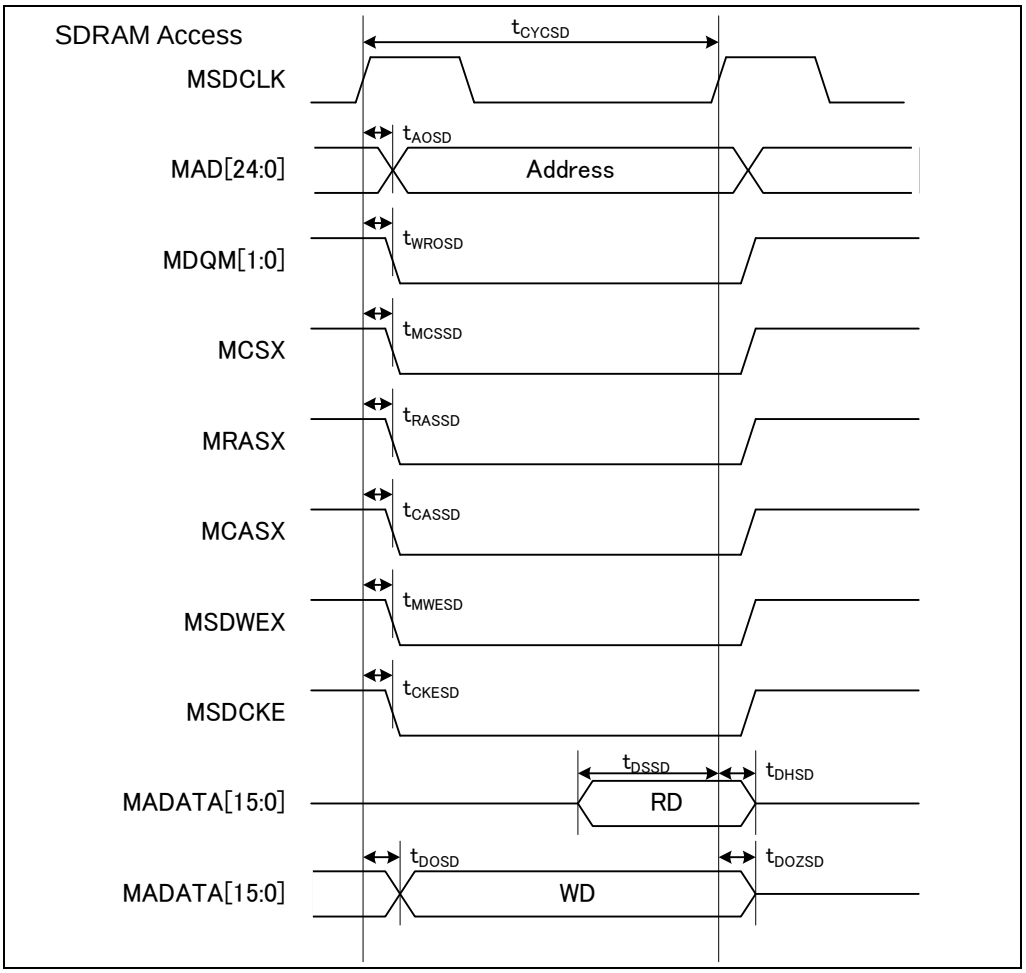
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Address delay time	t_{AV}	MCLK, MAD[24: 0]	-	1	9	ns	
MCSX delay time	t_{CSL}	MCLK, MCSX[7: 0]	-	1	9	ns	
	t_{CSH}		-	1	9	ns	
MOEX delay time	t_{REL}	MCLK, MOEX	-	1	9	ns	
	t_{REH}		-	1	9	ns	
Data set up →MCLK ↑ time	t_{DS}	MCLK, MADATA[31: 0]	-	19	-	ns	
MCLK ↑ → Data hold time	t_{DH}	MCLK, MADATA[31: 0]	-	0	-	ns	
MWEX delay time	t_{WEL}	MCLK, MWEX	-	1	9	ns	
	t_{WEH}		-	1	9	ns	
MDQM[1: 0] delay time	t_{DQML}	MCLK, MDQM[3: 0]	-	1	9	ns	
	t_{DQMH}		-	1	9	ns	
MCLK ↑ → Data output time	t_{ODS}	MCLK, MADATA[31: 0]	-	MCLK+1	MCLK+18	ns	
MCLK ↑ → Data hold time	t_{OD}	MCLK, MADATA[31: 0]	-	1	18	ns	

Note:

- *When the external load capacitance C_L = 30 pF*




SDRAM Access
MSDCLK
MAD[24:0]
MDQM[1:0]
MCSX
MRASX
MCASX
MSDWEX
MSDCKE
MADATA[15:0]
MADATA[15:0]
tCYCSD
tAOSD
Address
tWROSD
tMCSSD
tRASSD
tCASSD
tMWESD
tCKESD
tDSSD
tDHSD
RD
tDOSD
tDOZSD
WD

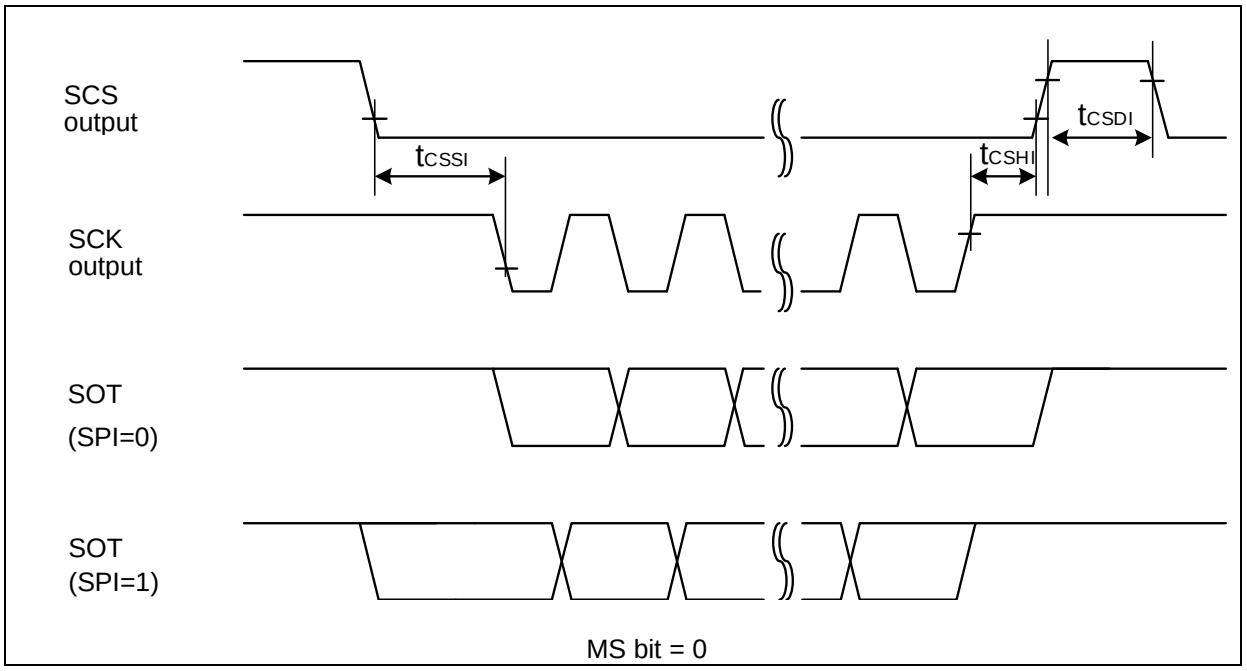
Synchronous Serial (SPI = 1, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

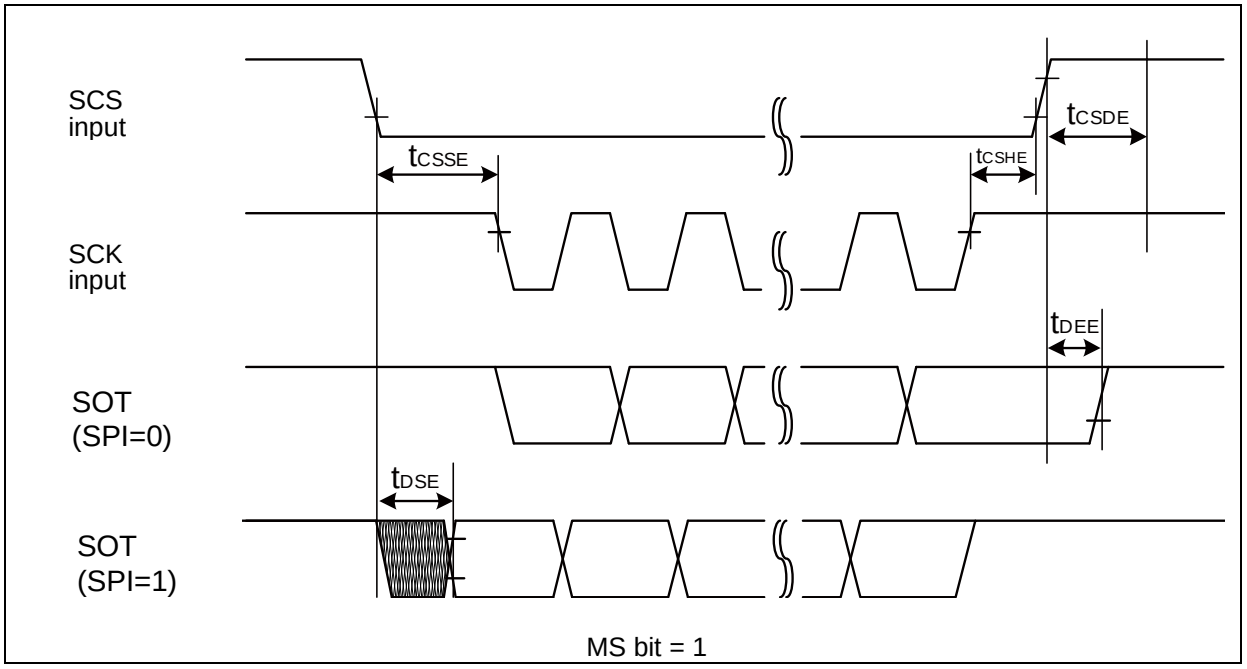
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
SOT→SCK↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK fall time	t_F	SCKx		-	5	-	5	ns
SCK rise time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.*
- *These characteristics only guarantee the same relocate port number; for example, the combination of SCKx_0 and SOTx_1 is not guaranteed.*
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0



MS bit = 1

High-Speed Synchronous Serial (SPI = 1, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		- 10	+ 10	- 10	+ 10	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		14 12.5*	-	12.5	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		5	-	5	-	ns
SOT→SCK↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 5	-	$2t_{CYCP}$ - 5	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		5	-	5	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		5	-	5	-	ns
SCK fall time	tF	SCKx		-	5	-	5	ns
SCK rise time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.*
- *These characteristics only guarantee the following pins:*

  No chip select: SIN4_0, SOT4_0, SCK4_0

  Chip select: SIN6_0, SOT6_0, SCK6_0, SCS60_0, SCS61_0, SCS62_0, SCS63_0
- *When the external load capacitance C_L = 30 pF. (for *, when C_L = 10 pF)*

12.4.13 External Input Timing

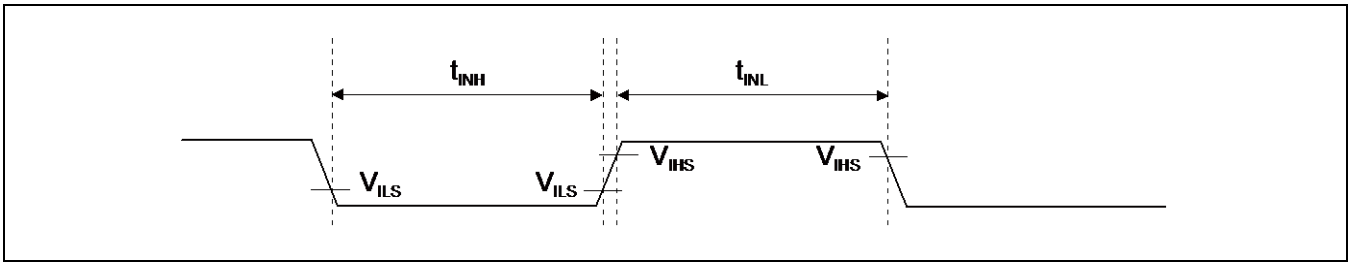
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH}, t_{INL}	ADTGx	-	$2t_{CYCP}$*1	-	ns	A/D converter trigger input
		FRCKx					Free-run timer input clock
		ICxx					Input capture
		DTTIxX	-	$2t_{CYCP}$*1	-	ns	Waveform generator
		INT00 to INT31, NMIX	-	$2t_{CYCP}$ + 100*1	-	ns	External interrupt, NMI
				500*2	-	ns	
		WKUPx	-	500*3	-	ns	Deep standby wake up

1: t_{CYCP} indicates the APB bus clock cycle time except stop when in Stop mode, in Timer mode. For more information about the APB bus number to which the A/D converter, multi-function timer, and external interrupt are connected, see 8. Block Diagram in this data sheet.

2: When in Stop mode, in Timer mode

3: When in Deep Standby RTC mode, in Deep Standby Stop mode



13. Ordering Information

Part number	Flash	RAM	Crypto	Package
S6E2C38H0AGV2000A	1 MB	128 KB	N/A	Plastic・LQFP (0.5-mm pitch), 144 pin (LQS144)
S6E2C39H0AGV2000A	1.5 MB	192 KB	N/A	
S6E2C3AH0AGV2000A	2 MB	256 KB	N/A	
S6E2C38J0AGV2000A	1 MB	128 KB	N/A	Plastic・LQFP (0.65-mm pitch), 176 pin (LQP176)
S6E2C39J0AGV2000A	1.5 MB	192 KB	N/A	
S6E2C3AJ0AGV2000A	2 MB	256 KB	N/A	
S6E2C38J0AGB1000A	1 MB	128 KB	N/A	Plastic・LQFP (0.8-mm pitch), 192 pin (LBE192)
S6E2C39J0AGB1000A	1.5 MB	192 KB	N/A	
S6E2C3AJ0AGB1000A	2 MB	256 KB	N/A	
S6E2C38L0AGL2000A	1 MB	128 KB	N/A	Plastic・LQFP (0.4-mm pitch), 216 pin (LQQ216)
S6E2C39L0AGL2000A	1.5 MB	192 KB	N/A	
S6E2C3AL0AGL2000A	2 MB	256 KB	N/A	

Document History

Document Title: S6E2C3 Series 32-bit ARM® Cortex®-M4F, FM4 Microcontroller
Document Number: 002-04988

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	AKIH	04/22/2015	New Spec.
*A	5126421	HITK	02/05/2016	Company name and layout design change. Added the note of TAP pin. Updated Package Code and Dimensions (LQFP-144, LQFP-176, LQFP-216).
*B	5634625	YSKA	02/20/2017	Deleted CAN in communications interfaces. (Page 1) Deleted CAN(RX0_2, TX0_2) in LQQ216 pin assignments (Page 12) Deleted RX2_0 in P7D in “4. Pin Descriptions” (Page 20) Updated 12.4.8 Power-On Reset Timing. Changed parameter from “Power Supply rise time(t_{VCCR})[ms]” to “Power ramp rate(dV/dt)[mV/us]” and add some comments. (Page 113) Modified CSIO timing typo (12.4.12 CSIO(SPI) Timing) Deleted “SPI=1, MS=0” in the titles and added MS=0,1 in the schematic (Page 134-141, 150-157) Modified RTC description(Features, Real-Time Clock(RTC)) Deleted “second , or day of the week” in the Interrupt function.(Page 3) Modifications related to the VBAT in the following chapter. “7. Handling Devices” Notes on Power-on (Page 76) “11. Pin Status in Each CPU State” List of VBAT Domain Pin Status (Page 90) “12.3.1 Current Rating” Table12-9. Typical and Maximum Current Consumption in Deep Standby STOP Mode, Deep Standby RTC Mode and VBAT (Page 105) Deleted MPNs below from “13. Ordering Information” (Page 190) S6E2C38H0AGV20000, S6E2C38J0AGB10000, S6E2C38J0AGV20000, S6E2C38L0AGL20000, S6E2C39H0AGV20000, S6E2C39J0AGB10000, S6E2C39J0AGV20000, S6E2C39L0AGL20000, S6E2C3AH0AGV20000, S6E2C3AJ0AGB10000, S6E2C3AJ0AGV20000, S6E2C3AL0AGL20000 Added MPNs below to “13. Ordering Information” (Page 190) S6E2C38H0AGV2000A, S6E2C38J0AGB1000A, S6E2C38J0AGV2000A, S6E2C38L0AGL2000A, S6E2C39H0AGV2000A, S6E2C39J0AGB1000A, S6E2C39J0AGV2000A, S6E2C39L0AGL2000A, S6E2C3AH0AGV2000A, S6E2C3AJ0AGB1000A, S6E2C3AJ0AGV2000A, S6E2C3AL0AGL2000A Deleted Baud rate spec for High-Speed Synchronous Serial in “12.4.12 CSIO(SPI) Timing”(Page 142-148) Modified the expression of the “Built-in CR” and add Note in the “1. Product Lineup”(Page 8) Modified typo(SCLKx_0 -> SCKx_0)(Page 126, 128, 130, 132) Change the name from “USB Function” to “USB Device” (Page 1, 8, 58) Added Maximum Access size in “Features”(Page 1) Updated IO circuit (type A) (Page 62)

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