NOTE

The parameters specified in this MCU document supersede any values found in the module specifications.

5.1 Maximum Ratings

Table 7. Absolute Maximum Ratings [1, 2]

Characteristic	Symbol	Value	Unit
Core Supply Voltage	IV_{DD}	0.5 to +2.0	V
CMOS Pad Supply Voltage	EV_{DD}	0.3 to +4.0	V
DDR/Memory Pad Supply Voltage	SDV_{DD}	0.3 to +4.0	V
Oscillator Supply Voltage	$OSCV_{DD}$	0.3 to +4.0	V
PLL Supply Voltage	$PLLV_{DD}$	0.3 to +2.0	V
RTC Supply Voltage	$RTCV_{DD}$	0.5 to +2.0	V
Digital Input Voltage [3]	V_{IN}	0.3 to +3.6	V
Instantaneous Maximum Current Single pin limit (applies to all pins) [3, 4, 5]	I_D	25	mA
Operating Temperature Range (Packaged)	T_A (T_L T_H)	40 to +85	qC
Storage Temperature Range	T_{stg}	55 to +150	qC

1 Functional operating conditions are given in Section 5.4, DC Electrical Specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Continued operation at these levels may affect device reliability or cause permanent damage to the device.

2 This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or EV_{DD}).

3 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

4 All functional non-supply pins are internally clamped to V_{SS} and EV_{DD}.

5 Power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > EV_{DD}$) is greater than I_{DD}, the injection current may flow out of EV_{DD} and could result in external power supply going out of regulation. Insure external EV_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power (ex; no clock). Power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions.

4.3 Pinout—196 MAPBGA

The pinout for the MCF52277 package is shown below.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	LCD_D6	LCD_D5	LCD_D4	LCD_D2	LCD_ LSCLK	T0IN	U1TXD	U1RXD	USB_DM	USB_DP	FB_CS2	FB_A21	FB_A17	FB_A16	A
B	LCD_D8	LCD_D7	LCD_D3	LCD_D1	LCD_ ACD/OE	T1IN	IRQ_1	U1RTS	DSPI_ PCS0	VDD_ USB	FB_CS3	FB_A20	FB_A18	FB_A15	B
C	LCD_D13	LCD_D12	LCD_D10	LCD_D0	I2C_SCL	T2IN	IRQ_4	U1CTS	DSPI_ SCK	FB_CS0	FB_A23	FB_A19	FB_A14	FB_A13	C
D	LCD_D15	LCD_D14	LCD_D11	LCD_D9	I2C_SDA	T3IN	IRQ_7	DSPI_SIN	DSPI_ SOUT	FB_CS1	FB_A22	FB_A12	FB_A11	FB_A10	D
E	LCD_LP/ HSYNC	LCD_FLM/ VSYNC	LCD_D17	LCD_D16	IVDD	EVDD	EVDD	SDVDD	SDVDD	TEST	FB_A9	FB_A8	FB_A7	FB_A6	E
F	SD_CS0	SD_CKE	SD_WE	FB_TS	EVDD	EVDD	VSS	VSS	SDVDD	IVDD	FB_A5	FB_A4	FB_A3	EXTAL	F
G	FB_D15	FB_D14	FB_D13	FB_D12	EVDD	VSS	VSS	VSS	SDVDD	BOOT MOD1	FB_A2	FB_A1	VDD_ OSC	XTAL	G
H	FB_D11	FB_D10	FB_D9	FB_D8	SDVDD	VSS	VSS	VSS	EVDD	BOOT MOD0	FB_A0	FB_TA	VSS_ OSC	VDD_ PLL	H
J	FB_BE/ BWE1	SD_DQS3	FB_BE/ BWE3	FB_D31	SDVDD	SDVDD	VSS	VSS	EVDD	IVDD	RESET	U0RTS	VDD_ RTC	RTC_ EXTAL	J
K	FB_D30	FB_D29	FB_D28	FB_D27	IVDD	SDVDD	SDVDD	EVDD	EVDD	JTAG_EN	RSTOUT	U0CTS	U0RXD	RTC_ XTAL	K
L	FB_D26	FB_D25	FB_D24	SD_A10	FB_D17	FB_BE/ BWE0	FB_D4	FB_D0	PST3	DDATA3	TDO	U0TXD	VDD_ ADC	VSS_ ADC	L
M	SD_CLK	SD_ SDR_DQS	FB_D23	FB_D20	FB_D16	FB_D7	FB_D3	FB_R/W	PST2	DDATA2	TDI	ADC_ REF	ADC_IN1	ADC_IN0	M
N	SD_CLK	SD_CAS	FB_D22	FB_D19	FB_BE/ BWE2	FB_D6	FB_D2	FB_OE	PST1	DDATA1	TMS	ADC_IN6	ADC_IN4	ADC_IN2	N
P	FB_CLK	SD_RAS	FB_D21	FB_D18	SD_ DQS0	FB_D5	FB_D1	TCLK	PST0	DDATA0	TRST	ADC_IN7	ADC_IN5	ADC_IN3	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 8. MCF52277 Pinout (196 MAPBGA)

5 Electrical Characteristics

This document contains electrical specification tables and reference timing diagrams for the MCF5227x microprocessor. This section contains detailed information on DC/AC electrical characteristics and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle, however for production silicon these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

9 If JTAG_EN is asserted, these pins default to alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.

4.2 Pinout—176 LQFP

The pinout for the MCF52274 package is shown below.

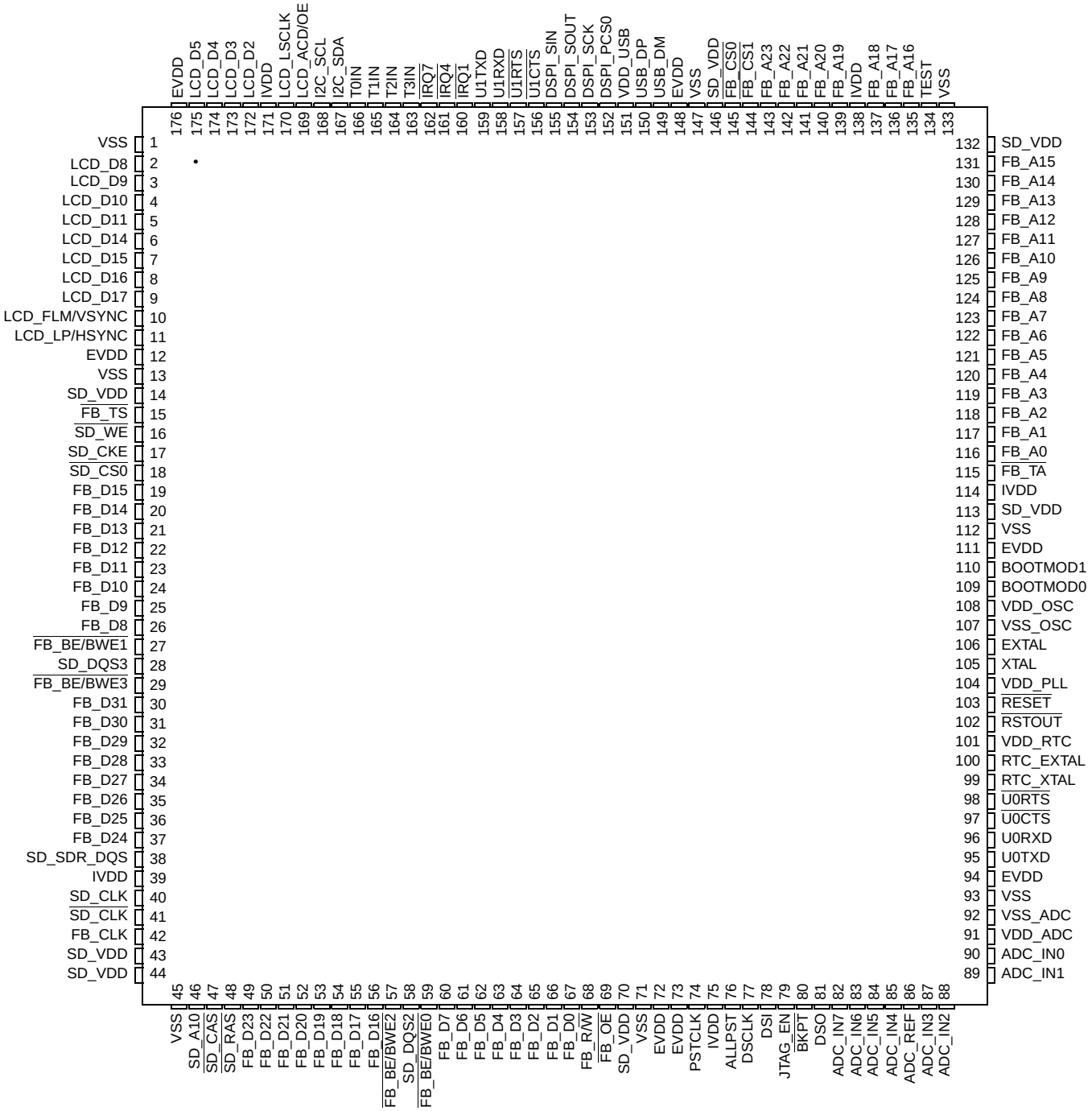

Figure 7. MCF52274 Pinout (176 LQFP)

Table 6. MCF5227*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF52274 176 LQFP	MCF52277 196 MAPBGA
ALLPST	—	—	—	—	O	EVDD	76	—
JTAG_EN	—	—	—	D	I	EVDD	79	K10
PSTCLK	—	TCLK	—	U	O	EVDD	74	P8
DSI	—	TDI	—	U	I	EVDD	78	M11
DSO	—	TDO	—	—	O	EVDD	81	L11
$\overline{\text{BKPT}}$	—	TMS	—	U	I	EVDD	80	N11
DSCLK	—	$\overline{\text{TRST}}$	—	U	I	EVDD	77	P11
Test								
TEST	—	—	—	D	I	EVDD	134	E10
Power Supplies								
IVDD	—	—	—	—	—	—	39, 75, 114, 138, 171	K5, F10, E5, J10
EVDD	—	—	—	—	—	—	12, 72, 73, 94, 111, 148, 176	E6, E7, F5, F6, G5, H9, J9, K8, K9
SD_VDD	—	—	—	—	—	—	14, 43, 44, 70, 113, 132, 146	E8, E9, F9, G9, H5, J5, J6, K6, K7
VDD_OSC	—	—	—	—	—	—	108	G13
VDD_PLL	—	—	—	—	—	—	104	H14
VDD_USB	—	—	—	—	—	—	151	B10
VDD_RTC	—	—	—	—	—	—	101	J13
VDD_ADC	—	—	—	—	—	—	91	L13
VSS	—	—	—	—	—	—	1, 13, 45, 71, 93, 112, 133, 147	F7, F8, G6–G8, H6–H8, J7, J8
VSS_OSC	—	—	—	—	—	—	107	H13
VSS_ADC	—	—	—	—	—	—	92	L14

1 Pull-ups are generally only enabled on pins with their primary function, except as noted.

2 Refers to pin's primary function.

3 Enabled only in oscillator bypass mode (internal crystal oscillator is disabled).

4 GPIO functionality is determined by the edge port module. The GPIO module is only responsible for assigning the alternate functions.

5 Pull-up when $\overline{\text{DREQ}}$ controls the pin.

6 The 176 LQFP device only supports a 12-bit LCD data bus.

7 DSPI or SBF signal functionality is controlled by $\overline{\text{RESET}}$. When asserted, these pins are configured for serial boot; when negated, the pins are configured for DSPI.

8 Pull-up when the serial boot facility (SBF) controls the pin.

Table 6. MCF5227*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF52274 176 LQFP	MCF52277 196 MAPBGA
Touchscreen Controller								
ADC_IN[7:0]	—	—	—	—	I	VDD_ADC	82–85, 87–90	P12, N12, P13, N13, P14, N14, M13, M14
ADC_REF	—	—	—	—	I	VDD_ADC	86	M12
I^2C								
I2C_SCL	PI2C1	CANTX	U2TXD	U	I/O	EVDD	168	C5
I2C_SDA	PI2C0	CANRX	U2RXD	U	I/O	EVDD	167	D5
DSPI[7]								
DSPI_PCS0/$\overline{SS}$	PDSPI3	$\overline{U2RTS}$	—	U	I/O	EVDD	152	B9
DSPI_SIN	PDSPI2	U2RXD	SBF_DI	[8]	I	EVDD	155	D8
DSPI_SOUT	PDSPI1	U2TXD	SBF_D0	—	O	EVDD	154	D9
DSPI_SCK	PDSPI0	$\overline{U2CTS}$	SBF_CK	—	I/O	EVDD	153	C9
UARTs								
$\overline{U1CTS}$	PUART7	SSI_BCLK	LCD_CLS	—	I	EVDD	156	C8
$\overline{U1RTS}$	PUART6	SSI_FS	LCD_PS	—	O	EVDD	157	B8
U1TXD	PUART5	SSI_TXD	—	—	O	EVDD	159	A7
U1RXD	PUART4	SSI_RXD	—	—	I	EVDD	158	A8
$\overline{U0CTS}$	PUART3	DT1OUT	USB_VBUS_EN	—	I	EVDD	97	K12
$\overline{U0RTS}$	PUART2	DT1IN	USB_VBUS_OC	—	O	EVDD	98	J12
U0TXD	PUART1	CANTX	—	—	O	EVDD	95	L12
U0RXD	PUART0	CANRX	—	—	I	EVDD	96	K13
DMA Timers								
DT3IN	PTIMER3	DT3OUT	SSI_MCLK	—	I	EVDD	163	D6
DT2IN/$\overline{SBF\_CS}$[7]	PTIMER2	DT2OUT	DSPI_PCS2	—	I	EVDD	164	C6
DT1IN	PTIMER1	DT1OUT	LCD_CONTRAST	—	I	EVDD	165	B6
DT0IN	PTIMER0	DT0OUT	LCD_REV	—	I	EVDD	166	A6
BDM/JTAG[9]								
PST[3:0]	—	—	—	—	O	EVDD	—	L9, M9, N9, P9
DDATA[3:0]	—	—	—	—	O	EVDD	—	L10, M10, N10, P10

Table 6. MCF5227*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF52274 176 LQFP	MCF52277 196 MAPBGA
SD_SDR_DQS	—	—	—	—	O	SDVDD	38	M2
$\overline{\text{SD\_WE}}$	—	—	—	—	O	SDVDD	16	F3
External Interrupts Port[4]								
$\overline{\text{IRQ7}}$	PIRQ7	—	—	—	I	EVDD	162	D7
$\overline{\text{IRQ4}}$	PIRQ4	$\overline{\text{DREQ0}}$	DSPI_PCS4	[5]	I	EVDD	161	C7
$\overline{\text{IRQ1}}$	PIRQ1	USB_CLKIN	SSI_CLKIN	—	I	EVDD	160	B7
LCD Controller[6]								
LCD_D[17:16][6]	PLCDDH[1:0]	LCD_D[11:10]	—	—	O	EVDD	9, 8	E3, E4
LCD_D[15:14][6]	PLCDDM[7:6]	LCD_D[9:8]	—	—	O	EVDD	7, 6	D1, D2
LCD_D13	PLCDDM5	CANTX	—	—	O	EVDD	—	C1
LCD_D12	PLCDDM4	CANRX	—	—	O	EVDD	—	C2
LCD_D[11:8][6]	PLCDDM[3:0]	LCD_D[7:4]	—	—	O	EVDD	5–2	D3, C3, D4, B1
LCD_D7	PLCDDL7	PWM7	—	—	O	EVDD	—	B2
LCD_D6	PLCDDL6	PWM5	—	—	O	EVDD	—	A1
LCD_D[5:2][6]	PLCDDL[5:2]	LCD_D[3:0]	—	—	O	EVDD	175–172	A2, A3, B3, A4
LCD_D1	PLCDDL1	PWM3	—	—	O	EVDD	—	B4
LCD_D0	PLCDDL0	PWM1	—	—	O	EVDD	—	C4
LCD_ACD/ LCD_OE	PLCDCTL3	LCD_SPL_SPR	—	—	O	EVDD	169	B5
LCD_FLM/ LCD_VSYNC	PLCDCTL2	—	—	—	O	EVDD	10	E2
LCD_LP/ LCD_HSYNC	PLCDCTL1	—	—	—	O	EVDD	11	E1
LCD_LSCLK	PLCDCTL0	—	—	—	O	EVDD	170	A5
USB On-the-Go								
USB_DM	—	—	—	—	O	USB VDD	149	A9
USB_DP	—	—	—	—	O	USB VDD	150	A10
Real Time Clock								
RTC_EXTAL	—	—	—	—	I	EVDD	100	J14
RTC_XTAL	—	—	—	—	O	EVDD	99	K14