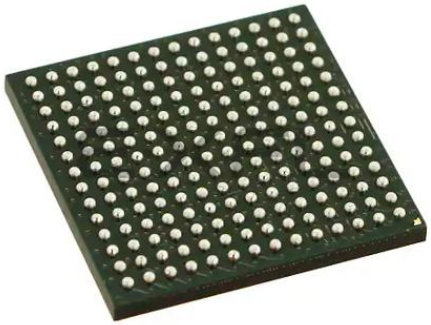

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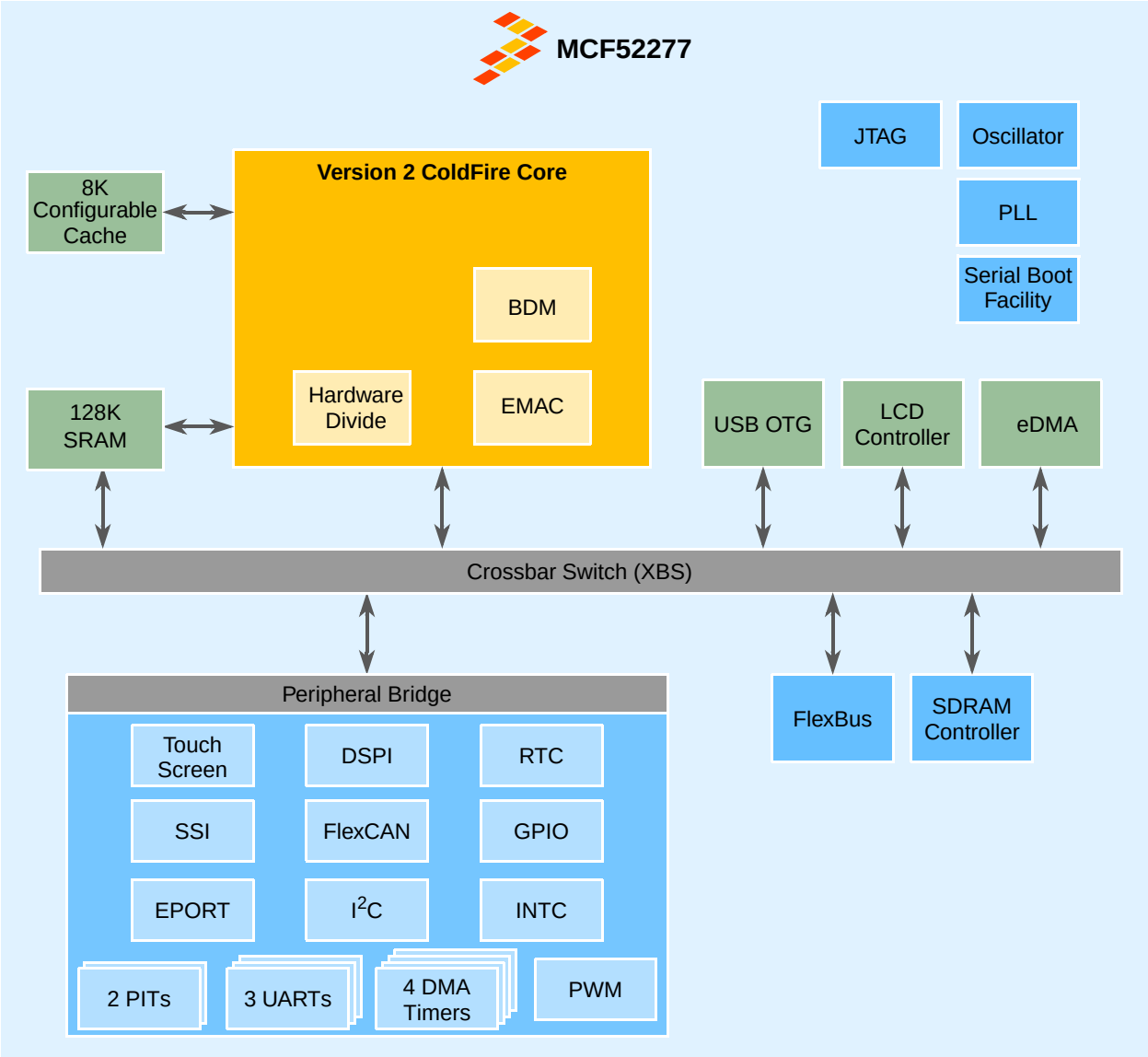
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	166.67MHz
Connectivity	CANbus, EBI/EMI, I²C, SPI, SSI, UART/USART, USB OTG
Peripherals	DMA, LCD, PWM, WDT
Number of I/O	55
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.4V ~ 1.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	196-LBGA
Supplier Device Package	196-MAPBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf52277cvm160



LEGEND

BDM	– Background debug module	**LCD**	– Liquid-crystal display
DSPI	– DMA serial peripheral interface	**PIT**	– Programmable interrupt timer
eDMA	– Enhanced direct memory access	**PLL**	– Phase-locked loop module
EMAC	– Enchanced multiply-accumulate unit	**PWM**	– Pulse-width modulator
EPORT	– Edge port module	**RTC**	– Real time clock
GPIO	– General purpose input/output module	**SSI**	– Synchronous serial interface
I^2C	– Inter-intergrated circuit	**UART**	– Universal asynchronous receiver/transmitter
INTC	– Interrupt controller	**USB OTG**	– Universal Serial Bus On-the-Go controller
JTAG	– Joint Test Action Group interface		

Figure 1. MCF52277 Block Diagram

1 MCF5227x Family Comparison

The following table compares the various device derivatives available within the MCF5227*x* family.

Table 1. MCF5227*x* Family Configurations

Module	MCF52274	MCF52277
ColdFire Version 2 Core with EMAC (Enhanced Multiply-Accumulate Unit)	•	•
Core (System) Clock	up to 120 MHz	up to 166.67 MHz
Peripheral and External Bus Clock (Core clock ÷ 2)	up to 60 MHz	up to 83.33 MHz
Performance (Dhrystone/2.1 MIPS)	up to 114	up to 159
Static RAM (SRAM)	128 Kbytes	
Configurable Cache	8 Kbytes	
ASP Touchscreen Controller	•	•
LCD Controller	12-bit color	18-bit color
USB 2.0 On-the-Go	•	•
FlexBus External Interface	•	•
SDR/DDR SDRAM Controller	•	•
FlexCAN 2.0B communication module	•	•
Real Time Clock	•	•
Watchdog Timer	•	•
16-channel Direct Memory Access (DMA)	•	•
Interrupt Controllers (INTC)	1	1
Synchronous Serial Interface (SSI)	•	•
I^2C	•	•
DSPI	•	•
UARTs	3	3
32-bit DMA Timers	4	4
Periodic Interrupt Timers (PIT)	2	2
PWM Module	•	•
Edge Port Module (EPORT)	•	•
General Purpose I/O Module (GPIO)	•	•
JTAG - IEEE® 1149.1 Test Access Port	•	•
Package	176 LQFP	196 MAPBGA

3.3 ADC Power Filtering

To minimize noise, an external filters is required for the $ADCV_{DD}$ power pin. The filter shown in Figure 4 should be connected between the board EV_{DD} and the $ADCV_{DD}$ pin. The resistor and capacitors should be placed as close to the dedicated $ADCV_{DD}$ pin as possible.

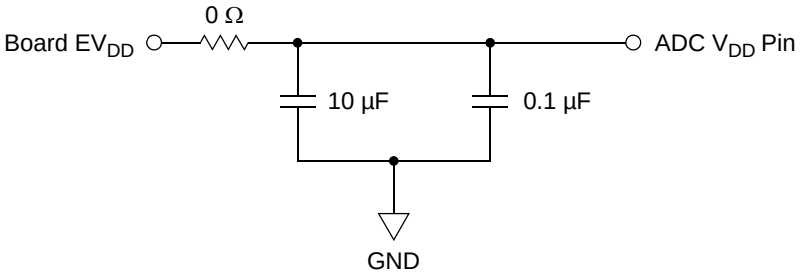


Figure 4. ADC V_{DD} Power Filter

3.4 Supply Voltage Sequencing

The relationship between SDV_{DD} and EV_{DD} is non-critical during power-up and power-down sequences. Both SDV_{DD} (2.5V or 3.3V) and EV_{DD} are specified relative to IV_{DD}.

3.4.1 Power Up Sequence

If EV_{DD}/SDV_{DD} are powered up with IV_{DD} at 0 V, then the sense circuits in the I/O pads will cause all pad output drivers connected to the EV_{DD}/SDV_{DD} to be in a high impedance state. There is no limit on how long after EV_{DD}/SDV_{DD} powers up before IV_{DD} must powered up. IV_{DD} should not lead the EV_{DD}, SDV_{DD} or $PLLV_{DD}$ by more than 0.4 V during power ramp-up, or there will be high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 500 us to avoid turning on the internal ESD protection clamp diodes.

3.4.2 Power Down Sequence

If $IV_{DD}/PLLV_{DD}$ are powered down first, then sense circuits in the I/O pads will cause all output drivers to be in a high impedance state. There is no limit on how long after IV_{DD} and $PLLV_{DD}$ power down before EV_{DD} or SDV_{DD} must power down. IV_{DD} should not lag EV_{DD}, SDV_{DD}, or $PLLV_{DD}$ going low by more than 0.4 V during power down or there will be undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop $IV_{DD}/PLLV_{DD}$ to 0 V.
2. Drop EV_{DD}/SDV_{DD} supplies.

3.5 Power Consumption Specifications

All application power consumption data is lab data measured on an M52277EVB running the Freescale Linux BSP.

Table 3. MCF52277 Application Power Consumption[1]

Core Freq.		Idle (LCD image)	Idle (audio image)	Button Demo	Slideshow Demo	MP3 Playback	USB FS File Copy	Units
160 MHz	IV_{DD}	61.4	59.2	84.7	96.5	89.2	89.5	mA
	EV_{DD}	28.87	25.73	35.3	34.6	33.46	29.86	
	SDV_{DD}	18.8	18.57	21.8	23.9	22.66	22.2	
	Total Power	**221.211**	**207.135**	**282.78**	**301.95**	**285.006**	**272.748**	**mW**

1 All voltage rails at nominal values: IV_{DD} = 1.5 V, EV_{DD} = 3.3 V, and SDV_{DD} = 1.8 V.

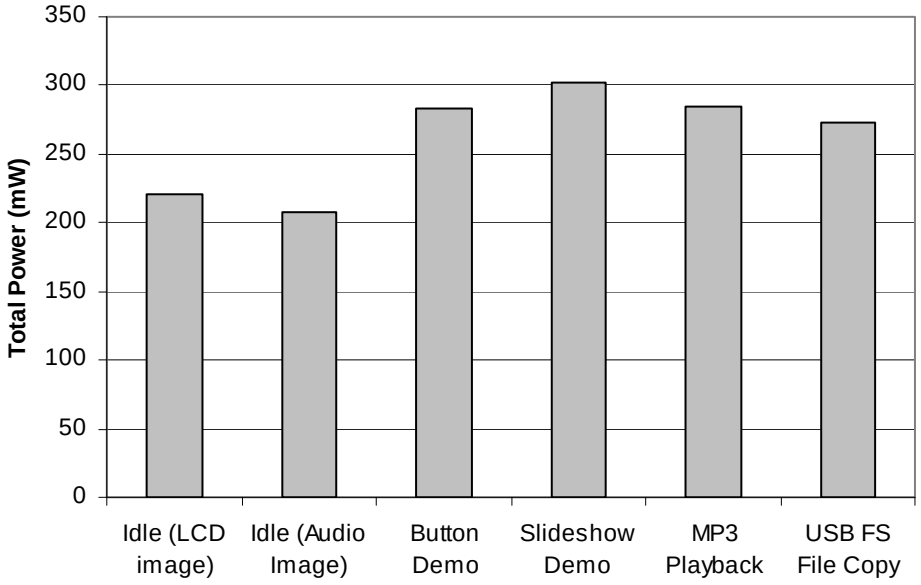


Figure 5. Power Consumption in Various Applications

All current consumption data is lab data measured on a single device using an evaluation board. Table 4 shows the typical power consumption in low-power modes. These current measurements are taken after executing a STOP instruction.

Table 4. Current Consumption in Low-Power Modes[1,2]

Mode	Voltage Supply	System Frequency				
		80MHz	64MHz	48MHz	32MHz	4MHz (LIMP mode)
RUN	IV_{DD} (mA)	75.1	62.7	49.2	36.6	3.5
	Power (mW)	112.65	94.05	73.80	54.90	5.25
WAIT	IV_{DD} (mA)	61.9	52.8	42.0	31.7	2.9
	Power (mW)	92.85	79.20	63.00	47.55	4.35

4 Pin Assignments and Reset States

4.1 Signal Multiplexing

The following table lists all the MCF5227*x* pins grouped by function. The direction column is the direction for the primary function of the pin only. Refer to Section 4, "Pin Assignments and Reset States," for package diagrams. For a more detailed discussion of the MCF5227*x* signals, consult the *MCF52277 Reference Manual* (MCF52277RM).

NOTE

In this table and throughout this document a single signal within a group is designated without square brackets (i.e., FB_A23), while designations for multiple signals within a group use brackets (i.e., FB_A[23:21]) and is meant to include all signals within the two bracketed numbers when these numbers are separated by a colon.

NOTE

The primary functionality of a pin is not necessarily its default functionality. Most pins that are muxed with GPIO will default to their GPIO functionality. See Table 5 for a list of the exceptions.

Table 5. Special-Case Default Signal Functionality

Pin	Default Signal
$\overline{\text{FB\_BE/BWE}}$[3:0]	$\overline{\text{FB\_BE/BWE}}$[3:0]
$\overline{\text{FB\_CS}}$[3:0]	$\overline{\text{FB\_CS}}$[3:0]
$\overline{\text{FB\_OE}}$	$\overline{\text{FB\_OE}}$
$\overline{\text{FB\_TA}}$	$\overline{\text{FB\_TA}}$
FB_R/$\overline{\text{W}}$	FB_R/$\overline{\text{W}}$
$\overline{\text{FB\_TS}}$	$\overline{\text{FB\_TS}}$

Table 6. MCF5227*x* Signal Information and Muxing

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF52274 176 LQFP	MCF52277 196 MAPBGA
Reset								
RESET	—	—	—	U	I	EVDD	103	J11
$\overline{\text{RSTOUT}}$	—	—	—	—	O	EVDD	102	K11
Clock								
EXTAL	—	—	—	—	I	EVDD	106	F14
XTAL	—	—	—	U[3]	O	EVDD	105	G14
Mode Selection								
BOOTMOD[1:0]	—	—	—	—	I	EVDD	110, 109	G10, H10

5.2 Thermal Characteristics

Table 8. Thermal Characteristics

Characteristic		Symbol	196 MAPBGA	176 LQFP	Unit
Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	38[1,2]	48[1,2]	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	34[1,2]	42[1,2]	°C/W
Junction to board		θ_{JB}	27[3]	37[3]	°C/W
Junction to case		θ_{JC}	17[4]	14[4]	°C/W
Junction to top of package		Ψ_{jt}	4[1,5]	3[1,5]	°C/W
Maximum operating junction temperature		T_j	105	105	°C

1 θ_{JA}, θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JmA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

2 Per JEDEC JESD51-6 with the board horizontal.

3 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

4 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

5 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad \textbf{Eqn. 1}$$

Where:

T_A = Ambient Temperature, °C
Q_{JMA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
P_D = $P_{INT} + P_{I/O}$
P_{INT} = $I_{DD} \times IV_{DD}$, Watts - Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = \frac{K}{(T_J + 273\,°C)} \quad \textbf{Eqn. 2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A \times 273°C) + Q_{JMA} \times P_D^2 \quad \textbf{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

5.3 ESD Protection

Table 9. ESD Protection Characteristics[1,2]

Characteristic	Symbol	Value	Unit
ESD Target for Human Body Model	HBM	2000	V

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

5.4 DC Electrical Specifications

Table 10. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Core Supply Voltage	IV_{DD}	1.4	1.6	V
PLL Supply Voltage	$PLLV_{DD}$	1.4	1.6	V
RTC Supply Voltage	$RTCV_{DD}$	1.4	1.6	V
CMOS Pad Supply Voltage	EV_{DD}	3.0	3.6	V
SDRAM and FlexBus Supply Voltage Mobile DDR/Bus Pad Supply Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{DD}	 1.7 2.25 3.0	 1.95 2.75 3.6	V
USB Supply Voltage	$USBV_{DD}$	3.0	3.6	V
Oscillator Supply Voltage	$OSCV_{DD}$	3.0	3.6	V
CMOS Input High Voltage	EV_{IH}	2	EV_{DD} + 0.3	V
CMOS Input Low Voltage	EV_{IL}	V_{SS} – 0.3	0.8	V
CMOS Output High Voltage I_{OH} = –5.0 mA	EV_{OH}	EV_{DD} – 0.4	—	V
CMOS Output Low Voltage I_{OL} = 5.0 mA	EV_{OL}	—	0.4	V
SDRAM and FlexBus Input High Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{IH}	 1.35 1.7 2	 SDV_{DD} + 0.3 SDV_{DD} + 0.3 SDV_{DD} + 0.3	V
SDRAM and FlexBus Input Low Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{IL}	 V_{SS} – 0.3 V_{SS} – 0.3 V_{SS} – 0.3	 0.45 0.8 0.8	V

Table 12. ASP Electrical Characteristics (continued)

Characteristic	Symbol	Min	Typical	Max	Unit
Conversion Time	t_{ADC}	15	—	32	t_{AIC} cycles
Sample Time	t_{ADS}	3	—	20	t_{AIC} cycles
Multiplexer Settling Time	t_{AMS}	—	—	3	t_{AIC} cycles
Zero-scale Error	ZE	—	±4	±12	lsb[1]
Full-scale Error	FE	—	±320	±370	lsb[1]
Input Capacitance	C_{AIN}	—	—	34	pF

1 A least significant bit (lsb) is a unit of voltage equal to the smallest resolution of the ADC. This unit of measure approximately relates the error voltage to the observed error in conversion (code error), and is useful for systemic errors such as differential non-linearity. A 2.56-V input on an ADC with ± 3 lsb of error could read between 0x1FD and 0x203. This unit is by far the most common terminology and will be the preferred unit used for error representation.
A bit is a unit equal to the log (base2) of the error voltage normalized to the resolution of the ADC. An error of N bits corresponds to 2^N lsb of error. This measure is easily confused with lsb and is hard to extrapolate between integer values.

5.7 External Interface Timing Specifications

5.7.1 FlexBus

A multi-function external bus interface called FlexBus is provided with basic functionality to interface to slave-only devices up to a maximum bus frequency of 66MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices a simple chip-select based interface can be used.

All processor bus timings are synchronous; that is, input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data will be latched or driven onto the external bus, relative to the Flexbus output clock, FB_CLK. All other timing relationships can be derived from these values.

Table 13. FlexBus AC Timing Specifications

Num	Characteristic	Symbol	Min	Max	Unit	Notes
	Frequency of Operation		—	83.33	MHz	$f_{sys/2}$
FB1	Clock Period (FB_CLK)	t_{FBCK}	12.0	—	ns	t_{cyc}
FB2	Address, Data, and Control Output Valid (FB_A[23:0], FB_D[31:0], FB_CS[5:0], FB_R/W, FB_TS, FB_BE/BWE[3:0] and FB_OE)	$t_{FBCHDCV}$	—	7.0	ns	1
FB3	Address, Data, and Control Output Hold (FB_A[23:0], FB_D[31:0], FB_CS[5:0], FB_R/W, FB_TS, FB_BE/BWE[3:0], and FB_OE)	$t_{FBCHDCI}$	1	—	ns	1, 2

Table 14. SDR Timing Specifications (continued)

Num	Characteristic	Symbol	Min	Max	Unit	Notes
SD8	SD_DQS[3:2] input hold relative to SD_CLK	$t_{DQISDCH}$	Does not apply. 0.5×SD_CLK fixed width.			6
SD9	Data (D[31:0]) Input Setup relative to SD_CLK (reference only)	t_{DVSDCH}	0.25 × SD_CLK	—	ns	7
SD10	Data Input Hold relative to SD_CLK (reference only)	t_{DISDCH}	1.0	—	ns	
SD11	Data (D[31:0]) and Data Mask(SD_DQM[3:0]) Output Valid	$t_{SDCHDMV}$	—	0.5 × SD_CLK + 2	ns	
SD12	Data (D[31:0]) and Data Mask (SD_DQM[3:0]) Output Hold	$t_{SDCHDMI}$	1.5	—	ns	

1 The device supports same frequency of operation for both FlexBus and SDRAM clock operates as that of the internal bus clock. Please see the PLL chapter of the device reference manual for more information on setting the SDRAM clock rate.

2 SD_CLK is one SDRAM clock in ns.

3 Pulse width high plus pulse width low cannot exceed min and max clock period.

4 SD_SDR_DQS is designed to pulse 0.25 clock before the rising edge of the memory clock. This is a guideline only. Subtle variation from this guideline is expected. SD_SDR_DQS will only pulse during a read cycle and one pulse will occur for each data beat.

5 SD_DQS is designed to pulse 0.25 clock before the rising edge of the memory clock. This spec is a guideline only. Subtle variation from this guideline is expected. SD_DQS will only pulse during a read cycle and one pulse will occur for each data beat.

6 The SD_DQS pulse is designed to be 0.5 clock in width. The timing of the rising edge is most important. The falling edge does not affect the memory controller.

7 Since a read cycle in SDR mode still uses the DQS circuit within the device, it is critical that the data valid window be centered 1/4 clk after the rising edge of DQS. Ensuring that this happens will result in successful SDR reads. The input setup spec is provided as guidance.

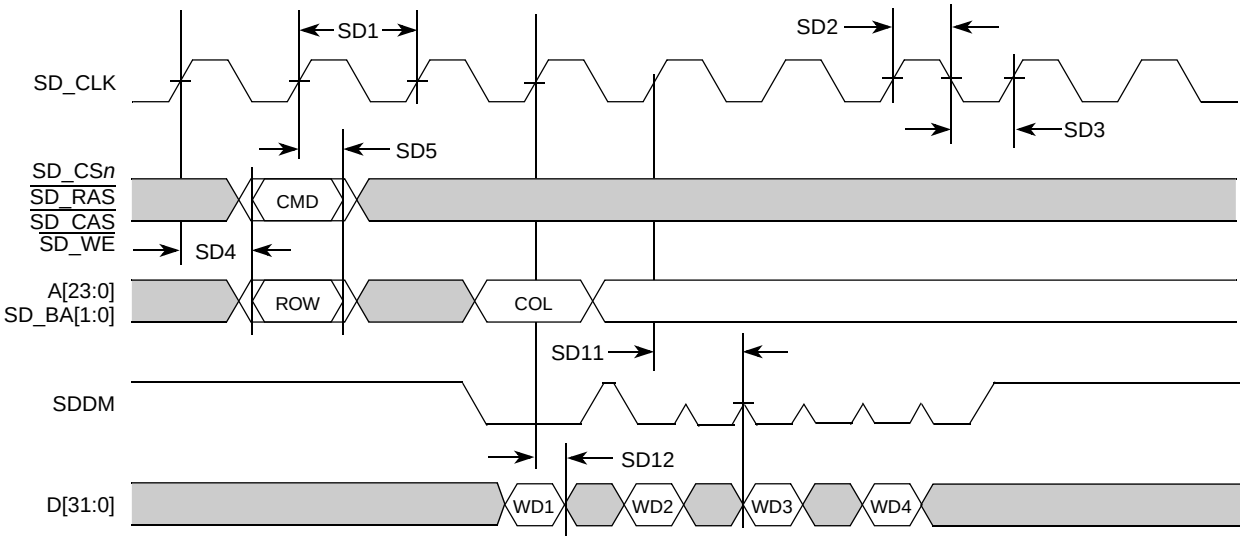


Figure 11. SDR Write Timing

Table 15. DDR Timing Specifications (continued)

Num	Characteristic	Symbol	Min	Max	Unit	Notes
DD8	Data and Data Mask Output Hold (DQS→DQ) Relative to DQS (DDR Write Mode)	t_{DQDMI}	1.0	—	ns	7
DD9	Input Data Skew Relative to DQS (Input Setup)	t_{DVDQ}	—	1	ns	8
DD10	Input Data Hold Relative to DQS	t_{DIDQ}	0.25 × SD_CLK + 0.5ns	—	ns	9
DD11	DQS falling edge from SDCLK rising (output hold time)	$t_{DQLSDCH}$	0.5	—	ns	

1 The frequency of operation is either 2x or 4x the FB_CLK frequency of operation. FlexBus and SDRAM clock operate at the same frequency as the internal bus clock.

2 SD_CLK is one SDRAM clock in ns.

3 Pulse-width high plus pulse-width low cannot exceed minimum or maximum clock period.

4 Command output valid should be one-half the memory bus clock (SD_CLK) plus some minor adjustments for process, temperature, and voltage variations.

5 This specification relates to the required input setup time of today's DDR memories. The device's output setup should be larger than the input setup of the DDR memories. If it is not larger, then the input setup on the memory will be in violation. MEM_DATA[31:24] is relative to MEM_DQS[3], MEM_DATA[23:16] is relative to MEM_DQS[2], MEM_DATA[15:8] is relative to MEM_DQS[1], and MEM_DATA[7:0] is relative MEM_DQS[0].

6 The first data beat will be valid before the first rising edge of DQS and after the DQS write preamble. The remaining data beats will be valid for each subsequent DQS edge.

7 This specification relates to the required hold time of today's DDR memories. MEM_DATA[31:24] is relative to MEM_DQS[3], MEM_DATA[23:16] is relative to MEM_DQS[2], MEM_DATA[15:8] is relative to MEM_DQS[1], and MEM_DATA[7:0] is relative MEM_DQS[0].

8 Data input skew is derived from each DQS clock edge. It begins with a DQS transition and ends when the last data line becomes valid. This input skew must include DDR memory output skew and system-level board skew (due to routing or other factors).

9 Data input hold is derived from each DQS clock edge. It begins with a DQS transition and ends when the first data line becomes invalid.

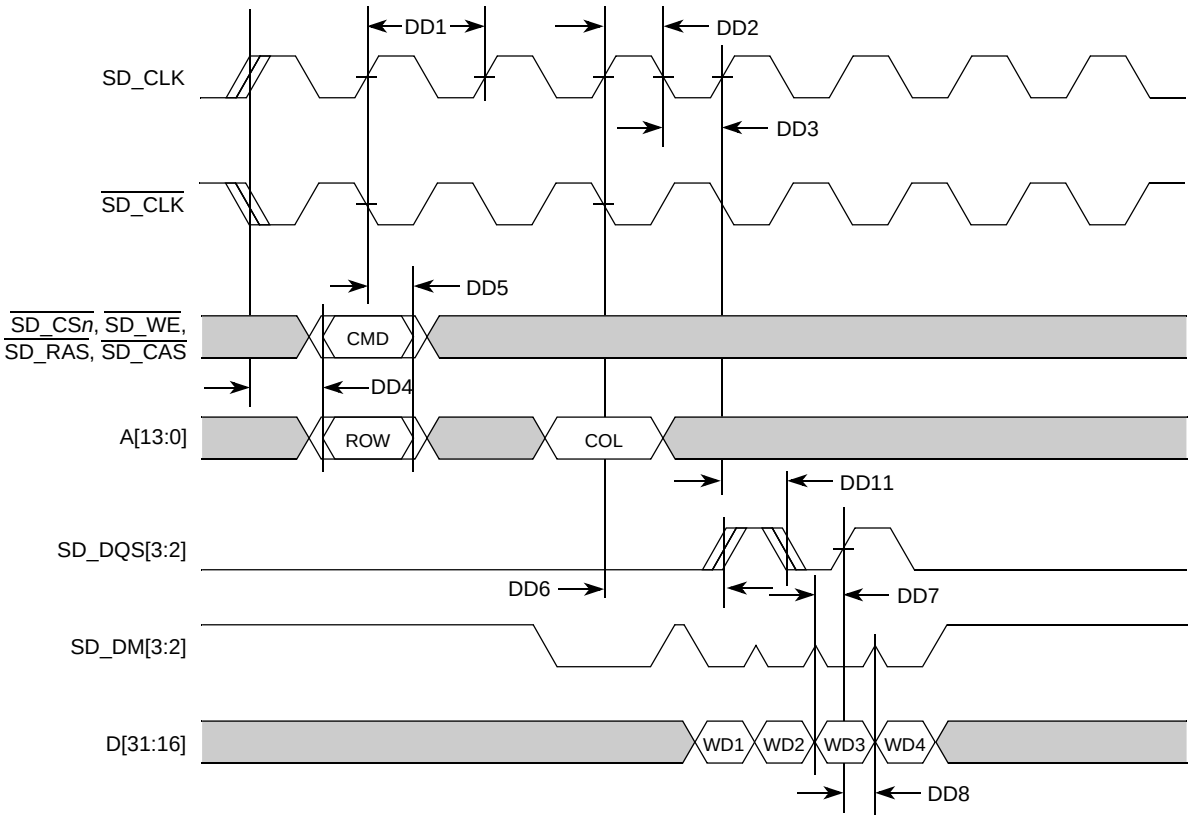


Figure 13. DDR Write Timing

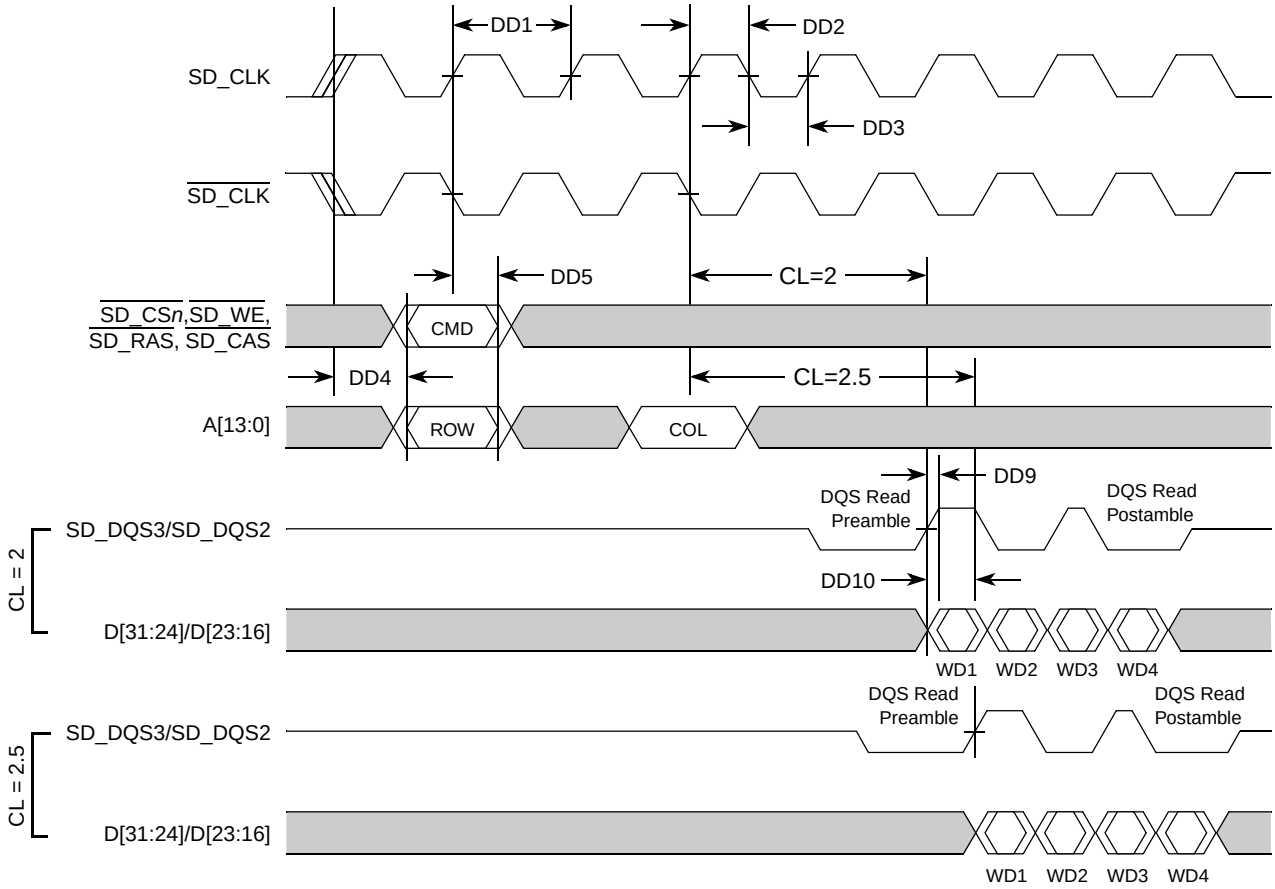


Figure 14. DDR Read Timing

Table 16. DDR Clock Crossover Specifications

Symbol	Characteristic	Min	Max	Unit
V_{MP}	Clock output mid-point voltage	1.05	1.45	V
V_{OUT}	Clock output voltage level	–0.3	SD_VDD + 0.3	V
V_{ID}	Clock output differential voltage (peak to peak swing)	0.7	SD_VDD + 0.6	V
V_{IX}	Clock crossing point voltage[1]	1.05	1.45	V

1 The clock crossover voltage is only guaranteed when using the highest drive strength option for the SDCLK[1:0] and $\overline{\text{SDCLK}}$[1:0] signals.

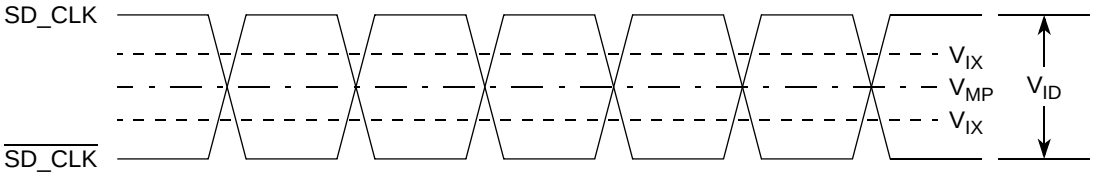


Figure 15. SD_CLK and $\overline{\text{SD\_CLK}}$ Crossover Timing

5.8 General Purpose I/O Timing

Table 17. GPIO Timing[1]

Num	Characteristic	Symbol	Min	Max	Unit
G1	FB_CLK High to GPIO Output Valid	t_{CHPOV}	—	10	ns
G2	FB_CLK High to GPIO Output Invalid	t_{CHPOI}	1.5	—	ns
G3	GPIO Input Valid to FB_CLK High	t_{PVCH}	9	—	ns
G4	FB_CLK High to GPIO Input Invalid	t_{CHPI}	1.5	—	ns

1 These general purpose specifications apply to the following signals: $\overline{\text{IRQ}}n$, all UART signals, FlexCAN signals, PWM signals, $\overline{\text{DACK}}n$ and $\overline{\text{DREQ}}n$, and all signals configured as GPIO.

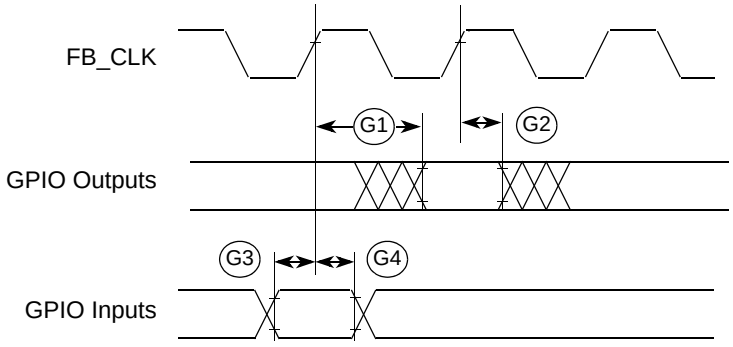


Figure 16. GPIO Timing

5.9 Reset and Configuration Override Timing

Table 18. Reset and Configuration Override Timing

Num	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{\text{RESET}}$ Input valid to FB_CLK High	t_{RVCH}	9	—	ns
R2	FB_CLK High to $\overline{\text{RESET}}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{\text{RESET}}$ Input valid Time [1]	t_{RIVT}	5	—	t_{CYC}
R4	FB_CLK High to $\overline{\text{RSTOUT}}$ Valid	t_{CHROV}	—	10	ns
R5	$\overline{\text{RSTOUT}}$ valid to Config. Overrides valid	t_{ROVCV}	0	—	ns
R6	Configuration Override Setup Time to $\overline{\text{RSTOUT}}$ invalid	t_{COS}	20	—	t_{CYC}
R7	Configuration Override Hold Time after $\overline{\text{RSTOUT}}$ invalid	t_{COH}	0	—	ns
R8	$\overline{\text{RSTOUT}}$ invalid to Configuration Override High Impedance	t_{ROICZ}	—	1	t_{CYC}

1 During low power STOP, the synchronizers for the $\overline{\text{RESET}}$ input are bypassed and $\overline{\text{RESET}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RESET}}$ must be held a minimum of 100 ns.

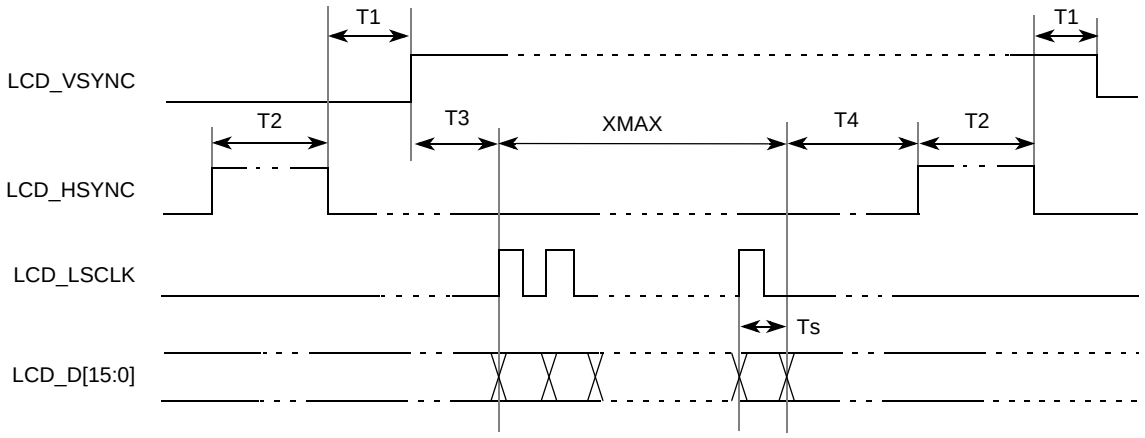


Figure 21. Non-TFT Mode Panel Timing

Table 22. Non-TFT Mode Panel Timing

Num	Characteristic	Min	Value	Unit
T1	LCD_HSYNC to LCD_VSYNC delay	2	HWAIT2 + 2	Tpix
T2	LCD_HSYNC pulse width	1	HWIDTH + 1	Tpix
T3	LCD_VSYNC to LCD_LSCLK	—	0 ≤ T3 ≤ Ts	—
T4	LCD_LSCLK to LCD_HSYNC	1	HWAIT1 + 1	Tpix

Note: Ts is the LCD_LSCLK period while Tpix is the pixel clock period. LCD_VSYNC, LCD_HSYNC, and LCD_LSCLK can be programmed as active high or active low. In Figure 21, all these 3 signals are active high. When it is in CSTN mode or monochrome mode with bus width = 1, T3 = Tpix = Ts. When it is in monochrome mode with bus width = 2, 4 and 8, T3 = 1, 2 and 4 Tpix respectively.

5.11 USB On-The-Go Specifications

The MCF5227x device is compliant with industry standard USB 2.0 specification.

Table 23. USB On-Chip Transceiver DC Characteristics

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Input High	Driven	V_{IH}	2.0	—	—	V
Input Low		V_{IL}	—	—	0.8	V
Input Differential	(DP – DM)	V_{ID}	200	—	00	mV
Differential Common Mode Range		V_{CM}	0.8	—	2.5	V
Single Ended Receive Threshold		V_{SETHR}	0.8	—	2.0	V
Single Ended Receive Hysteresis		V_{SEHYS}	—	400	—	mV
Output High	Driven	V_{OH}	0.0	—	300	mV
Output Low	Driven	V_{OL}	2.8	—	2.0	V
Differential Output Crossover	DP = DM	V_{CRS}	1.3	—	2.0	V

Table 23. USB On-Chip Transceiver DC Characteristics (continued)

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
P side Impedance	Driven	Z_P	6.25	8.25	11.25	Ω
M side Impedance	Driven	Z_M	6.25	8.25	11.25	Ω
Impedance Matching P/M		$Z_{Matching}$	—	0.17	0.23	Ω
Pulldown Resistance[1]		R_{PD}	30k	50k	70k	Ω

1 The pulldown resistors are included to provide a method to keep DP and DM signals in a known quiescent state if desired when the USB port is not being used or when the USB cable is not connected. These on-chip resistors should not be used to provide the 15-kΩ host-mode pulldowns called for in Chapter 7 of the USB Specification, Rev. 1.1 or Rev. 2.0.

Table 24. USB On-Chip Transceiver Full Speed AC Characteristics

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Rise Time	10–90%	t_{LH}	7	11	17.5	ns
Fall Time	90–10%	t_{HL}	7	11	17.5	ns
Rise/Fall Matching	—	$\frac{t_{LH}}{t_{HL}}$ Matching	20	40	60	ps
Rise/Fall Matching, DP and DM	—	$\frac{t_{LH}}{t_{HL}}$ Pad-to-Pad	330	360	640	ps
TIme Skew Between DP and DM	—	t_{SKE}	100	140	210	ps

Table 25. USB On-Chip Transceiver Low Speed AC Characteristics

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Rise Time	10–90%	t_{LH}	75	—	300	ns
Fall Time	90–10%	t_{HL}	75	—	300	ns
Rise/Fall Matching	$\frac{t_{LH}}{t_{HL}}$	$\frac{t_{LH}}{t_{HL}}$ Matching	80	—	125	%

5.12 SSI Timing Specifications

This section provides the AC timings for the SSI in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (SSI_TCR[TSCKP] = 0, SSI_RCR[RSCKP] = 0) and a non-inverted frame sync (SSI_TCR[TFSI] = 0, SSI_RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SSI_BCLK) and/or the frame sync (SSI_FS) shown in the figures below.

Table 26. SSI Timing—Master Modes[1]

Num	Characteristic	Symbol	Min	Max	Unit	Notes
S1	SSI_MCLK cycle time	t_{MCLK}	$4 \times 1/f_{SYS}$	—	ns	2
S2	SSI_MCLK pulse width high / low		45%	55%	t_{MCLK}	
S3	SSI_BCLK cycle time	t_{BCLK}	$4 \times 1/f_{SYS}$	—	ns	3
S4	SSI_BCLK pulse width		45%	55%	t_{BCLK}	

Table 26. SSI Timing—Master Modes[1] (continued)

Num	Characteristic	Symbol	Min	Max	Unit	Notes
S5	SSI_BCLK to SSI_FS output valid		—	10	ns	
S6	SSI_BCLK to SSI_FS output invalid		0	—	ns	
S7	SSI_BCLK to SSI_TXD valid		—	10	ns	
S8	SSI_BCLK to SSI_TXD invalid / high impedence		0	—	ns	
S9	SSI_RXD / SSI_FS input setup before SSI_BCLK		10	—	ns	
S10	SSI_RXD / SSI_FS input hold after SSI_BCLK		0	—	ns	

1 All timings specified with a capactive load of 25pF.

2 SSI_MCLK can be generated from SSI_CLKIN or a divided version of the internal system clock (SYSCLK).

3 SSI_BCLK can be derived from SSI_CLKIN or a divided version of SYSCLK. If the SYSCLK is used, the minimum divider is 6. If the SSI_CLKIN input is used, the programmable dividers must be set to ensure that SSI_BCLK does not exceed 4 x f_{SYS}.

Table 27. SSI Timing—Slave Modes[1]

Num	Characteristic	Symbol	Min	Max	Unit	Notes
S11	SSI_BCLK cycle time	t_{BCLK}	$4 \times 1/f_{SYS}$	—	ns	
S12	SSI_BCLK pulse width high / low		45%	55%	t_{BCLK}	
S13	SSI_FS input setup before SSI_BCLK		10	—	ns	
S14	SSI_FS input hold after SSI_BCLK		2	—	ns	
S15	SSI_BCLK to SSI_TXD / SSI_FS output valid		—	10	ns	
S16	SSI_BCLK to SSI_TXD / SSI_FS output invalid / high impedence		0	—	ns	
S17	SSI_RXD setup before SSI_BCLK		10	—	ns	
S18	SSI_RXD hold after SSI_BCLK		2	—	ns	

1 All timings specified with a capactive load of 25 pF.

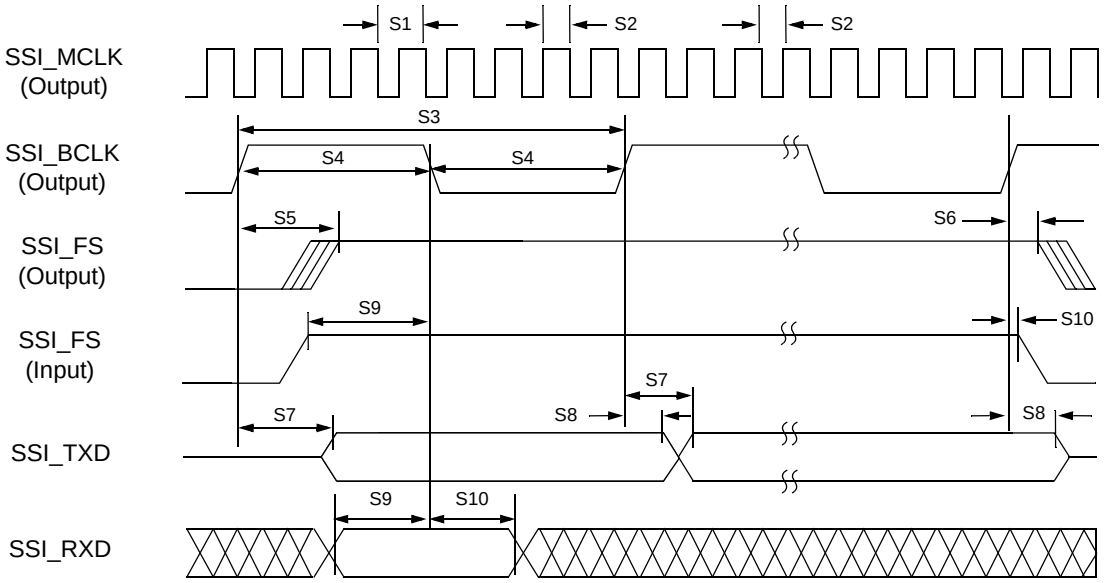


Figure 22. SSI Timing—Master Modes

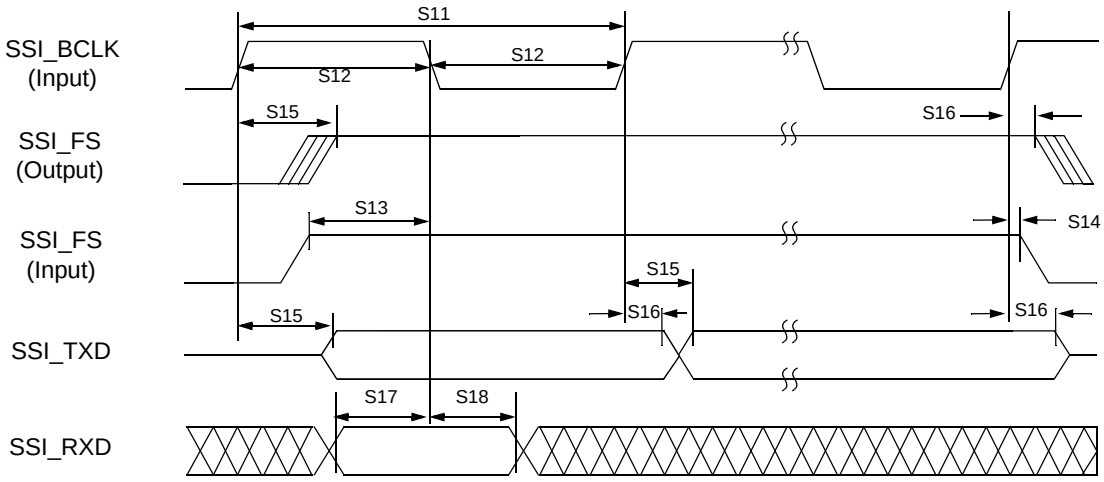


Figure 23. SSI Timing—Slave Modes

5.13 I²C Timing Specifications

Table 28 lists specifications for the I²C input timing parameters shown in Figure 24.

Table 28. I²C Input Timing Specifications between SCL and SDA

Num	Characteristic	Min	Max	Unit
I1	Start condition hold time	2	—	t_{cyc}
I2	Clock low period	8	—	t_{cyc}
I3	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	ms
I4	Data hold time	0	—	ns

Table 28. I²C Input Timing Specifications between SCL and SDA (continued)

Num	Characteristic	Min	Max	Unit
I5	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	1	ms
I6	Clock high time	4	—	t_{cyc}
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	2	—	t_{cyc}
I9	Stop condition setup time	2	—	t_{cyc}

Table 29 lists specifications for the I²C output timing parameters shown in Figure 24.

Table 29. I²C Output Timing Specifications between SCL and SDA

Num	Characteristic	Min	Max	Unit
I1[1]	Start condition hold time	6	—	t_{cyc}
I2[1]	Clock low period	10	—	t_{cyc}
I3[2]	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	—	µs
I4[1]	Data hold time	7	—	t_{cyc}
I5[3]	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	3	ns
I6[1]	Clock high time	10	—	t_{cyc}
I7[1]	Data setup time	2	—	t_{cyc}
I8[1]	Start condition setup time (for repeated start condition only)	20	—	t_{cyc}
I9[1]	Stop condition setup time	10	—	t_{cyc}

1 Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 29. The I²C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 29 are minimum values.

2 Because I2C_SCL and I2C_SDA are open-collector-type outputs, which the processor can only actively drive low, the time I2C_SCL or I2C_SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Specified at a nominal 50-pF load.

Figure 24 shows timing for the values in Table 29 and Table 28.

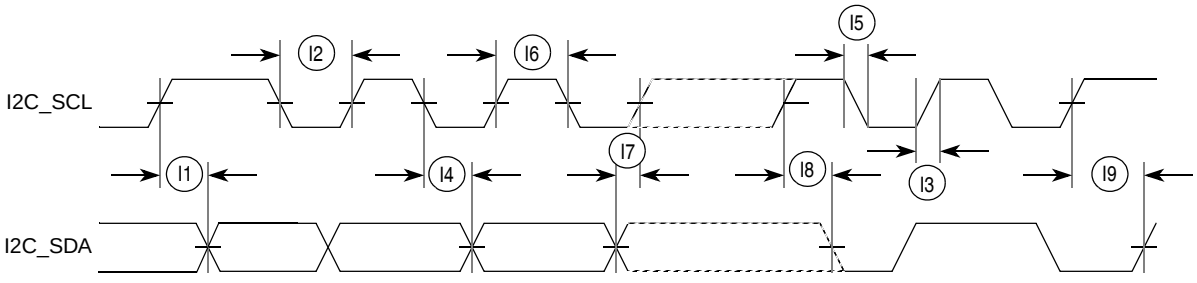


Figure 24. I²C Input/Output Timings

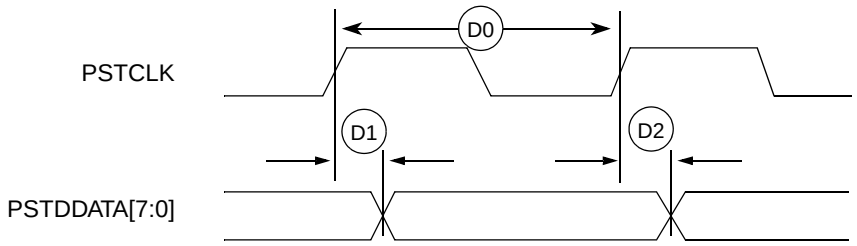


Figure 32. Real-Time Trace AC Timing

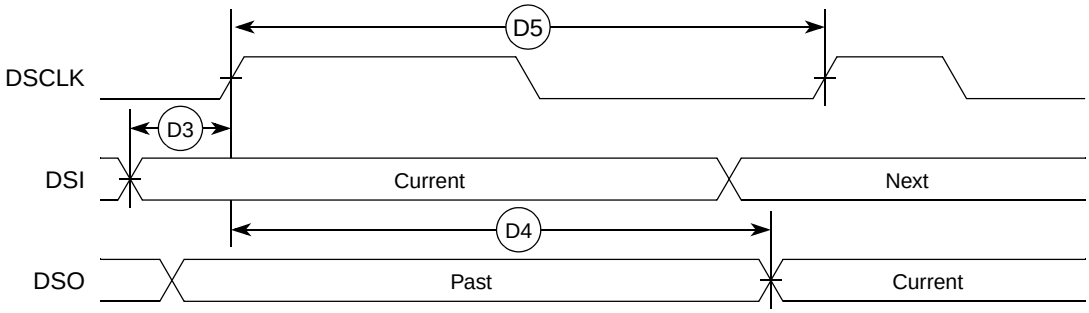


Figure 33. BDM Serial Port AC Timing

6 Package Information

The latest package outline drawings are available on the product summary pages on our web site: http://www.freescale.com/coldfire. The following table lists the case outline numbers per device. Use these numbers in the web page's keyword search engine to find the latest package outline drawings.

Table 35. Package Information

Device	Package Type	Mask Set	Revision	Case Outline Numbers
MCF52274	176 LQFP	All	All	98ASS23479W
MCF52277	196 MAPBGA	M26H	1.1	98ASH98061A
		2M26H, 3M26H	1.2–1.3	98ARH98390A

7 Product Documentation

Documentation is available from a local Freescale distributor, a Freescale sales office, the Freescale Literature Distribution Center, or through the Freescale world-wide web address at http://www.freescale.com/coldfire.

8 Revision History

Table 36 summarizes revisions to this document.

Table 36. MCF52277 Data Sheet Revision History

Rev. No.	Date of Release	Summary of Changes
3	02/2008	Initial public revision.
4	05/2008	Corrected MCF52274 order number from MCF52274CAB120 to MCF52274CLU120 in Table 2
5	07/2008	Corrected MCF52277CVM166 part number to MCF52277CVM160 in Table 2. Although, this device has a maximum rated frequency of 166.67 MHz.
6	07/2008	Added data to Section 3.5, "Power Consumption Specifications."
7	02/2009	Changed document type from Data Sheet: Advance Information to Data Sheet: Technical Data and corresponding footnote on first page Replaced t_{SYS} with $1/f_{SYS}$ throughout Changed the following specs in Table 14 and Table 15: • Minimum frequency of operation from TBD to 60MHz • Maximum clock period from TBD to 16.67 ns Added RTC and Oscillator Supply Voltage specs to Table 7 and Table 10 In Table 8: • Updated thermal characteristics for the 196 MAPBGA package • Added thermal characteristics for the 176 LQFP package that were TBD In Table 11: • Corrected maximum crystal reference frequency range from 66.67 to 25 MHz • Added footnotes to maximum crystal and external reference frequency ranges • Changed minimum core/system and CLKOUT frequencies from TBD to 512 and 256 Hz, respectively. In Table 12: • Added Typical column • Removed Internal Reference Voltage spec as it isn't necessary • Moved Current Consumption specs from maximum column to typical column • Added INL and DNL specs that were TBD, and changed the unit footnote • Replaced Gain and Offset Error specs with Full-Scale and Zero-Scale Error • Removed Input Leakage Current and Input Current specs as they aren't necessary Removed Gain Calculations section as it isn't necessary
8	09/2009	Iin Table 35, added case outline number for MCF52277 masks 2M26H and 3M26H