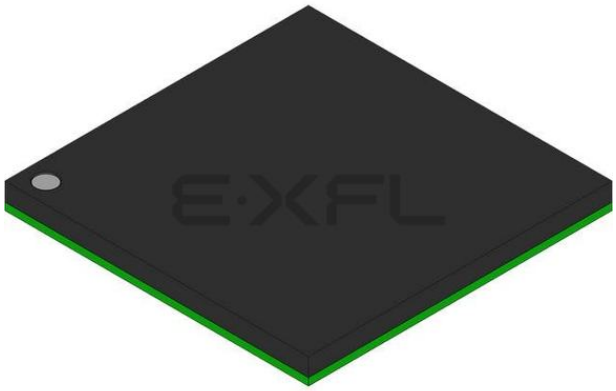

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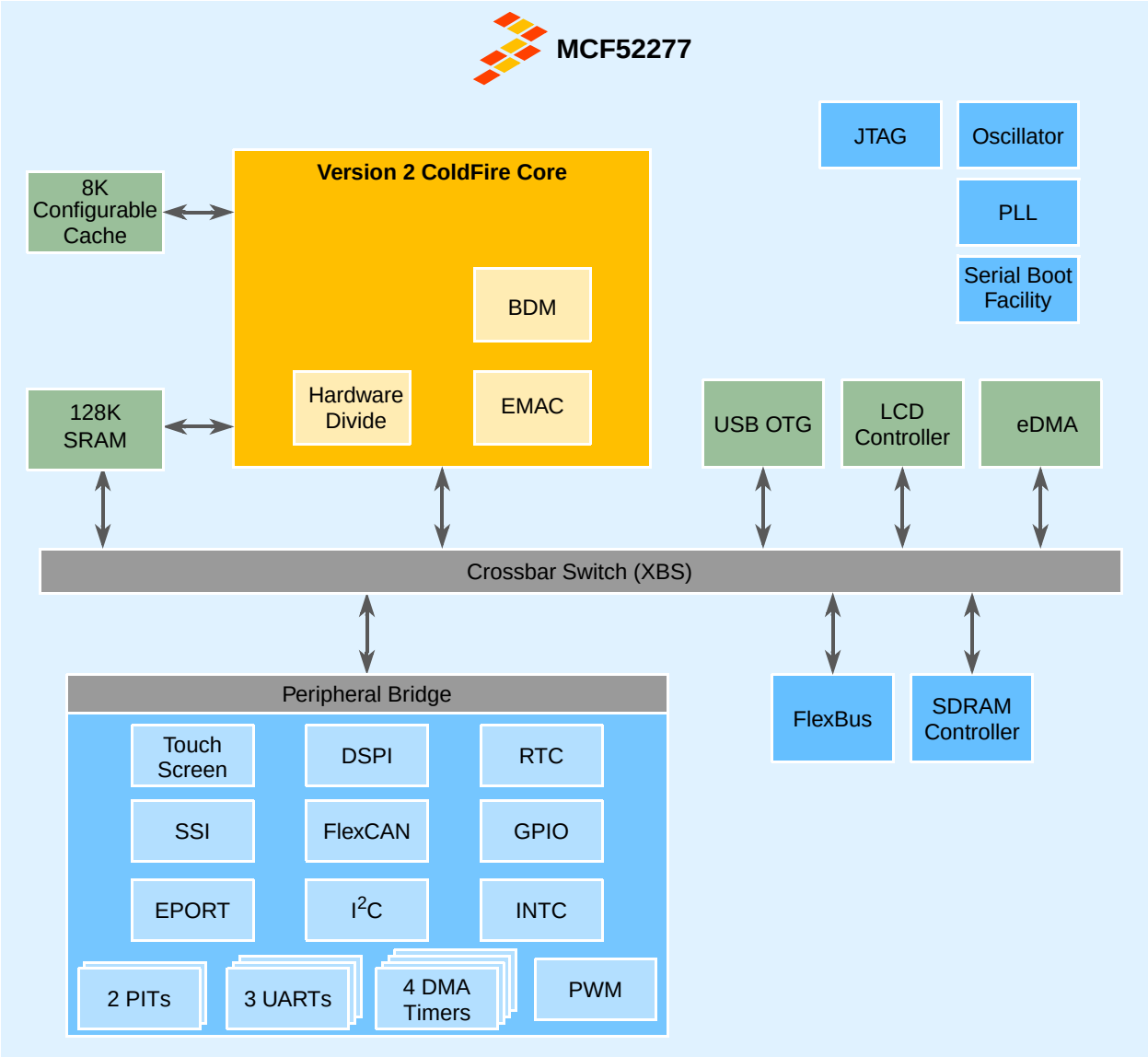
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	166.67MHz
Connectivity	CANbus, EBI/EMI, I²C, SPI, SSI, UART/USART, USB OTG
Peripherals	DMA, LCD, PWM, WDT
Number of I/O	55
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.4V ~ 1.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	196-LBGA
Supplier Device Package	196-MAPBGA (15x15)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf52277cvm160j



LEGEND

BDM	– Background debug module	**LCD**	– Liquid-crystal display
DSPI	– DMA serial peripheral interface	**PIT**	– Programmable interrupt timer
eDMA	– Enhanced direct memory access	**PLL**	– Phase-locked loop module
EMAC	– Enchanced multiply-accumulate unit	**PWM**	– Pulse-width modulator
EPORT	– Edge port module	**RTC**	– Real time clock
GPIO	– General purpose input/output module	**SSI**	– Synchronous serial interface
I^2C	– Inter-intergrated circuit	**UART**	– Universal asynchronous receiver/transmitter
INTC	– Interrupt controller	**USB OTG**	– Universal Serial Bus On-the-Go controller
JTAG	– Joint Test Action Group interface		

Figure 1. MCF52277 Block Diagram

3.3 ADC Power Filtering

To minimize noise, an external filters is required for the $ADCV_{DD}$ power pin. The filter shown in Figure 4 should be connected between the board EV_{DD} and the $ADCV_{DD}$ pin. The resistor and capacitors should be placed as close to the dedicated $ADCV_{DD}$ pin as possible.

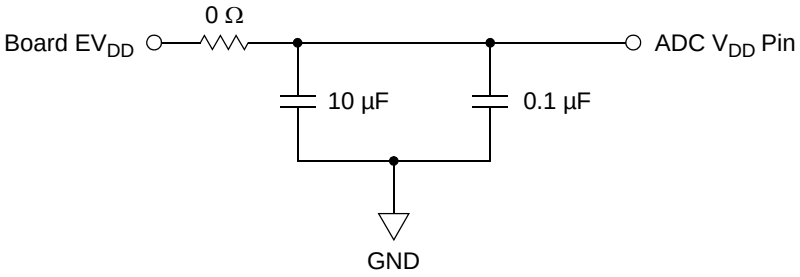


Figure 4. ADC V_{DD} Power Filter

3.4 Supply Voltage Sequencing

The relationship between SDV_{DD} and EV_{DD} is non-critical during power-up and power-down sequences. Both SDV_{DD} (2.5V or 3.3V) and EV_{DD} are specified relative to IV_{DD}.

3.4.1 Power Up Sequence

If EV_{DD}/SDV_{DD} are powered up with IV_{DD} at 0 V, then the sense circuits in the I/O pads will cause all pad output drivers connected to the EV_{DD}/SDV_{DD} to be in a high impedance state. There is no limit on how long after EV_{DD}/SDV_{DD} powers up before IV_{DD} must powered up. IV_{DD} should not lead the EV_{DD}, SDV_{DD} or $PLLV_{DD}$ by more than 0.4 V during power ramp-up, or there will be high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 500 us to avoid turning on the internal ESD protection clamp diodes.

3.4.2 Power Down Sequence

If $IV_{DD}/PLLV_{DD}$ are powered down first, then sense circuits in the I/O pads will cause all output drivers to be in a high impedance state. There is no limit on how long after IV_{DD} and $PLLV_{DD}$ power down before EV_{DD} or SDV_{DD} must power down. IV_{DD} should not lag EV_{DD}, SDV_{DD}, or $PLLV_{DD}$ going low by more than 0.4 V during power down or there will be undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop $IV_{DD}/PLLV_{DD}$ to 0 V.
2. Drop EV_{DD}/SDV_{DD} supplies.

3.5 Power Consumption Specifications

All application power consumption data is lab data measured on an M52277EVB running the Freescale Linux BSP.

Table 3. MCF52277 Application Power Consumption[1]

Core Freq.		Idle (LCD image)	Idle (audio image)	Button Demo	Slideshow Demo	MP3 Playback	USB FS File Copy	Units
160 MHz	IV_{DD}	61.4	59.2	84.7	96.5	89.2	89.5	mA
	EV_{DD}	28.87	25.73	35.3	34.6	33.46	29.86	
	SDV_{DD}	18.8	18.57	21.8	23.9	22.66	22.2	
	Total Power	**221.211**	**207.135**	**282.78**	**301.95**	**285.006**	**272.748**	**mW**

1 All voltage rails at nominal values: IV_{DD} = 1.5 V, EV_{DD} = 3.3 V, and SDV_{DD} = 1.8 V.

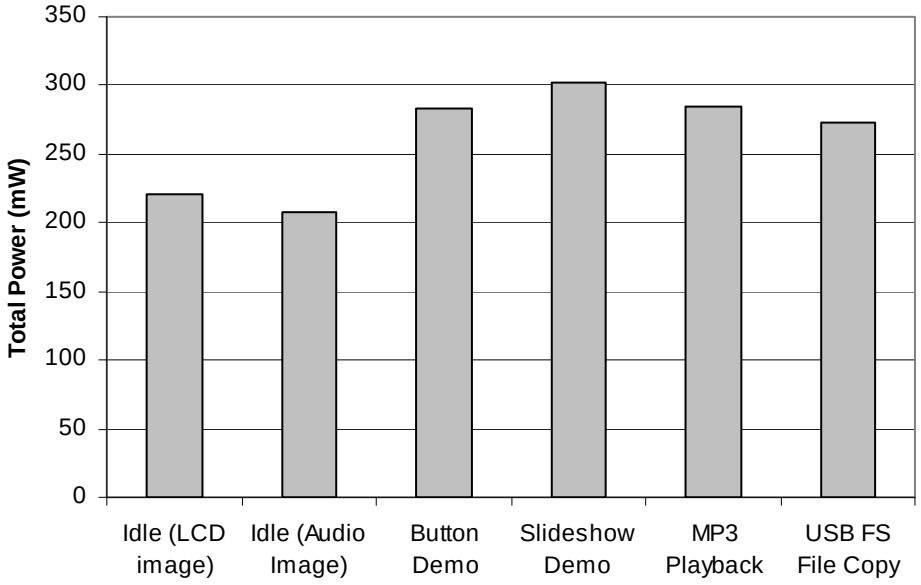


Figure 5. Power Consumption in Various Applications

All current consumption data is lab data measured on a single device using an evaluation board. Table 4 shows the typical power consumption in low-power modes. These current measurements are taken after executing a STOP instruction.

Table 4. Current Consumption in Low-Power Modes[1,2]

Mode	Voltage Supply	System Frequency				
		80MHz	64MHz	48MHz	32MHz	4MHz (LIMP mode)
RUN	IV_{DD} (mA)	75.1	62.7	49.2	36.6	3.5
	Power (mW)	112.65	94.05	73.80	54.90	5.25
WAIT	IV_{DD} (mA)	61.9	52.8	42.0	31.7	2.9
	Power (mW)	92.85	79.20	63.00	47.55	4.35

Table 6. MCF5227*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF52274 176 LQFP	MCF52277 196 MAPBGA
ALLPST	—	—	—	—	O	EVDD	76	—
JTAG_EN	—	—	—	D	I	EVDD	79	K10
PSTCLK	—	TCLK	—	U	O	EVDD	74	P8
DSI	—	TDI	—	U	I	EVDD	78	M11
DSO	—	TDO	—	—	O	EVDD	81	L11
$\overline{\text{BKPT}}$	—	TMS	—	U	I	EVDD	80	N11
DSCLK	—	$\overline{\text{TRST}}$	—	U	I	EVDD	77	P11
Test								
TEST	—	—	—	D	I	EVDD	134	E10
Power Supplies								
IVDD	—	—	—	—	—	—	39, 75, 114, 138, 171	K5, F10, E5, J10
EVDD	—	—	—	—	—	—	12, 72, 73, 94, 111, 148, 176	E6, E7, F5, F6, G5, H9, J9, K8, K9
SD_VDD	—	—	—	—	—	—	14, 43, 44, 70, 113, 132, 146	E8, E9, F9, G9, H5, J5, J6, K6, K7
VDD_OSC	—	—	—	—	—	—	108	G13
VDD_PLL	—	—	—	—	—	—	104	H14
VDD_USB	—	—	—	—	—	—	151	B10
VDD_RTC	—	—	—	—	—	—	101	J13
VDD_ADC	—	—	—	—	—	—	91	L13
VSS	—	—	—	—	—	—	1, 13, 45, 71, 93, 112, 133, 147	F7, F8, G6–G8, H6–H8, J7, J8
VSS_OSC	—	—	—	—	—	—	107	H13
VSS_ADC	—	—	—	—	—	—	92	L14

1 Pull-ups are generally only enabled on pins with their primary function, except as noted.

2 Refers to pin's primary function.

3 Enabled only in oscillator bypass mode (internal crystal oscillator is disabled).

4 GPIO functionality is determined by the edge port module. The GPIO module is only responsible for assigning the alternate functions.

5 Pull-up when $\overline{\text{DREQ}}$ controls the pin.

6 The 176 LQFP device only supports a 12-bit LCD data bus.

7 DSPI or SBF signal functionality is controlled by $\overline{\text{RESET}}$. When asserted, these pins are configured for serial boot; when negated, the pins are configured for DSPI.

8 Pull-up when the serial boot facility (SBF) controls the pin.

9 If JTAG_EN is asserted, these pins default to alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.

4.2 Pinout—176 LQFP

The pinout for the MCF52274 package is shown below.

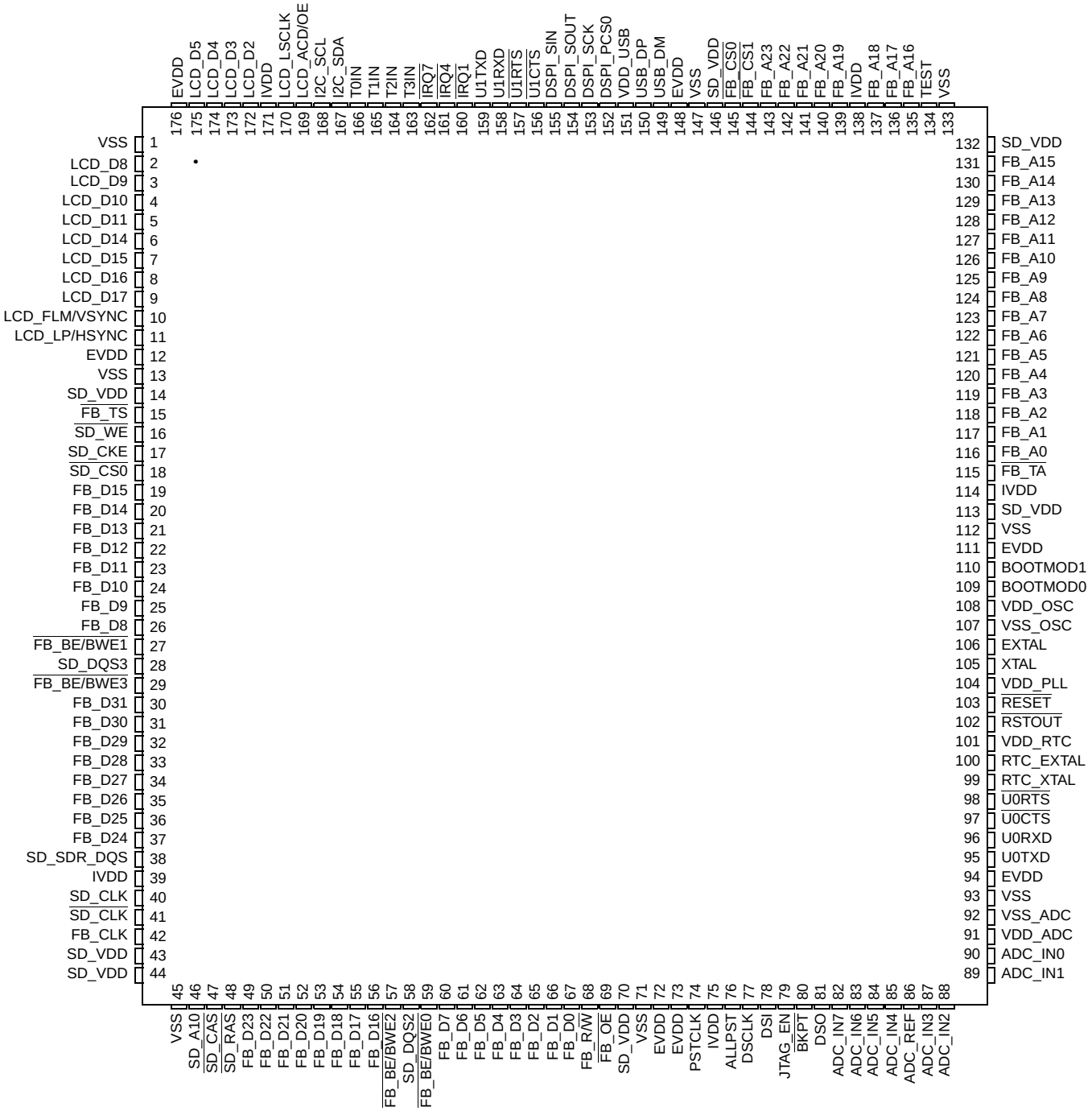


Figure 7. MCF52274 Pinout (176 LQFP)

4.3 Pinout—196 MAPBGA

The pinout for the MCF52277 package is shown below.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	LCD_D6	LCD_D5	LCD_D4	LCD_D2	LCD_ LSCLK	T0IN	U1TXD	U1RXD	USB_DM	USB_DP	FB_CS2	FB_A21	FB_A17	FB_A16	A
B	LCD_D8	LCD_D7	LCD_D3	LCD_D1	LCD_ ACD/OE	T1IN	IRQ_1	U1RTS	DSPI_ PCS0	VDD_ USB	FB_CS3	FB_A20	FB_A18	FB_A15	B
C	LCD_D13	LCD_D12	LCD_D10	LCD_D0	I2C_SCL	T2IN	IRQ_4	U1CTS	DSPI_ SCK	FB_CS0	FB_A23	FB_A19	FB_A14	FB_A13	C
D	LCD_D15	LCD_D14	LCD_D11	LCD_D9	I2C_SDA	T3IN	IRQ_7	DSPI_SIN	DSPI_ SOUT	FB_CS1	FB_A22	FB_A12	FB_A11	FB_A10	D
E	LCD_LP/ HSYNC	LCD_FLM/ VSYNC	LCD_D17	LCD_D16	IVDD	EVDD	EVDD	SDVDD	SDVDD	TEST	FB_A9	FB_A8	FB_A7	FB_A6	E
F	SD_CS0	SD_CKE	SD_WE	FB_TS	EVDD	EVDD	VSS	VSS	SDVDD	IVDD	FB_A5	FB_A4	FB_A3	EXTAL	F
G	FB_D15	FB_D14	FB_D13	FB_D12	EVDD	VSS	VSS	VSS	SDVDD	BOOT MOD1	FB_A2	FB_A1	VDD_ OSC	XTAL	G
H	FB_D11	FB_D10	FB_D9	FB_D8	SDVDD	VSS	VSS	VSS	EVDD	BOOT MOD0	FB_A0	FB_TA	VSS_ OSC	VDD_ PLL	H
J	FB_BE/ BWE1	SD_DQS3	FB_BE/ BWE3	FB_D31	SDVDD	SDVDD	VSS	VSS	EVDD	IVDD	RESET	U0RTS	VDD_ RTC	RTC_ EXTAL	J
K	FB_D30	FB_D29	FB_D28	FB_D27	IVDD	SDVDD	SDVDD	EVDD	EVDD	JTAG_EN	RSTOUT	U0CTS	U0RXD	RTC_ XTAL	K
L	FB_D26	FB_D25	FB_D24	SD_A10	FB_D17	FB_BE/ BWE0	FB_D4	FB_D0	PST3	DDATA3	TDO	U0TXD	VDD_ ADC	VSS_ ADC	L
M	SD_CLK	SD_ SDR_DQS	FB_D23	FB_D20	FB_D16	FB_D7	FB_D3	FB_R/W	PST2	DDATA2	TDI	ADC_ REF	ADC_IN1	ADC_IN0	M
N	SD_CLK	SD_CAS	FB_D22	FB_D19	FB_BE/ BWE2	FB_D6	FB_D2	FB_OE	PST1	DDATA1	TMS	ADC_IN6	ADC_IN4	ADC_IN2	N
P	FB_CLK	SD_RAS	FB_D21	FB_D18	SD_ DQS0	FB_D5	FB_D1	TCLK	PST0	DDATA0	TRST	ADC_IN7	ADC_IN5	ADC_IN3	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 8. MCF52277 Pinout (196 MAPBGA)

5 Electrical Characteristics

This document contains electrical specification tables and reference timing diagrams for the MCF5227x microprocessor. This section contains detailed information on DC/AC electrical characteristics and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle, however for production silicon these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this MCU document supersede any values found in the module specifications.

5.1 Maximum Ratings

Table 7. Absolute Maximum Ratings[1, 2]

Characteristic	Symbol	Value	Unit
Core Supply Voltage	IV_{DD}	–0.5 to +2.0	V
CMOS Pad Supply Voltage	EV_{DD}	–0.3 to +4.0	V
DDR/Memory Pad Supply Voltage	SDV_{DD}	–0.3 to +4.0	V
Oscillator Supply Voltage	$OSCV_{DD}$	–0.3 to +4.0	V
PLL Supply Voltage	$PLLV_{DD}$	–0.3 to +2.0	V
RTC Supply Voltage	$RTCV_{DD}$	–0.5 to +2.0	V
Digital Input Voltage [3]	V_{IN}	–0.3 to +3.6	V
Instantaneous Maximum Current Single pin limit (applies to all pins) [3, 4, 5]	I_D	25	mA
Operating Temperature Range (Packaged)	T_A (T_L – T_H)	–40 to +85	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C

1 Functional operating conditions are given in Section 5.4, “DC Electrical Specifications.” Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Continued operation at these levels may affect device reliability or cause permanent damage to the device.

2 This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or EV_{DD}).

3 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

4 All functional non-supply pins are internally clamped to V_{SS} and EV_{DD}.

5 Power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions. If positive injection current (V_{in} > EV_{DD}) is greater than I_{DD}, the injection current may flow out of EV_{DD} and could result in external power supply going out of regulation. Insure external EV_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power (ex; no clock). Power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions.

5.3 ESD Protection

Table 9. ESD Protection Characteristics[1,2]

Characteristic	Symbol	Value	Unit
ESD Target for Human Body Model	HBM	2000	V

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

5.4 DC Electrical Specifications

Table 10. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Core Supply Voltage	IV_{DD}	1.4	1.6	V
PLL Supply Voltage	$PLLV_{DD}$	1.4	1.6	V
RTC Supply Voltage	$RTCV_{DD}$	1.4	1.6	V
CMOS Pad Supply Voltage	EV_{DD}	3.0	3.6	V
SDRAM and FlexBus Supply Voltage Mobile DDR/Bus Pad Supply Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{DD}	 1.7 2.25 3.0	 1.95 2.75 3.6	V
USB Supply Voltage	$USBV_{DD}$	3.0	3.6	V
Oscillator Supply Voltage	$OSCV_{DD}$	3.0	3.6	V
CMOS Input High Voltage	EV_{IH}	2	EV_{DD} + 0.3	V
CMOS Input Low Voltage	EV_{IL}	V_{SS} – 0.3	0.8	V
CMOS Output High Voltage I_{OH} = –5.0 mA	EV_{OH}	EV_{DD} – 0.4	—	V
CMOS Output Low Voltage I_{OL} = 5.0 mA	EV_{OL}	—	0.4	V
SDRAM and FlexBus Input High Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{IH}	 1.35 1.7 2	 SDV_{DD} + 0.3 SDV_{DD} + 0.3 SDV_{DD} + 0.3	V
SDRAM and FlexBus Input Low Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V)	SDV_{IL}	 V_{SS} – 0.3 V_{SS} – 0.3 V_{SS} – 0.3	 0.45 0.8 0.8	V

Table 10. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
SDRAM and FlexBus Output High Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V) I_{OH} = –5.0 mA for all modes	SDV_{OH}	 1.4 2.1 2.4	 — — —	V
SDRAM and FlexBus Output Low Voltage Mobile DDR/Bus Input High Voltage (nominal 1.8V) DDR/Bus Pad Supply Voltage (nominal 2.5V) SDR/Bus Pad Supply Voltage (nominal 3.3V) I_{OL} = 5.0 mA for all modes	SDV_{OL}	 — — —	 0.3 0.3 0.5	V
Input Leakage Current V_{in} = V_{DD} or V_{SS}, Input-only pins	I_{in}	–1.0	1.0	µA
Weak Internal Pull-Up Device Current, tested at V_{IL} Max.[1]	I_{APU}	–10	–130	µA
Input Capacitance [2] All input-only pins All input/output (three-state) pins	C_{in}	 — —	 7 7	pF

1 Refer to the signals section for pins having weak internal pull-up devices.

2 This parameter is characterized before qualification rather than 100% tested.

5.5 Oscillator and PLL Electrical Characteristics

Table 11. PLL Electrical Characteristics

Num	Characteristic	Symbol	Min	Max	Unit
1	PLL Reference Frequency Range Crystal reference External reference	 $f_{ref\_crystal}$ f_{ref_ext}	 16 16	 25[1] 66.67[1]	 MHz MHz
2	Core/system frequency CLKOUT Frequency	f_{sys} $f_{sys/2}$	512 Hz[2] 256 Hz[2]	166.67 83.33	MHz MHz
3	Crystal Start-up Time[3,4]	t_{cst}	—	10	ms
4	EXTAL Input High Voltage Crystal Mode[5] All other modes (External, Limp)	 V_{IHEXT} V_{IHEXT}	 V_{XTAL} + 0.4 E_{VDD}/2 + 0.4	 — —	 V V
5	EXTAL Input Low Voltage Crystal Mode[5] All other modes (External, Limp)	 V_{ILEXT} V_{ILEXT}	 — —	 V_{XTAL} – 0.4 E_{VDD}/2 – 0.4	 V V
7	PLL Lock Time [3,6]	t_{lpll}	—	50000	CLKIN
8	Duty cycle of reference[3]	t_{dc}	40	60	%
9	XTAL Current	I_{XTAL}	1	3	mA
10	Total on-chip stray capacitance on XTAL	C_{S_XTAL}	—	1.5	pF
11	Total on-chip stray capacitance on EXTAL	C_{S_EXTAL}	—	1.5	pF
12	Crystal capacitive load	C_L	See crystal spec		

Table 11. PLL Electrical Characteristics (continued)

Num	Characteristic	Symbol	Min	Max	Unit
13	Discrete load capacitance for XTAL Discrete load capacitance for EXTAL	C_{L_XTAL} C_{L_EXTAL}	—	$2 \times (C_L - C_{S\_XTAL} - C_{S\_EXTAL} - C_{S\_PCB})$[7]	pF
14	Frequency un-LOCK Range	f_{UL}	–4.0	4.0	% f_{sys}
15	Frequency LOCK Range	f_{LCK}	–2.0	2.0	% f_{sys}
17	CLKOUT period jitter [4, 5, 8] measured at f_{sys} max Peak-to-peak jitter (Clock edge to clock edge) Long-term jitter	C_{jitter}	 — —	 10 TBD	 % $f_{sys/2}$ % $f_{sys/2}$
19	VCO frequency ($f_{vco} = f_{ref} \times PFDR$)	f_{vco}	350	540	MHz

1 Although these are the allowable frequency ranges, do not violate the VCO frequency range of the PLL. See the *MCF5227x Reference Manual* for more details.

2 The minimum system frequency is the minimum input clock divided by the maximum low-power divider (16 MHz ÷ 32,768). When the PLL is enabled, the minimum system frequency (f_{sys}) is 37.5 MHz.

3 This parameter is guaranteed by characterization before qualification rather than 100% tested. Applies to external clock reference only.

4 Proper PC board layout procedures must be followed to achieve specifications.

5 This parameter is guaranteed by design rather than 100% tested.

6 This specification is the PLL lock time only and does not include oscillator start-up time..

7 C_{S_PCB} is the measured PCB stray capacitance on EXTAL and XTAL.

8 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via PLL V_{DD}, EV_{DD}, and V_{SS} and variation in crystal oscillator frequency increase the Cjitter percentage for a given interval.

5.6 ASP Electrical Characteristics

Table 12 lists the electrical specifications for the ASP module.

Table 12. ASP Electrical Characteristics

Characteristic	Symbol	Min	Typical	Max	Unit
ASP Analog Supply Voltage	V_{DDA}	3.0	—	3.6	V
Input Voltage Range	V_{ADIN}	0	—	V_{DDA}	V
Operating Current Consumption	I_{DDA_ON}	—	700	—	uA
Power-down Current Consumption	I_{DDA_OFF}	—	1	—	uA
Resolution	R_{ES}	—	—	12	bits
Sampling rate		—	—	125	kS/s
Integral Non-linearity	INL	—	±8	±24	lsb[1]
Differential Non-linearity	DNL	—	±2	±24	lsb[1]
ADC Internal Clock Frequency	t_{AIC}	2	—	8	MHz
Conversion Range	R_{AD}	0	—	V_{DDA}	V

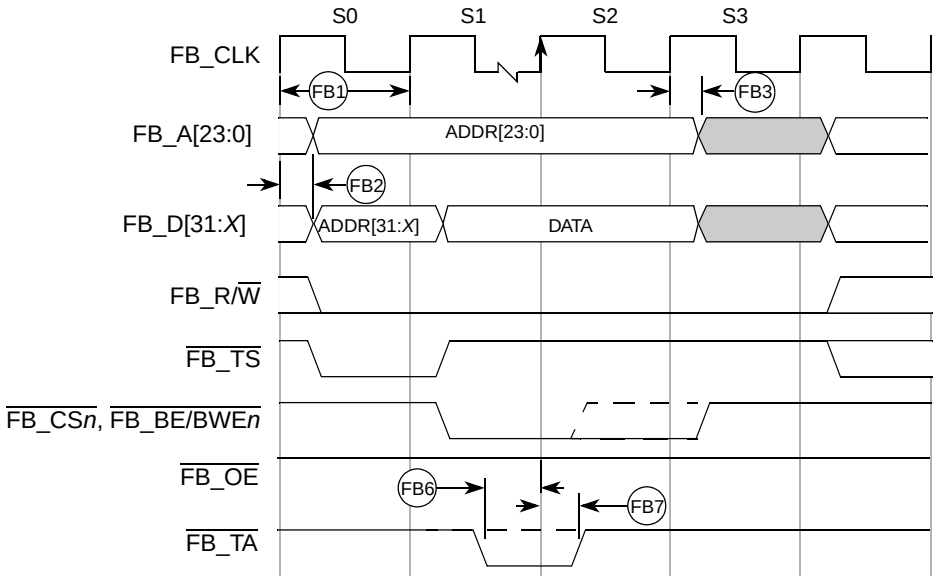


Figure 10. Flexbus Write Timing

5.7.2 SDRAM Bus

The SDRAM controller supports accesses to main SDRAM memory from any internal master. It supports either standard SDRAM or double data rate (DDR) SDRAM, but it does not support both at the same time.

5.7.2.1 SDR SDRAM AC Timing Specifications

The following timing numbers indicate when data will be latched or driven onto the external bus, relative to the memory bus clock, when operating in SDR mode on write cycles and relative to SD_DQS on read cycles. The device's SDRAM controller is a DDR controller that has an SDR mode. Because it is designed to support DDR, a DQS pulse must still be supplied to the device for each data beat of an SDR read. The processor accomplishes this by asserting a signal named SD_SDR_DQS during read cycles. Care must be taken during board design to adhere to the following guidelines and specs with regard to the SD_SDR_DQS signal and its usage.

Table 14. SDR Timing Specifications

Num	Characteristic	Symbol	Min	Max	Unit	Notes
	Frequency of Operation		60	83.33	MHz	1
SD1	Clock Period	t_{SDCK}	12.0	16.67	ns	2
SD2	Pulse Width High	t_{SDCKH}	0.45	0.55	SD_CLK	3
SD3	Pulse Width Low	t_{SDCKH}	0.45	0.55	SD_CLK	3
SD4	Address, SD_CKE, $\overline{\text{SD\_CAS}}$, $\overline{\text{SD\_RAS}}$, $\overline{\text{SD\_WE}}$, SD_BA, SD_CS[1:0] - Output Valid	$t_{SDCHACV}$	—	0.5 × SD_CLK + 1.0	ns	
SD5	Address, SD_CKE, $\overline{\text{SD\_CAS}}$, $\overline{\text{SD\_RAS}}$, $\overline{\text{SD\_WE}}$, SD_BA, SD_CS[1:0] - Output Hold	$t_{SDCHACI}$	2.0	—	ns	
SD6	SD_SDR_DQS Output Valid	t_{DQSOV}	—	Self timed	ns	4
SD7	SD_DQS[3:2] input setup relative to SD_CLK	$t_{DQVSDCH}$	0.25 × SD_CLK	0.40 × SD_CLK	ns	5

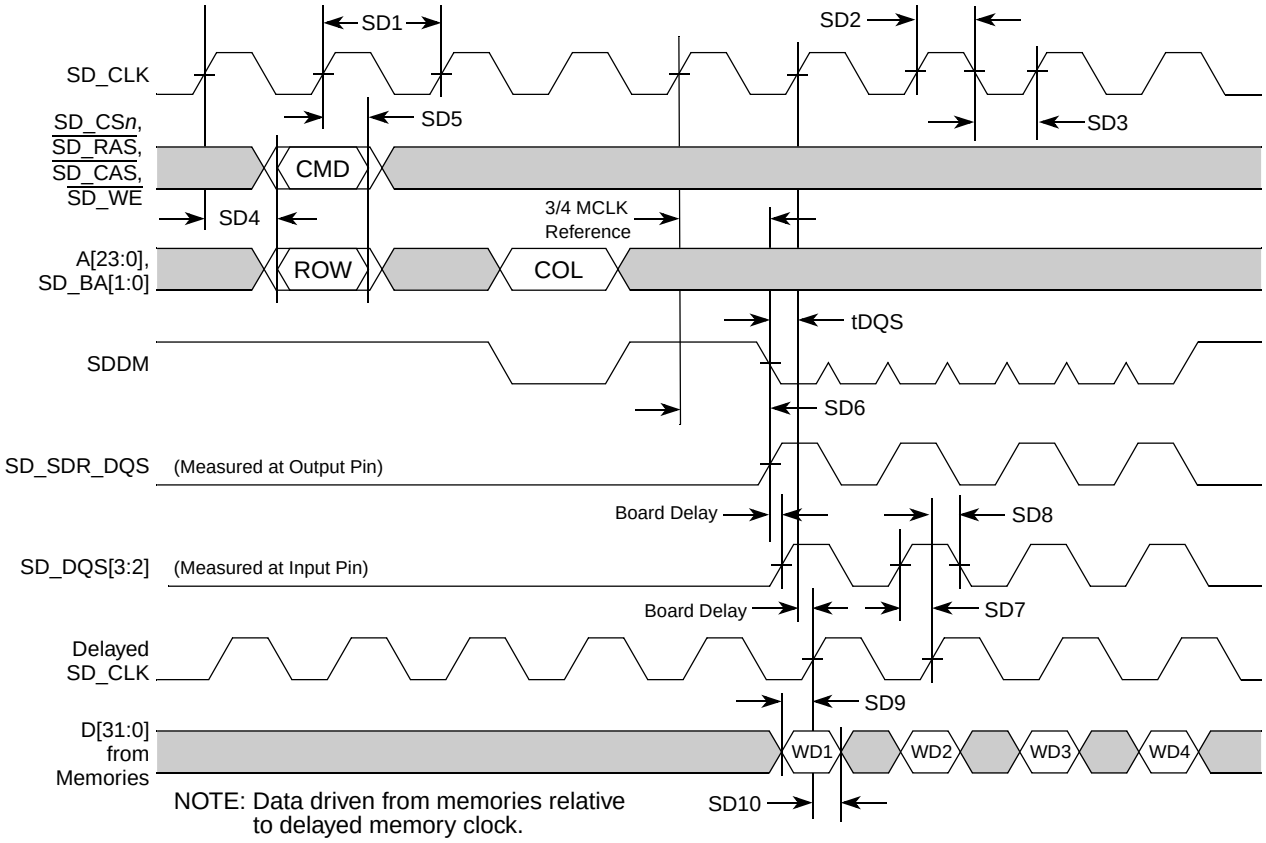


Figure 12. SDR Read Timing

5.7.2.2 DDR SDRAM AC Timing Specifications

When using the SDRAM controller in DDR mode, the following timing numbers must be followed to properly latch or drive data onto the memory bus. All timing numbers are relative to the two DQS byte lanes.

Table 15. DDR Timing Specifications

Num	Characteristic	Symbol	Min	Max	Unit	Notes
	Frequency of Operation	t_{DDCK}	60	83.33	MHz	1
DD1	Clock Period	t_{DDSK}	12.0	16.67	ns	2
DD2	Pulse Width High	t_{DDCKH}	0.45	0.55	SD_CLK	3
DD3	Pulse Width Low	t_{DDCKL}	0.45	0.55	SD_CLK	3
DD4	Address, SD_CKE, $\overline{\text{SD\_CAS}}$, $\overline{\text{SD\_RAS}}$, $\overline{\text{SD\_WE}}$, $\overline{\text{SD\_CS}}$[1:0] - Output Valid	$t_{SDCHACV}$	—	0.5 × SD_CLK + 1.0	ns	4
DD5	Address, SD_CKE, $\overline{\text{SD\_CAS}}$, $\overline{\text{SD\_RAS}}$, $\overline{\text{SD\_WE}}$, $\overline{\text{SD\_CS}}$[1:0] - Output Hold	$t_{SDCHACI}$	2.0	—	ns	
DD6	Write Command to first DQS Latching Transition	t_{CMDVDQ}	—	1.25	SD_CLK	
DD7	Data and Data Mask Output Setup (DQ→DQS) Relative to DQS (DDR Write Mode)	t_{DQDMV}	1.5	—	ns	5 6

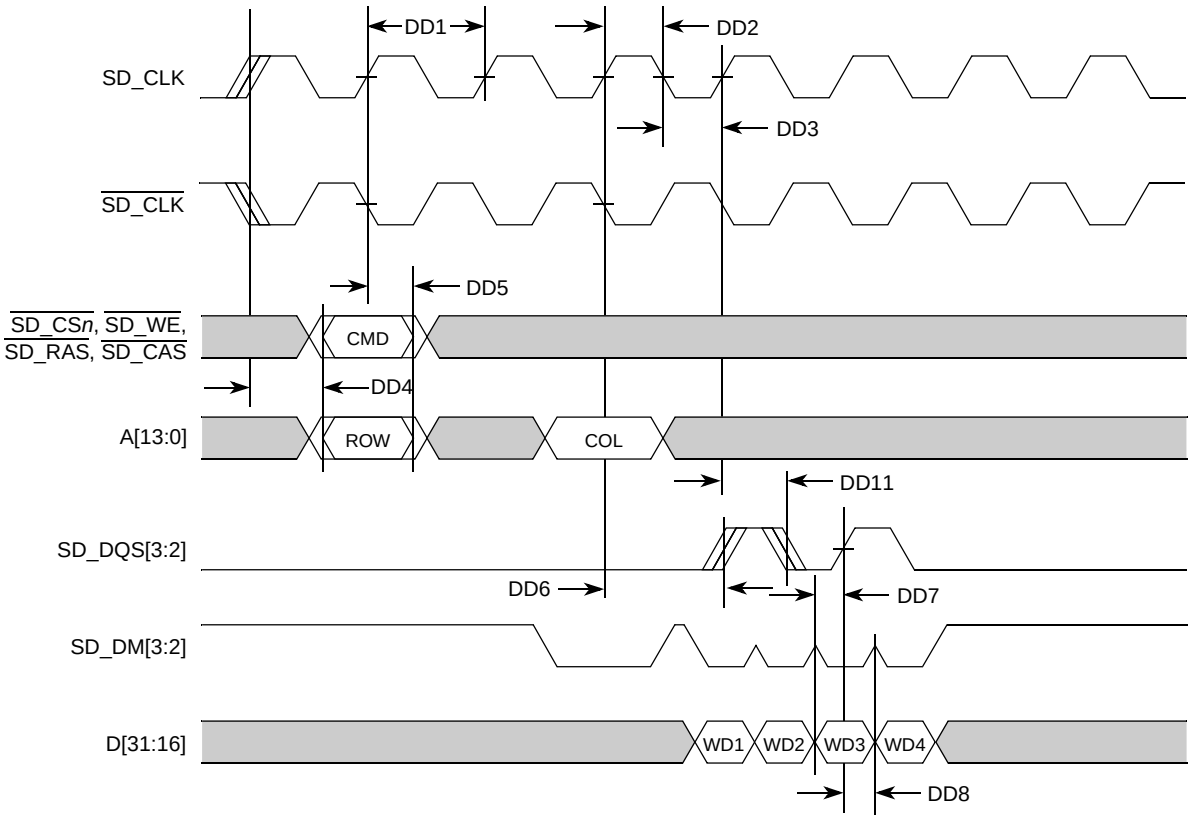


Figure 13. DDR Write Timing

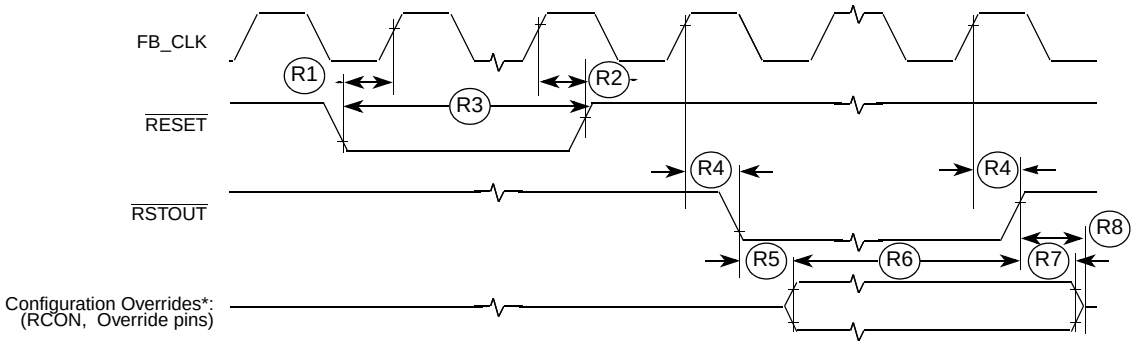


Figure 17. RESET and Configuration Override Timing

NOTE

Refer to the CCM chapter of the *MCF52277 Reference Manual* for more information.

5.10 LCD Controller Timing Specifications

This sections lists the timing specifications for the LCD Controller.

Table 19. LCD_LSCLK Timing

Num	Characteristic	Min	Max	Unit
T1	LCD_LSCLK Period	25	2000	ns
T2	Pixel data setup time	11	—	ns
T3	Pixel data up time	11	—	ns

Note: The pixel clock is equal to LCD_LSCLK / (PCD + 1). When it is in CSTN, TFT, or monochrome mode with bus width = 1, LCD_LSCLK is equal to the pixel clock. When it is in monochrome with other bus width settings, LCD_LSCLK is equal to the pixel clock divided by bus width. The polarity of LCD_LSCLK and LCD_D signals can also be programmed.

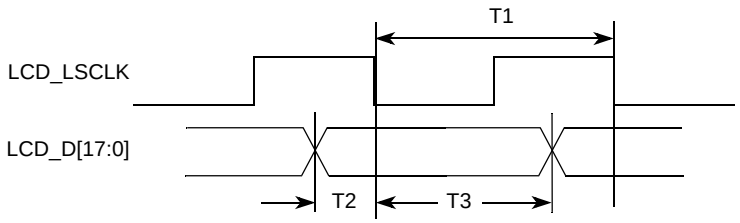


Figure 18. LCD_LSCLK to LCD_D[17:0] timing diagram

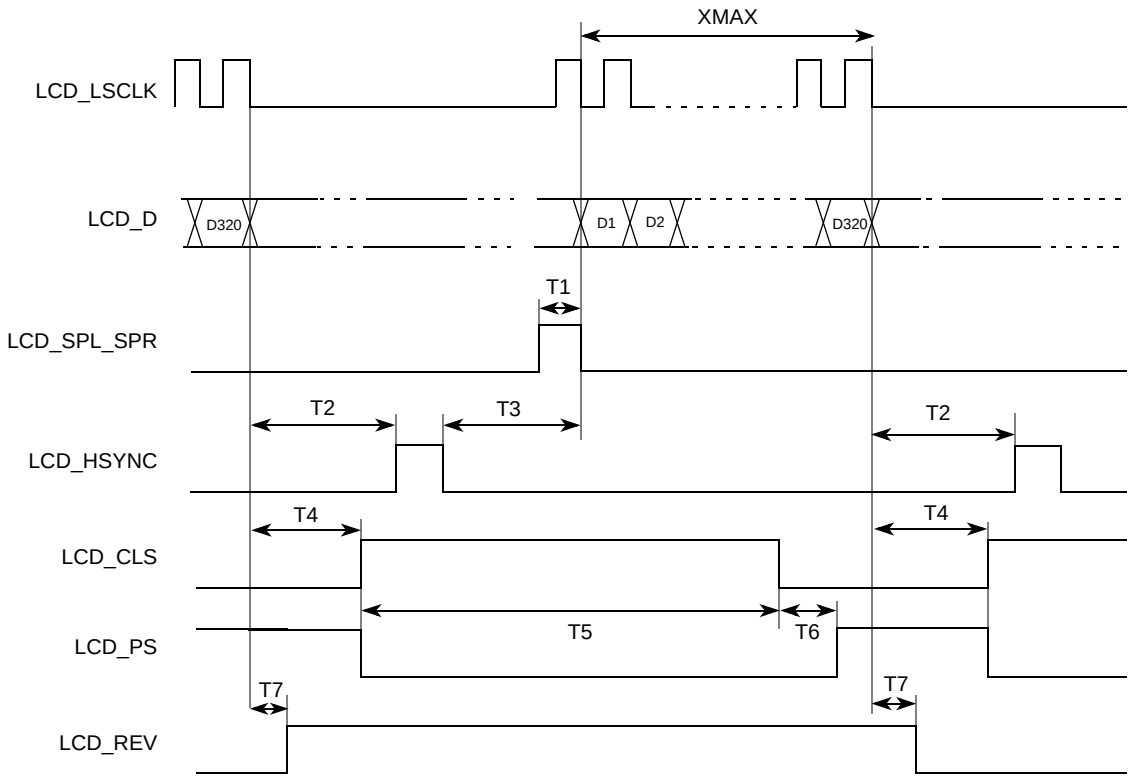


Figure 20. Sharp TFT Panel Timing

Table 21. Sharp TFT Panel Timing

Num	Characteristic	Min	Value	Unit
T1	LCD_SPL/LCD_SPR pulse width	—	1	Ts
T2	End of LCD_D of line to beginning of LCD_HSYNC	1	HWAIT1+1	Ts
T3	End of LCD_HSYNC to beginning of LCD_D of line	4	HWAIT2 + 4	Ts
T4	LCD_CLS rise delay from end of LCD_D of line	3	CLS_RISE_DELAY+1	Ts
T5	LCD_CLS pulse width	1	CLS_HI_WIDTH+1	Ts
T6	LCD_PS rise delay from LCD_CLS negation	0	PS_RISE_DELAY	Ts
T7	LCD_REV toggle delay from last LCD_D of line	1	REV_TOGGLE_DELAY+1	Ts

Note: Falling of LCD_SPL/LCD_SPR aligns with first LCD_D of line.

Note: Falling of LCD_PS aligns with rising edge of LCD_CLS.

Note: LCD_REV toggles in every LCD_HSYN period.

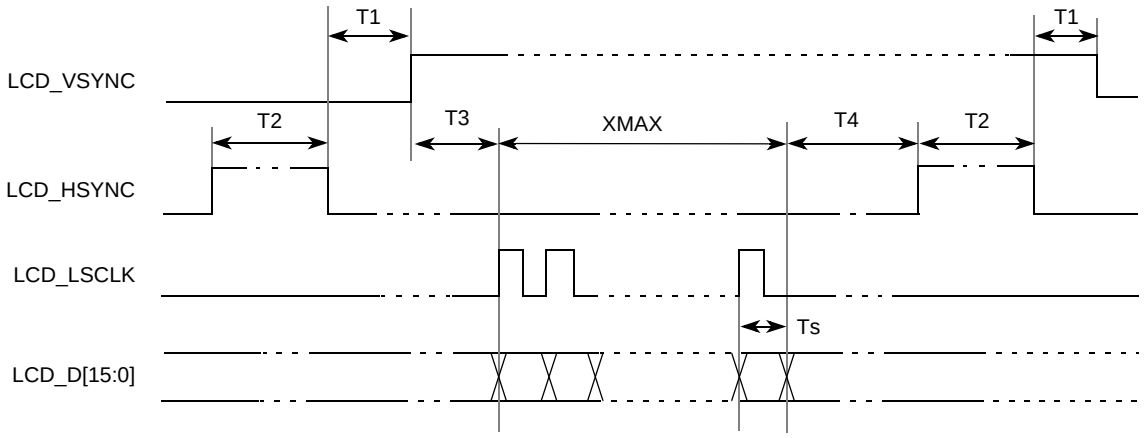


Figure 21. Non-TFT Mode Panel Timing

Table 22. Non-TFT Mode Panel Timing

Num	Characteristic	Min	Value	Unit
T1	LCD_HSYNC to LCD_VSYNC delay	2	HWAIT2 + 2	Tpix
T2	LCD_HSYNC pulse width	1	HWIDTH + 1	Tpix
T3	LCD_VSYNC to LCD_LSCLK	—	0 ≤ T3 ≤ Ts	—
T4	LCD_LSCLK to LCD_HSYNC	1	HWAIT1 + 1	Tpix

Note: Ts is the LCD_LSCLK period while Tpix is the pixel clock period. LCD_VSYNC, LCD_HSYNC, and LCD_LSCLK can be programmed as active high or active low. In Figure 21, all these 3 signals are active high. When it is in CSTN mode or monochrome mode with bus width = 1, T3 = Tpix = Ts. When it is in monochrome mode with bus width = 2, 4 and 8, T3 = 1, 2 and 4 Tpix respectively.

5.11 USB On-The-Go Specifications

The MCF5227x device is compliant with industry standard USB 2.0 specification.

Table 23. USB On-Chip Transceiver DC Characteristics

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Input High	Driven	V_{IH}	2.0	—	—	V
Input Low		V_{IL}	—	—	0.8	V
Input Differential	(DP – DM)	V_{ID}	200	—	00	mV
Differential Common Mode Range		V_{CM}	0.8	—	2.5	V
Single Ended Receive Threshold		V_{SETHR}	0.8	—	2.0	V
Single Ended Receive Hysteresis		V_{SEHYS}	—	400	—	mV
Output High	Driven	V_{OH}	0.0	—	300	mV
Output Low	Driven	V_{OL}	2.8	—	2.0	V
Differential Output Crossover	DP = DM	V_{CRS}	1.3	—	2.0	V

5.14 DMA Timer Timing Specifications

Table 30 lists timer module AC timings.

Table 30. Timer Module AC Timing Specifications

Num	Characteristic	Min	Max	Unit
T1	DT0IN / DT1IN / DT2IN / DT3IN cycle time	3	—	t_{CYC}
T2	DT0IN / DT1IN / DT2IN / DT3IN pulse width	1	—	t_{CYC}

5.15 DSPI Timing Specifications

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with both master and slave operations. Many of the transfer attributes are programmable. Table 31 provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the *MCF52277 Reference Manual* for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 31. DSPI Module AC Timing Specifications[1]

Num	Characteristic	Symbol	Min	Max	Unit	Notes
DS1	DSPI_SCK Cycle Time	t_{SCK}	4 x $1/f_{SYS}$	—	ns	[2]
DS2	DSPI_SCK Duty Cycle	—	(tsck ÷ 2) – 2.0	(tsck ÷ 2) + 2.0	ns	
Master Mode						
DS3	DSPI_PCS*n* to DSPI_SCK delay	t_{CSC}	$(2 \times 1/f_{SYS}) - 2.0$	—	ns	[3]
DS4	DSPI_SCK to DSPI_PCS*n* delay	t_{ASC}	$(2 \times 1/f_{SYS}) - 3.0$	—	ns	[4]
DS5	DSPI_SCK to DSPI_SOUT valid	—	—	5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	—	–5	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	—	9	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	—	0	—	ns	
Slave Mode						
DS9	DSPI_SCK to DSPI_SOUT valid	—	—	4	ns	
DS10	DSPI_SCK to DSPI_SOUT invalid	—	0	—	ns	
DS11	DSPI_SIN to DSPI_SCK input setup	—	2	—	ns	
DS12	DSPI_SCK to DSPI_SIN input hold	—	7	—	ns	
DS13	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	—	20	ns	
DS14	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	—	18	ns	

1 Timings shown are for DMCR[MTFE] = 0 (classic SPI) and DCTAR*n*[CPHA] = 0. Data is sampled on the DSPI_SIN pin on the odd-numbered DSPI_SCK edges and driven on the DSPI_SOUT pin on even-numbered DSPI edges.

2 When in master mode, the baud rate is programmable in DCTAR*n*[PBR] and DCTAR*n*[BR].

3 The DSPI_PCS*n* to DSPI_SCK delay is programmable in DCTAR*n*[PCSSCK] and DCTAR*n*[CSSCK].

4 The DSPI_SCK to DSPI_PCS*n* delay is programmable in DCTAR*n*[PASC] and DCTAR*n*[ASC].

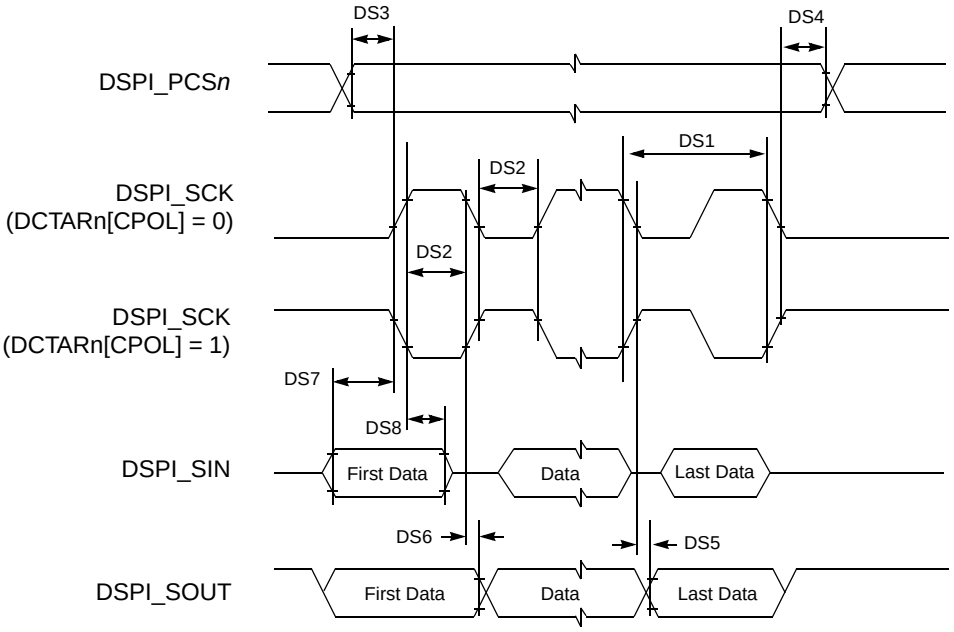


Figure 25. DSPI Classic SPI Timing—Master Mode

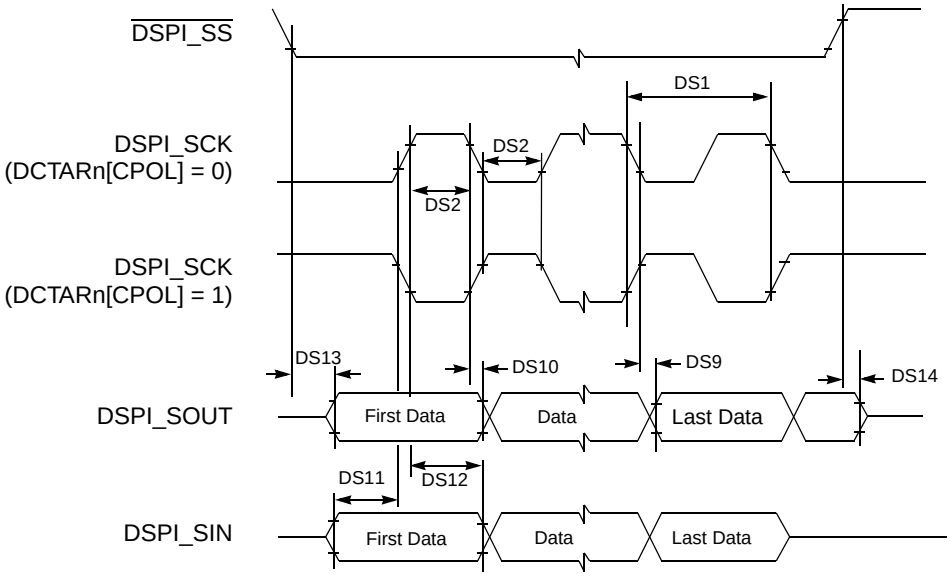


Figure 26. DSPI Classic SPI Timing—Slave Mode

5.16 SBF Timing Specifications

The Serial Boot Facility (SBF) provides a means to read configuration information and system boot code from a broad array of SPI-compatible EEPROMs, flashes, FRAMs, nVSRAMs, etc. Table 32 provides the AC timing specifications for the SBF.

Table 33. JTAG and Boundary Scan Timing (continued)

Num	Characteristic[1]	Symbol	Min	Max	Unit
J9	TMS, TDI Input Data Setup Time to TCLK Rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input Data Hold Time after TCLK Rise	t_{TAPBHT}	10	—	ns
J11	TCLK Low to TDO Data Valid	t_{TDODV}	0	26	ns
J12	TCLK Low to TDO High Z	t_{TDODZ}	0	8	ns
J13	$\overline{\text{TRST}}$ Assert Time	t_{TRSTAT}	100	—	ns
J14	$\overline{\text{TRST}}$ Setup Time (Negation) to TCLK High	t_{TRSTST}	10	—	ns

1 JTAG_EN is expected to be a static signal. Hence, specific timing is not associated with it.

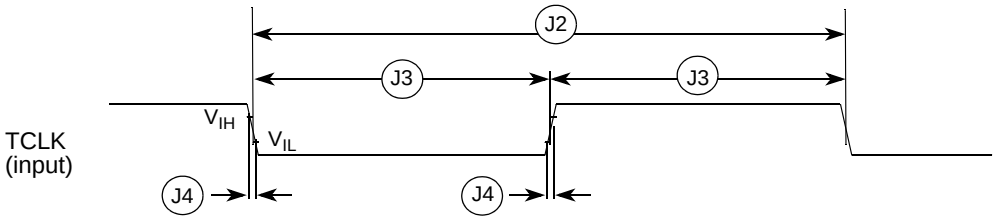


Figure 28. Test Clock Input Timing

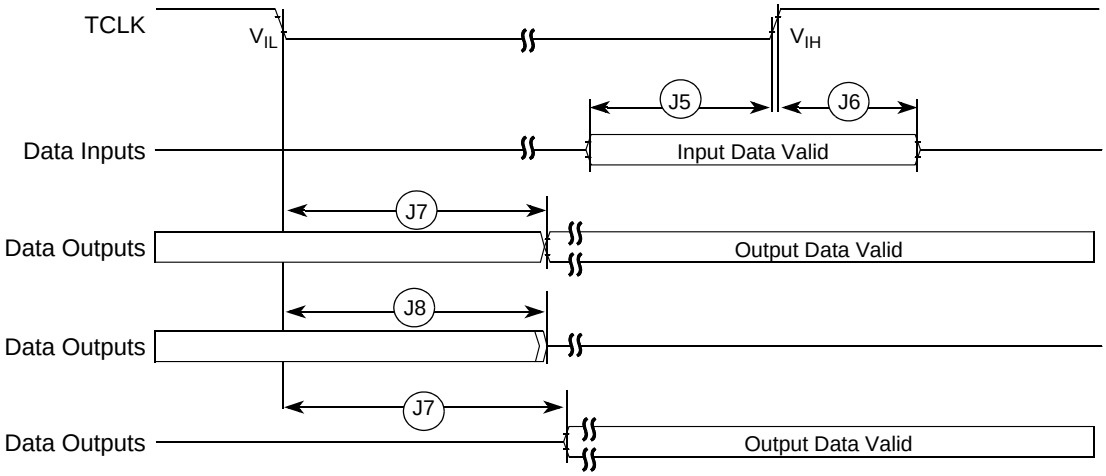


Figure 29. Boundary Scan (JTAG) Timing

8 Revision History

Table 36 summarizes revisions to this document.

Table 36. MCF52277 Data Sheet Revision History

Rev. No.	Date of Release	Summary of Changes
3	02/2008	Initial public revision.
4	05/2008	Corrected MCF52274 order number from MCF52274CAB120 to MCF52274CLU120 in Table 2
5	07/2008	Corrected MCF52277CVM166 part number to MCF52277CVM160 in Table 2. Although, this device has a maximum rated frequency of 166.67 MHz.
6	07/2008	Added data to Section 3.5, "Power Consumption Specifications."
7	02/2009	Changed document type from Data Sheet: Advance Information to Data Sheet: Technical Data and corresponding footnote on first page Replaced t_{SYS} with $1/f_{SYS}$ throughout Changed the following specs in Table 14 and Table 15: • Minimum frequency of operation from TBD to 60MHz • Maximum clock period from TBD to 16.67 ns Added RTC and Oscillator Supply Voltage specs to Table 7 and Table 10 In Table 8: • Updated thermal characteristics for the 196 MAPBGA package • Added thermal characteristics for the 176 LQFP package that were TBD In Table 11: • Corrected maximum crystal reference frequency range from 66.67 to 25 MHz • Added footnotes to maximum crystal and external reference frequency ranges • Changed minimum core/system and CLKOUT frequencies from TBD to 512 and 256 Hz, respectively. In Table 12: • Added Typical column • Removed Internal Reference Voltage spec as it isn't necessary • Moved Current Consumption specs from maximum column to typical column • Added INL and DNL specs that were TBD, and changed the unit footnote • Replaced Gain and Offset Error specs with Full-Scale and Zero-Scale Error • Removed Input Leakage Current and Input Current specs as they aren't necessary Removed Gain Calculations section as it isn't necessary
8	09/2009	Iin Table 35, added case outline number for MCF52277 masks 2M26H and 3M26H