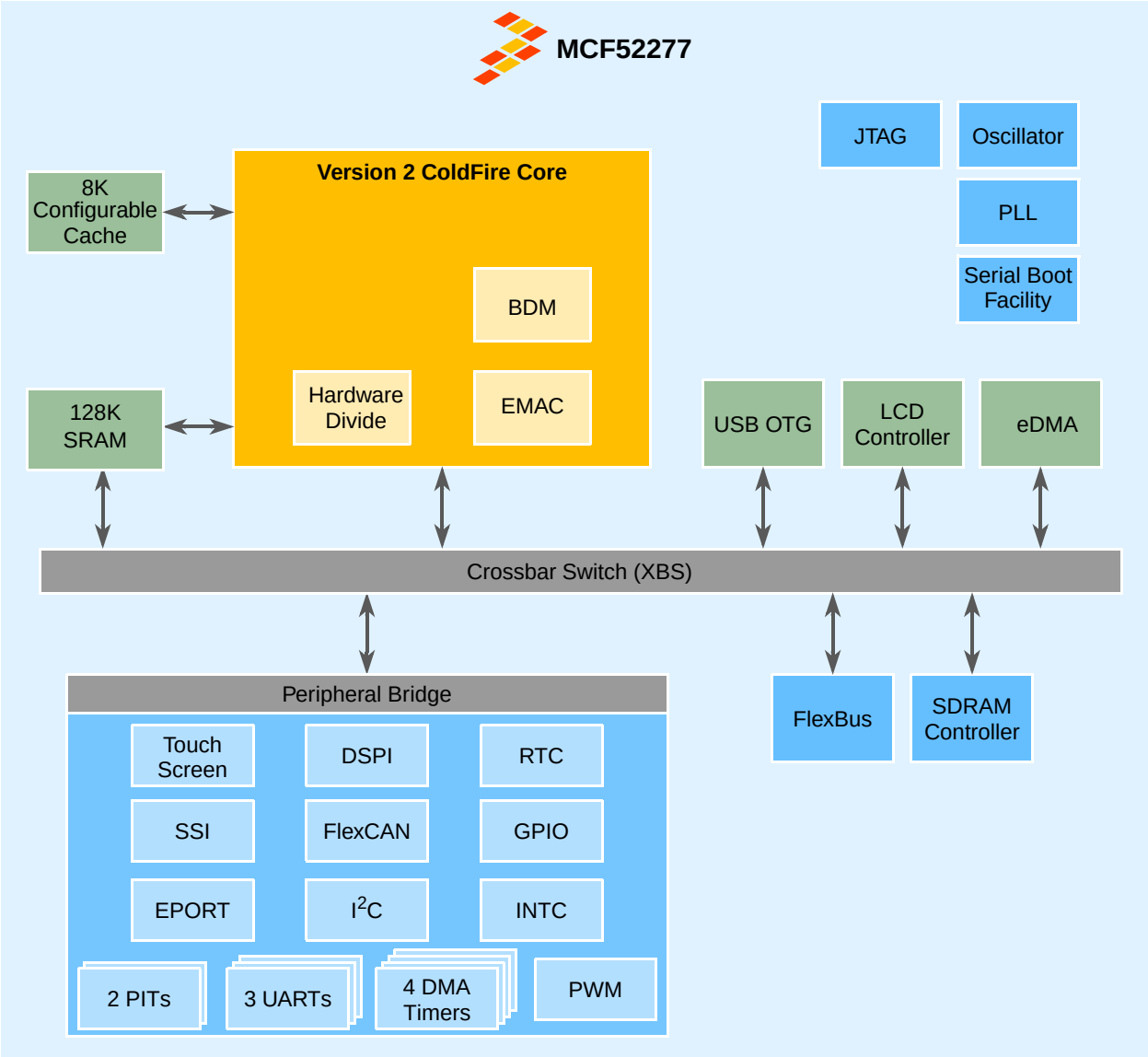
Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, I²C, SPI, SSI, UART/USART, USB OTG
Peripherals	DMA, LCD, PWM, WDT
Number of I/O	47
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.4V ~ 1.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/pcf52274clu120



LEGEND

BDM	– Background debug module	**LCD**	– Liquid-crystal display
DSPI	– DMA serial peripheral interface	**PIT**	– Programmable interrupt timer
eDMA	– Enhanced direct memory access	**PLL**	– Phase-locked loop module
EMAC	– Enchanced multiply-accumulate unit	**PWM**	– Pulse-width modulator
EPORT	– Edge port module	**RTC**	– Real time clock
GPIO	– General purpose input/output module	**SSI**	– Synchronous serial interface
I^2C	– Inter-intergrated circuit	**UART**	– Universal asynchronous receiver/transmitter
INTC	– Interrupt controller	**USB OTG**	– Universal Serial Bus On-the-Go controller
JTAG	– Joint Test Action Group interface		

Figure 1. MCF52277 Block Diagram

1 MCF5227x Family Comparison

The following table compares the various device derivatives available within the MCF5227*x* family.

Table 1. MCF5227*x* Family Configurations

Module	MCF52274	MCF52277
ColdFire Version 2 Core with EMAC (Enhanced Multiply-Accumulate Unit)	•	•
Core (System) Clock	up to 120 MHz	up to 166.67 MHz
Peripheral and External Bus Clock (Core clock ÷ 2)	up to 60 MHz	up to 83.33 MHz
Performance (Dhrystone/2.1 MIPS)	up to 114	up to 159
Static RAM (SRAM)	128 Kbytes	
Configurable Cache	8 Kbytes	
ASP Touchscreen Controller	•	•
LCD Controller	12-bit color	18-bit color
USB 2.0 On-the-Go	•	•
FlexBus External Interface	•	•
SDR/DDR SDRAM Controller	•	•
FlexCAN 2.0B communication module	•	•
Real Time Clock	•	•
Watchdog Timer	•	•
16-channel Direct Memory Access (DMA)	•	•
Interrupt Controllers (INTC)	1	1
Synchronous Serial Interface (SSI)	•	•
I^2C	•	•
DSPI	•	•
UARTs	3	3
32-bit DMA Timers	4	4
Periodic Interrupt Timers (PIT)	2	2
PWM Module	•	•
Edge Port Module (EPORT)	•	•
General Purpose I/O Module (GPIO)	•	•
JTAG - IEEE® 1149.1 Test Access Port	•	•
Package	176 LQFP	196 MAPBGA

3.5 Power Consumption Specifications

All application power consumption data is lab data measured on an M52277EVB running the Freescale Linux BSP.

Table 3. MCF52277 Application Power Consumption[1]

Core Freq.		Idle (LCD image)	Idle (audio image)	Button Demo	Slideshow Demo	MP3 Playback	USB FS File Copy	Units
160 MHz	IV_{DD}	61.4	59.2	84.7	96.5	89.2	89.5	mA
	EV_{DD}	28.87	25.73	35.3	34.6	33.46	29.86	
	SDV_{DD}	18.8	18.57	21.8	23.9	22.66	22.2	
	Total Power	**221.211**	**207.135**	**282.78**	**301.95**	**285.006**	**272.748**	**mW**

1 All voltage rails at nominal values: IV_{DD} = 1.5 V, EV_{DD} = 3.3 V, and SDV_{DD} = 1.8 V.

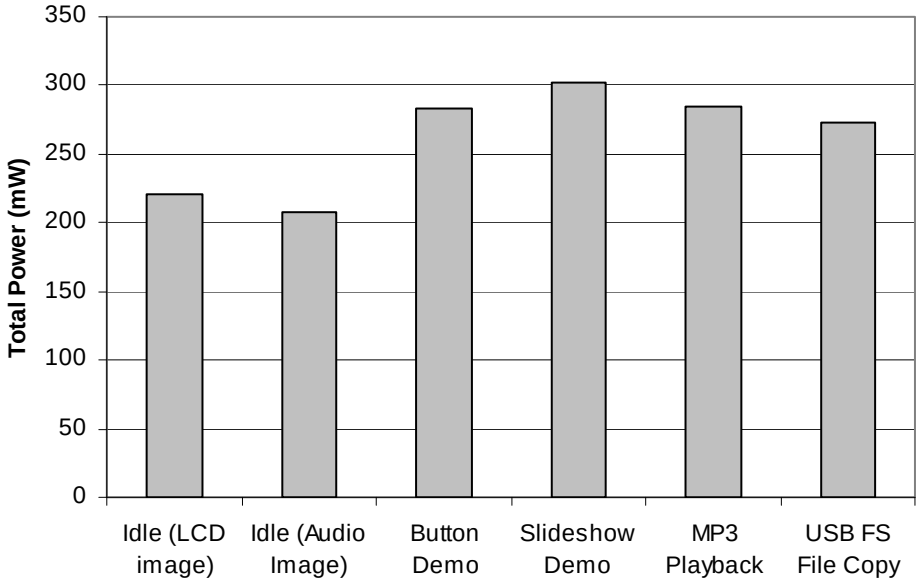


Figure 5. Power Consumption in Various Applications

All current consumption data is lab data measured on a single device using an evaluation board. Table 4 shows the typical power consumption in low-power modes. These current measurements are taken after executing a STOP instruction.

Table 4. Current Consumption in Low-Power Modes[1,2]

Mode	Voltage Supply	System Frequency				
		80MHz	64MHz	48MHz	32MHz	4MHz (LIMP mode)
RUN	IV_{DD} (mA)	75.1	62.7	49.2	36.6	3.5
	Power (mW)	112.65	94.05	73.80	54.90	5.25
WAIT	IV_{DD} (mA)	61.9	52.8	42.0	31.7	2.9
	Power (mW)	92.85	79.20	63.00	47.55	4.35

Table 4. Current Consumption in Low-Power Modes[1,2] (continued)

Mode	Voltage Supply	System Frequency				
		80MHz	64MHz	48MHz	32MHz	4MHz (LIMP mode)
DOZE	IV_{DD} (mA)	57.0	48.8	38.9	29.7	2.7
	Power (mW)	85.50	73.20	58.35	44.55	4.05
STOP 0	IV_{DD} (mA)	16.1	15.1	13.4	12.5	1.3
	Power (mW)	24.15	22.65	20.10	18.75	1.95
STOP 1	IV_{DD} (mA)	15.9	14.9	13.2	12.4	1.3
	Power (mW)	23.85	22.35	19.80	18.60	1.95
STOP 2	IV_{DD} (mA)	1.8	1.8	1.8	1.8	1.3
	Power (mW)	2.70	2.70	2.70	2.70	1.95
STOP 3	IV_{DD} (mA)	0.5	0.5	0.5	0.5	0.5
	Power (mW)	0.75	0.75	0.75	0.75	0.75

1 All values are measured on an M52277EVB with nominal core voltage(IV_{DD} = 1.5 V). Tests performed at room temperature. All peripheral clocks on prior to entering low-power mode

2 Refer to the Power Management chapter in the *MCF52277 Reference Manual* for more information on low-power modes.

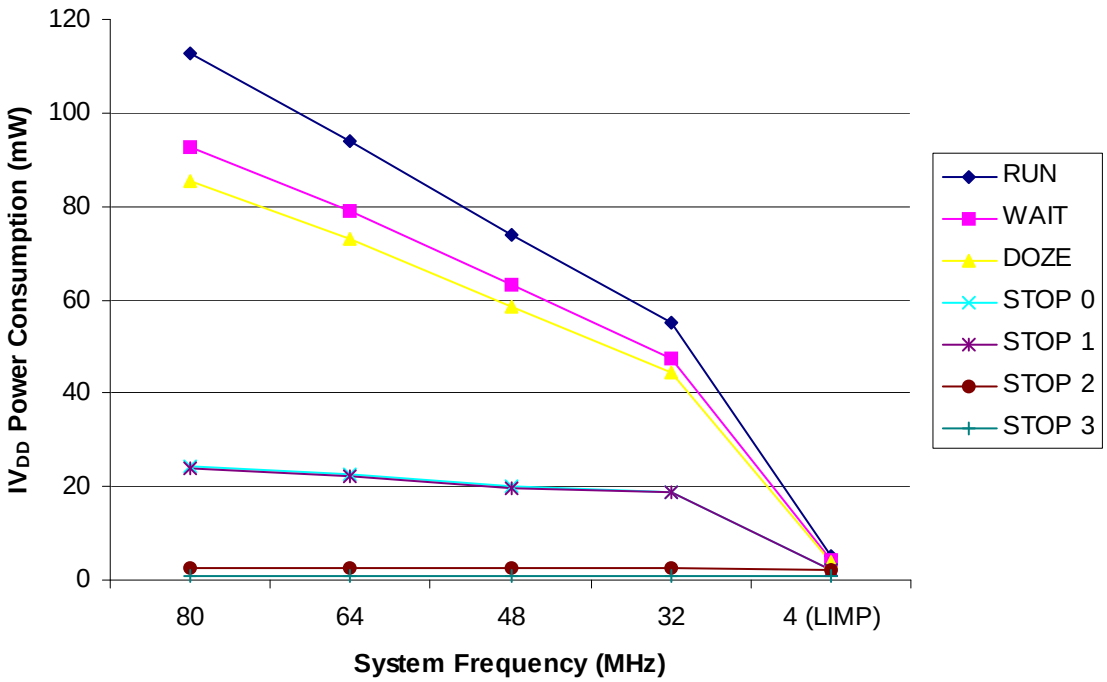


Figure 6. IV_{DD} Power Consumption in Low-Power Modes

Table 6. MCF5227*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF52274 176 LQFP	MCF52277 196 MAPBGA
FlexBus								
FB_A[23:22]	—	$\overline{\text{FB\_CS}}$[5:4]	—	—	O	SDVDD	143, 142	C11, D11
FB_A[21:16]	—	—	—	—	O	SDVDD	141–139, 137–135	A12, B12, C12, B13, A13, A14
FB_A[15:14]	—	SD_BA[1:0]	—	—	O	SDVDD	131, 130	B14, C13
FB_A[13:11]	—	SD_A[13:11]	—	—	O	SDVDD	129–127	C14, D12, D13
FB_A10	—	—	—		O	SDVDD	126	D14
FB_A[9:0]	—	SD_A[9:0]	—		O	SDVDD	125–116	E11–E14, F11–F13, G11, G12, H11
FB_D[31:16]	—	SD_D[31:16]	—		I/O	SDVDD	30–37, 49–56	J4, K1–K4, L1–L3, M3, N3, P3,M4, N4, P4, L5, M5
FB_D[15:0]	—	FB_D[31:16]	—		I/O	SDVDD	19–26, 60–67	G1–G4, H1–H4, M6, N6, P6, L7, M7, N7, P7, L8
FB_CLK	—	—	—		O	SDVDD	42	P1
$\overline{\text{FB\_BE/BWE}}$[3:0]	PBE[3:0]	SD_DQM[3:0]	—	—	O	SDVDD	29, 57, 27, 59	J3, N5, J1, L6
$\overline{\text{FB\_CS}}$[3:2]	PCS[3:2]	—	—	—	O	SDVDD	—	B11, A11
$\overline{\text{FB\_CS1}}$	PCS1	$\overline{\text{SD\_CS1}}$	—	—	O	SDVDD	144	D10
$\overline{\text{FB\_CS0}}$	PCS0	—	—	—	O	SDVDD	145	C10
$\overline{\text{FB\_OE}}$	PFBCTL3	—	—	—	O	SDVDD	69	N8
$\overline{\text{FB\_TA}}$	PFBCTL2	—	—	U	I	SDVDD	115	H12
FB_R/$\overline{\text{W}}$	PFBCTL1	—	—	—	O	SDVDD	68	M8
$\overline{\text{FB\_TS}}$	PFBCTL0	$\overline{\text{DACK0}}$	—	—	O	SDVDD	15	F4
SDRAM Controller								
SD_A10	—	—	—	—	O	SDVDD	46	L4
$\overline{\text{SD\_CAS}}$	—	—	—	—	O	SDVDD	47	N2
SD_CKE	—	—	—	—	O	SDVDD	17	F2
SD_CLK	—	—	—	—	O	SDVDD	40	M1
$\overline{\text{SD\_CLK}}$	—	—	—	—	O	SDVDD	41	N1
$\overline{\text{SD\_CS0}}$	—	—	—	—	O	SDVDD	18	F1
SD_DQS[3:2]	—	—	—	—	I/O	SDVDD	28, 58	J2, P5
$\overline{\text{SD\_RAS}}$	—	—	—	—	O	SDVDD	48	P2

Table 6. MCF5227*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF52274 176 LQFP	MCF52277 196 MAPBGA
Touchscreen Controller								
ADC_IN[7:0]	—	—	—	—	I	VDD_ADC	82–85, 87–90	P12, N12, P13, N13, P14, N14, M13, M14
ADC_REF	—	—	—	—	I	VDD_ADC	86	M12
I^2C								
I2C_SCL	PI2C1	CANTX	U2TXD	U	I/O	EVDD	168	C5
I2C_SDA	PI2C0	CANRX	U2RXD	U	I/O	EVDD	167	D5
DSPI[7]								
DSPI_PCS0/$\overline{SS}$	PDSPI3	$\overline{U2RTS}$	—	U	I/O	EVDD	152	B9
DSPI_SIN	PDSPI2	U2RXD	SBF_DI	[8]	I	EVDD	155	D8
DSPI_SOUT	PDSPI1	U2TXD	SBF_D0	—	O	EVDD	154	D9
DSPI_SCK	PDSPI0	$\overline{U2CTS}$	SBF_CK	—	I/O	EVDD	153	C9
UARTs								
$\overline{U1CTS}$	PUART7	SSI_BCLK	LCD_CLS	—	I	EVDD	156	C8
$\overline{U1RTS}$	PUART6	SSI_FS	LCD_PS	—	O	EVDD	157	B8
U1TXD	PUART5	SSI_TXD	—	—	O	EVDD	159	A7
U1RXD	PUART4	SSI_RXD	—	—	I	EVDD	158	A8
$\overline{U0CTS}$	PUART3	DT1OUT	USB_VBUS_EN	—	I	EVDD	97	K12
$\overline{U0RTS}$	PUART2	DT1IN	USB_VBUS_OC	—	O	EVDD	98	J12
U0TXD	PUART1	CANTX	—	—	O	EVDD	95	L12
U0RXD	PUART0	CANRX	—	—	I	EVDD	96	K13
DMA Timers								
DT3IN	PTIMER3	DT3OUT	SSI_MCLK	—	I	EVDD	163	D6
DT2IN/$\overline{SBF\_CS}$[7]	PTIMER2	DT2OUT	DSPI_PCS2	—	I	EVDD	164	C6
DT1IN	PTIMER1	DT1OUT	LCD_CONTRAST	—	I	EVDD	165	B6
DT0IN	PTIMER0	DT0OUT	LCD_REV	—	I	EVDD	166	A6
BDM/JTAG[9]								
PST[3:0]	—	—	—	—	O	EVDD	—	L9, M9, N9, P9
DDATA[3:0]	—	—	—	—	O	EVDD	—	L10, M10, N10, P10

Table 6. MCF5227*x* Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Pull-up (U)[1] Pull-down (D)	Direction[2]	Voltage Domain	MCF52274 176 LQFP	MCF52277 196 MAPBGA
ALLPST	—	—	—	—	O	EVDD	76	—
JTAG_EN	—	—	—	D	I	EVDD	79	K10
PSTCLK	—	TCLK	—	U	O	EVDD	74	P8
DSI	—	TDI	—	U	I	EVDD	78	M11
DSO	—	TDO	—	—	O	EVDD	81	L11
$\overline{\text{BKPT}}$	—	TMS	—	U	I	EVDD	80	N11
DSCLK	—	$\overline{\text{TRST}}$	—	U	I	EVDD	77	P11
Test								
TEST	—	—	—	D	I	EVDD	134	E10
Power Supplies								
IVDD	—	—	—	—	—	—	39, 75, 114, 138, 171	K5, F10, E5, J10
EVDD	—	—	—	—	—	—	12, 72, 73, 94, 111, 148, 176	E6, E7, F5, F6, G5, H9, J9, K8, K9
SD_VDD	—	—	—	—	—	—	14, 43, 44, 70, 113, 132, 146	E8, E9, F9, G9, H5, J5, J6, K6, K7
VDD_OSC	—	—	—	—	—	—	108	G13
VDD_PLL	—	—	—	—	—	—	104	H14
VDD_USB	—	—	—	—	—	—	151	B10
VDD_RTC	—	—	—	—	—	—	101	J13
VDD_ADC	—	—	—	—	—	—	91	L13
VSS	—	—	—	—	—	—	1, 13, 45, 71, 93, 112, 133, 147	F7, F8, G6–G8, H6–H8, J7, J8
VSS_OSC	—	—	—	—	—	—	107	H13
VSS_ADC	—	—	—	—	—	—	92	L14

1 Pull-ups are generally only enabled on pins with their primary function, except as noted.

2 Refers to pin's primary function.

3 Enabled only in oscillator bypass mode (internal crystal oscillator is disabled).

4 GPIO functionality is determined by the edge port module. The GPIO module is only responsible for assigning the alternate functions.

5 Pull-up when $\overline{\text{DREQ}}$ controls the pin.

6 The 176 LQFP device only supports a 12-bit LCD data bus.

7 DSPI or SBF signal functionality is controlled by $\overline{\text{RESET}}$. When asserted, these pins are configured for serial boot; when negated, the pins are configured for DSPI.

8 Pull-up when the serial boot facility (SBF) controls the pin.

4.3 Pinout—196 MAPBGA

The pinout for the MCF52277 package is shown below.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	LCD_D6	LCD_D5	LCD_D4	LCD_D2	LCD_ LSCLK	T0IN	U1TXD	U1RXD	USB_DM	USB_DP	FB_CS2	FB_A21	FB_A17	FB_A16	A
B	LCD_D8	LCD_D7	LCD_D3	LCD_D1	LCD_ ACD/OE	T1IN	IRQ_1	U1RTS	DSPI_ PCS0	VDD_ USB	FB_CS3	FB_A20	FB_A18	FB_A15	B
C	LCD_D13	LCD_D12	LCD_D10	LCD_D0	I2C_SCL	T2IN	IRQ_4	U1CTS	DSPI_ SCK	FB_CS0	FB_A23	FB_A19	FB_A14	FB_A13	C
D	LCD_D15	LCD_D14	LCD_D11	LCD_D9	I2C_SDA	T3IN	IRQ_7	DSPI_SIN	DSPI_ SOUT	FB_CS1	FB_A22	FB_A12	FB_A11	FB_A10	D
E	LCD_LP/ HSYNC	LCD_FLM/ VSYNC	LCD_D17	LCD_D16	IVDD	EVDD	EVDD	SDVDD	SDVDD	TEST	FB_A9	FB_A8	FB_A7	FB_A6	E
F	SD_CS0	SD_CKE	SD_WE	FB_TS	EVDD	EVDD	VSS	VSS	SDVDD	IVDD	FB_A5	FB_A4	FB_A3	EXTAL	F
G	FB_D15	FB_D14	FB_D13	FB_D12	EVDD	VSS	VSS	VSS	SDVDD	BOOT MOD1	FB_A2	FB_A1	VDD_ OSC	XTAL	G
H	FB_D11	FB_D10	FB_D9	FB_D8	SDVDD	VSS	VSS	VSS	EVDD	BOOT MOD0	FB_A0	FB_TA	VSS_ OSC	VDD_ PLL	H
J	FB_BE/ BWE1	SD_DQS3	FB_BE/ BWE3	FB_D31	SDVDD	SDVDD	VSS	VSS	EVDD	IVDD	RESET	U0RTS	VDD_ RTC	RTC_ EXTAL	J
K	FB_D30	FB_D29	FB_D28	FB_D27	IVDD	SDVDD	SDVDD	EVDD	EVDD	JTAG_EN	RSTOUT	U0CTS	U0RXD	RTC_ XTAL	K
L	FB_D26	FB_D25	FB_D24	SD_A10	FB_D17	FB_BE/ BWE0	FB_D4	FB_D0	PST3	DDATA3	TDO	U0TXD	VDD_ ADC	VSS_ ADC	L
M	SD_CLK	SD_ SDR_DQS	FB_D23	FB_D20	FB_D16	FB_D7	FB_D3	FB_R/W	PST2	DDATA2	TDI	ADC_ REF	ADC_IN1	ADC_IN0	M
N	SD_CLK	SD_CAS	FB_D22	FB_D19	FB_BE/ BWE2	FB_D6	FB_D2	FB_OE	PST1	DDATA1	TMS	ADC_IN6	ADC_IN4	ADC_IN2	N
P	FB_CLK	SD_RAS	FB_D21	FB_D18	SD_ DQS0	FB_D5	FB_D1	TCLK	PST0	DDATA0	TRST	ADC_IN7	ADC_IN5	ADC_IN3	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 8. MCF52277 Pinout (196 MAPBGA)

5 Electrical Characteristics

This document contains electrical specification tables and reference timing diagrams for the MCF5227x microprocessor. This section contains detailed information on DC/AC electrical characteristics and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle, however for production silicon these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

5.2 Thermal Characteristics

Table 8. Thermal Characteristics

Characteristic		Symbol	196 MAPBGA	176 LQFP	Unit
Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	38[1,2]	48[1,2]	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	34[1,2]	42[1,2]	°C/W
Junction to board		θ_{JB}	27[3]	37[3]	°C/W
Junction to case		θ_{JC}	17[4]	14[4]	°C/W
Junction to top of package		Ψ_{jt}	4[1,5]	3[1,5]	°C/W
Maximum operating junction temperature		T_j	105	105	°C

1 θ_{JA}, θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JmA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

2 Per JEDEC JESD51-6 with the board horizontal.

3 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

4 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

5 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad \textbf{Eqn. 1}$$

Where:

T_A = Ambient Temperature, °C
Q_{JMA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
P_D = $P_{INT} + P_{I/O}$
P_{INT} = $I_{DD} \times IV_{DD}$, Watts - Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = \frac{K}{(T_J + 273\,°C)} \quad \textbf{Eqn. 2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A \times 273°C) + Q_{JMA} \times P_D^2 \quad \textbf{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

Table 13. FlexBus AC Timing Specifications (continued)

Num	Characteristic	Symbol	Min	Max	Unit	Notes
FB4	Data Input Setup	t_{DVFBCH}	3.5	—	ns	
FB5	Data Input Hold	t_{DIFBCH}	0	—	ns	
FB6	Transfer Acknowledge ($\overline{TA}$) Input Setup	t_{CVFBCH}	4	—	ns	
FB7	Transfer Acknowledge ($\overline{TA}$) Input Hold	t_{CIFBCH}	0	—	ns	

1 Timing for chip selects only applies to the $\overline{FB\_CS}$[5:0] signals. Please see Section 5.7.2.2, "DDR SDRAM AC Timing Specifications," for SD_CS[3:0] timing.

2 The FlexBus supports programming an extension of the address hold. Please consult the device reference manual for more information.

NOTE

The processor drives the data lines during the first clock cycle of the transfer with the full 32-bit address. This may be ignored by standard connected devices using non-multiplexed address and data buses. However, some applications may find this feature beneficial.

The address and data busses are muxed between the FlexBus and SDRAM controller. At the end of the read and write bus cycles the address signals are indeterminate.

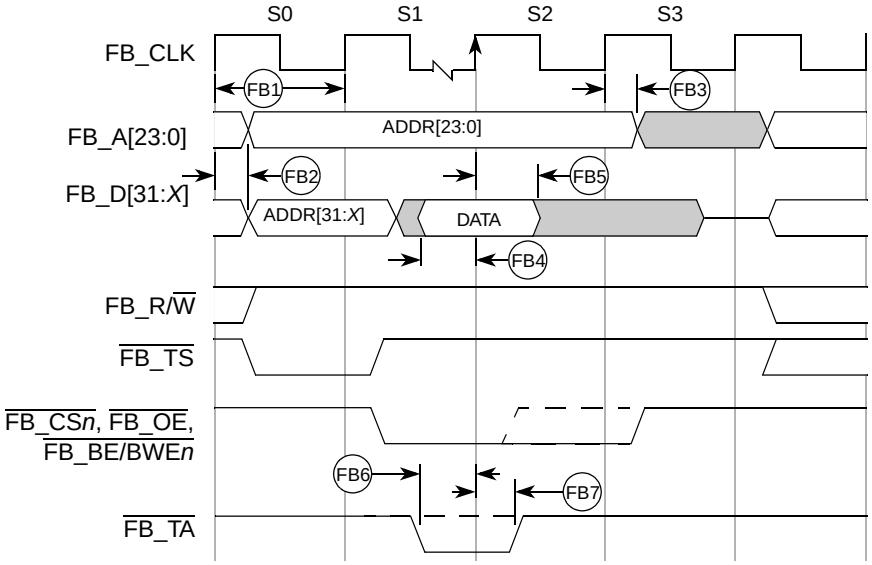


Figure 9. FlexBus Read Timing

Table 15. DDR Timing Specifications (continued)

Num	Characteristic	Symbol	Min	Max	Unit	Notes
DD8	Data and Data Mask Output Hold (DQS→DQ) Relative to DQS (DDR Write Mode)	t_{DQDMI}	1.0	—	ns	7
DD9	Input Data Skew Relative to DQS (Input Setup)	t_{DVDQ}	—	1	ns	8
DD10	Input Data Hold Relative to DQS	t_{DIDQ}	0.25 × SD_CLK + 0.5ns	—	ns	9
DD11	DQS falling edge from SDCLK rising (output hold time)	$t_{DQLSDCH}$	0.5	—	ns	

1 The frequency of operation is either 2x or 4x the FB_CLK frequency of operation. FlexBus and SDRAM clock operate at the same frequency as the internal bus clock.

2 SD_CLK is one SDRAM clock in ns.

3 Pulse-width high plus pulse-width low cannot exceed minimum or maximum clock period.

4 Command output valid should be one-half the memory bus clock (SD_CLK) plus some minor adjustments for process, temperature, and voltage variations.

5 This specification relates to the required input setup time of today's DDR memories. The device's output setup should be larger than the input setup of the DDR memories. If it is not larger, then the input setup on the memory will be in violation. MEM_DATA[31:24] is relative to MEM_DQS[3], MEM_DATA[23:16] is relative to MEM_DQS[2], MEM_DATA[15:8] is relative to MEM_DQS[1], and MEM_DATA[7:0] is relative MEM_DQS[0].

6 The first data beat will be valid before the first rising edge of DQS and after the DQS write preamble. The remaining data beats will be valid for each subsequent DQS edge.

7 This specification relates to the required hold time of today's DDR memories. MEM_DATA[31:24] is relative to MEM_DQS[3], MEM_DATA[23:16] is relative to MEM_DQS[2], MEM_DATA[15:8] is relative to MEM_DQS[1], and MEM_DATA[7:0] is relative MEM_DQS[0].

8 Data input skew is derived from each DQS clock edge. It begins with a DQS transition and ends when the last data line becomes valid. This input skew must include DDR memory output skew and system-level board skew (due to routing or other factors).

9 Data input hold is derived from each DQS clock edge. It begins with a DQS transition and ends when the first data line becomes invalid.

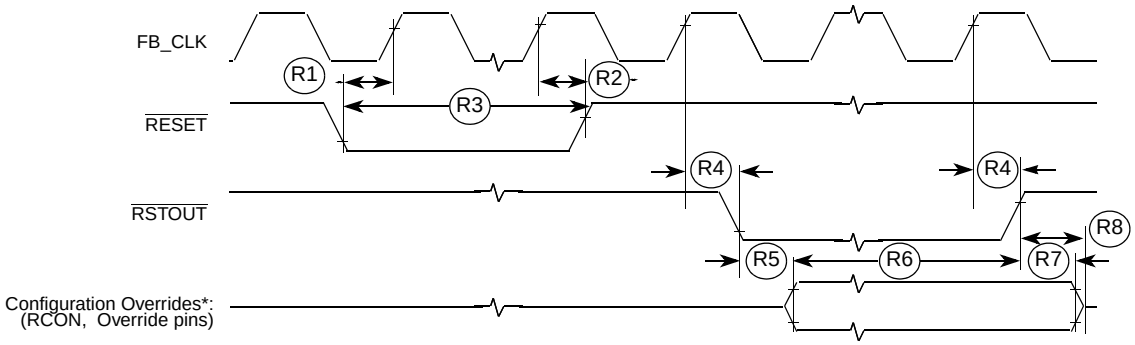


Figure 17. RESET and Configuration Override Timing

NOTE

Refer to the CCM chapter of the *MCF52277 Reference Manual* for more information.

5.10 LCD Controller Timing Specifications

This sections lists the timing specifications for the LCD Controller.

Table 19. LCD_LSCLK Timing

Num	Characteristic	Min	Max	Unit
T1	LCD_LSCLK Period	25	2000	ns
T2	Pixel data setup time	11	—	ns
T3	Pixel data up time	11	—	ns

Note: The pixel clock is equal to LCD_LSCLK / (PCD + 1). When it is in CSTN, TFT, or monochrome mode with bus width = 1, LCD_LSCLK is equal to the pixel clock. When it is in monochrome with other bus width settings, LCD_LSCLK is equal to the pixel clock divided by bus width. The polarity of LCD_LSCLK and LCD_D signals can also be programmed.

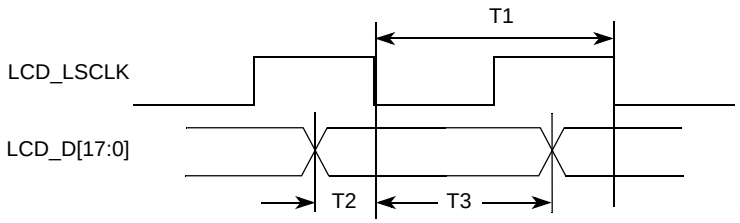


Figure 18. LCD_LSCLK to LCD_D[17:0] timing diagram

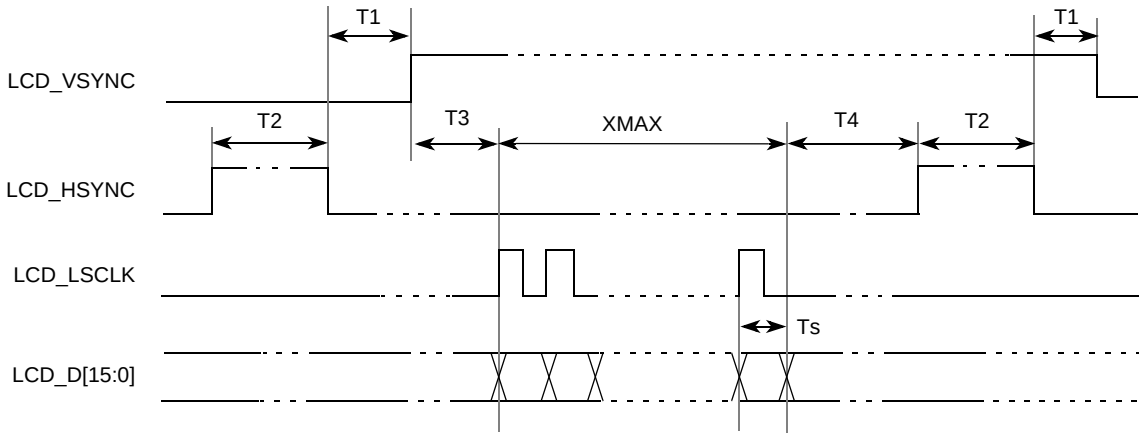


Figure 21. Non-TFT Mode Panel Timing

Table 22. Non-TFT Mode Panel Timing

Num	Characteristic	Min	Value	Unit
T1	LCD_HSYNC to LCD_VSYNC delay	2	HWAIT2 + 2	Tpix
T2	LCD_HSYNC pulse width	1	HWIDTH + 1	Tpix
T3	LCD_VSYNC to LCD_LSCLK	—	0 ≤ T3 ≤ Ts	—
T4	LCD_LSCLK to LCD_HSYNC	1	HWAIT1 + 1	Tpix

Note: Ts is the LCD_LSCLK period while Tpix is the pixel clock period. LCD_VSYNC, LCD_HSYNC, and LCD_LSCLK can be programmed as active high or active low. In Figure 21, all these 3 signals are active high. When it is in CSTN mode or monochrome mode with bus width = 1, T3 = Tpix = Ts. When it is in monochrome mode with bus width = 2, 4 and 8, T3 = 1, 2 and 4 Tpix respectively.

5.11 USB On-The-Go Specifications

The MCF5227x device is compliant with industry standard USB 2.0 specification.

Table 23. USB On-Chip Transceiver DC Characteristics

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Input High	Driven	V_{IH}	2.0	—	—	V
Input Low		V_{IL}	—	—	0.8	V
Input Differential	(DP – DM)	V_{ID}	200	—	00	mV
Differential Common Mode Range		V_{CM}	0.8	—	2.5	V
Single Ended Receive Threshold		V_{SETHR}	0.8	—	2.0	V
Single Ended Receive Hysteresis		V_{SEHYS}	—	400	—	mV
Output High	Driven	V_{OH}	0.0	—	300	mV
Output Low	Driven	V_{OL}	2.8	—	2.0	V
Differential Output Crossover	DP = DM	V_{CRS}	1.3	—	2.0	V

Table 26. SSI Timing—Master Modes[1] (continued)

Num	Characteristic	Symbol	Min	Max	Unit	Notes
S5	SSI_BCLK to SSI_FS output valid		—	10	ns	
S6	SSI_BCLK to SSI_FS output invalid		0	—	ns	
S7	SSI_BCLK to SSI_TXD valid		—	10	ns	
S8	SSI_BCLK to SSI_TXD invalid / high impedence		0	—	ns	
S9	SSI_RXD / SSI_FS input setup before SSI_BCLK		10	—	ns	
S10	SSI_RXD / SSI_FS input hold after SSI_BCLK		0	—	ns	

1 All timings specified with a capactive load of 25pF.

2 SSI_MCLK can be generated from SSI_CLKIN or a divided version of the internal system clock (SYSCLK).

3 SSI_BCLK can be derived from SSI_CLKIN or a divided version of SYSCLK. If the SYSCLK is used, the minimum divider is 6. If the SSI_CLKIN input is used, the programmable dividers must be set to ensure that SSI_BCLK does not exceed 4 x f_{SYS}.

Table 27. SSI Timing—Slave Modes[1]

Num	Characteristic	Symbol	Min	Max	Unit	Notes
S11	SSI_BCLK cycle time	t_{BCLK}	$4 \times 1/f_{SYS}$	—	ns	
S12	SSI_BCLK pulse width high / low		45%	55%	t_{BCLK}	
S13	SSI_FS input setup before SSI_BCLK		10	—	ns	
S14	SSI_FS input hold after SSI_BCLK		2	—	ns	
S15	SSI_BCLK to SSI_TXD / SSI_FS output valid		—	10	ns	
S16	SSI_BCLK to SSI_TXD / SSI_FS output invalid / high impedence		0	—	ns	
S17	SSI_RXD setup before SSI_BCLK		10	—	ns	
S18	SSI_RXD hold after SSI_BCLK		2	—	ns	

1 All timings specified with a capactive load of 25 pF.

5.14 DMA Timer Timing Specifications

Table 30 lists timer module AC timings.

Table 30. Timer Module AC Timing Specifications

Num	Characteristic	Min	Max	Unit
T1	DT0IN / DT1IN / DT2IN / DT3IN cycle time	3	—	t_{CYC}
T2	DT0IN / DT1IN / DT2IN / DT3IN pulse width	1	—	t_{CYC}

5.15 DSPI Timing Specifications

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with both master and slave operations. Many of the transfer attributes are programmable. Table 31 provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the *MCF52277 Reference Manual* for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 31. DSPI Module AC Timing Specifications[1]

Num	Characteristic	Symbol	Min	Max	Unit	Notes
DS1	DSPI_SCK Cycle Time	t_{SCK}	4 x $1/f_{SYS}$	—	ns	[2]
DS2	DSPI_SCK Duty Cycle	—	(tsck ÷ 2) – 2.0	(tsck ÷ 2) + 2.0	ns	
Master Mode						
DS3	DSPI_PCS*n* to DSPI_SCK delay	t_{CSC}	$(2 \times 1/f_{SYS}) - 2.0$	—	ns	[3]
DS4	DSPI_SCK to DSPI_PCS*n* delay	t_{ASC}	$(2 \times 1/f_{SYS}) - 3.0$	—	ns	[4]
DS5	DSPI_SCK to DSPI_SOUT valid	—	—	5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	—	–5	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	—	9	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	—	0	—	ns	
Slave Mode						
DS9	DSPI_SCK to DSPI_SOUT valid	—	—	4	ns	
DS10	DSPI_SCK to DSPI_SOUT invalid	—	0	—	ns	
DS11	DSPI_SIN to DSPI_SCK input setup	—	2	—	ns	
DS12	DSPI_SCK to DSPI_SIN input hold	—	7	—	ns	
DS13	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	—	20	ns	
DS14	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	—	18	ns	

1 Timings shown are for DMCR[MTFE] = 0 (classic SPI) and DCTAR*n*[CPHA] = 0. Data is sampled on the DSPI_SIN pin on the odd-numbered DSPI_SCK edges and driven on the DSPI_SOUT pin on even-numbered DSPI edges.

2 When in master mode, the baud rate is programmable in DCTAR*n*[PBR] and DCTAR*n*[BR].

3 The DSPI_PCS*n* to DSPI_SCK delay is programmable in DCTAR*n*[PCSSCK] and DCTAR*n*[CSSCK].

4 The DSPI_SCK to DSPI_PCS*n* delay is programmable in DCTAR*n*[PASC] and DCTAR*n*[ASC].

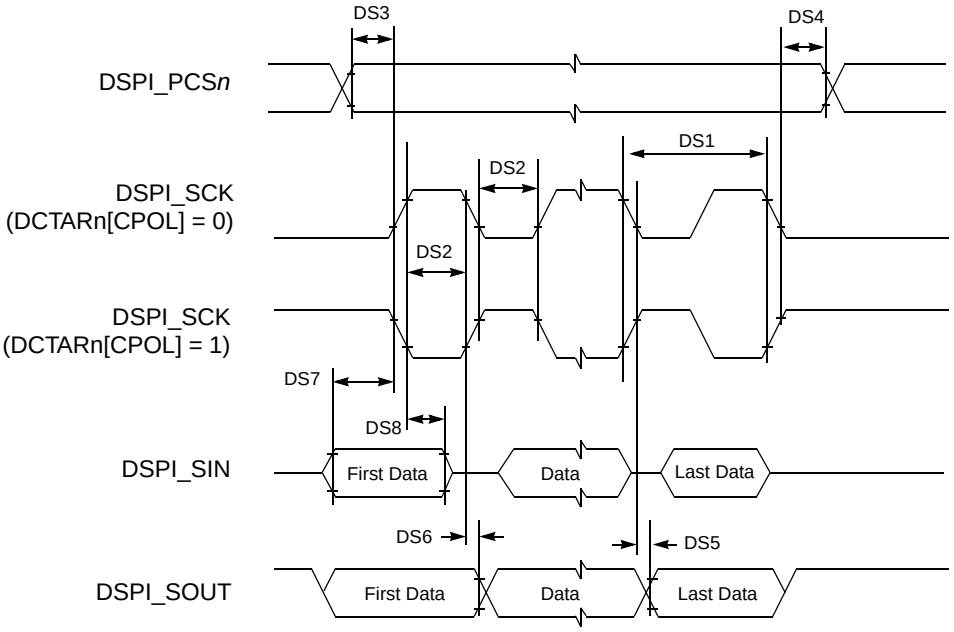


Figure 25. DSPI Classic SPI Timing—Master Mode

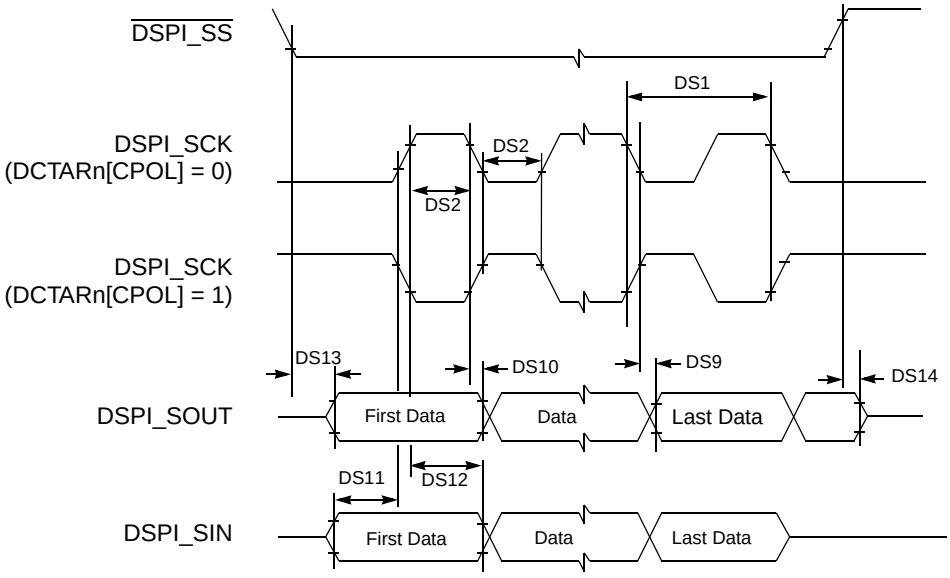


Figure 26. DSPI Classic SPI Timing—Slave Mode

5.16 SBF Timing Specifications

The Serial Boot Facility (SBF) provides a means to read configuration information and system boot code from a broad array of SPI-compatible EEPROMs, flashes, FRAMs, nVSRAMs, etc. Table 32 provides the AC timing specifications for the SBF.

Table 33. JTAG and Boundary Scan Timing (continued)

Num	Characteristic[1]	Symbol	Min	Max	Unit
J9	TMS, TDI Input Data Setup Time to TCLK Rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input Data Hold Time after TCLK Rise	t_{TAPBHT}	10	—	ns
J11	TCLK Low to TDO Data Valid	t_{TDODV}	0	26	ns
J12	TCLK Low to TDO High Z	t_{TDODZ}	0	8	ns
J13	$\overline{\text{TRST}}$ Assert Time	t_{TRSTAT}	100	—	ns
J14	$\overline{\text{TRST}}$ Setup Time (Negation) to TCLK High	t_{TRSTST}	10	—	ns

1 JTAG_EN is expected to be a static signal. Hence, specific timing is not associated with it.

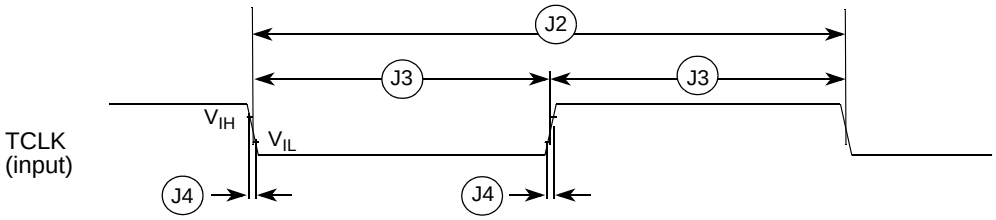


Figure 28. Test Clock Input Timing

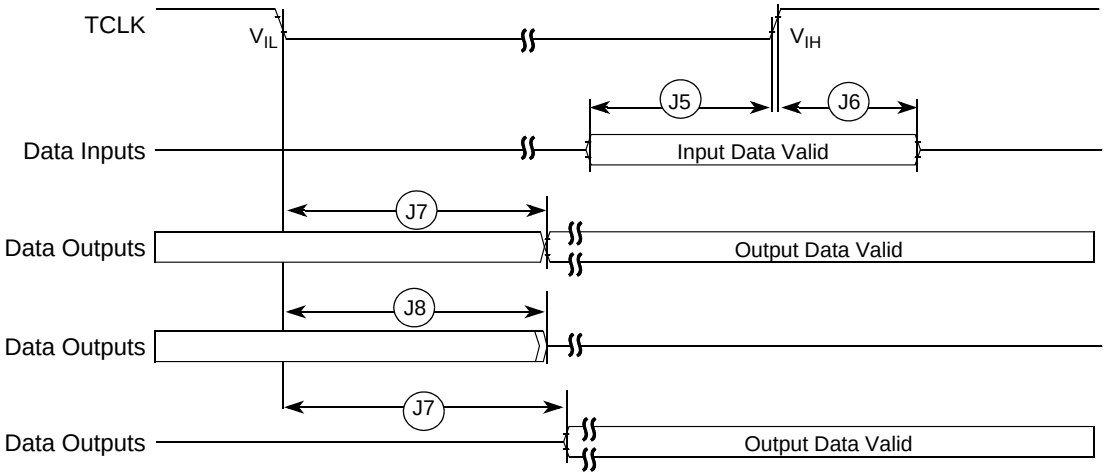


Figure 29. Boundary Scan (JTAG) Timing

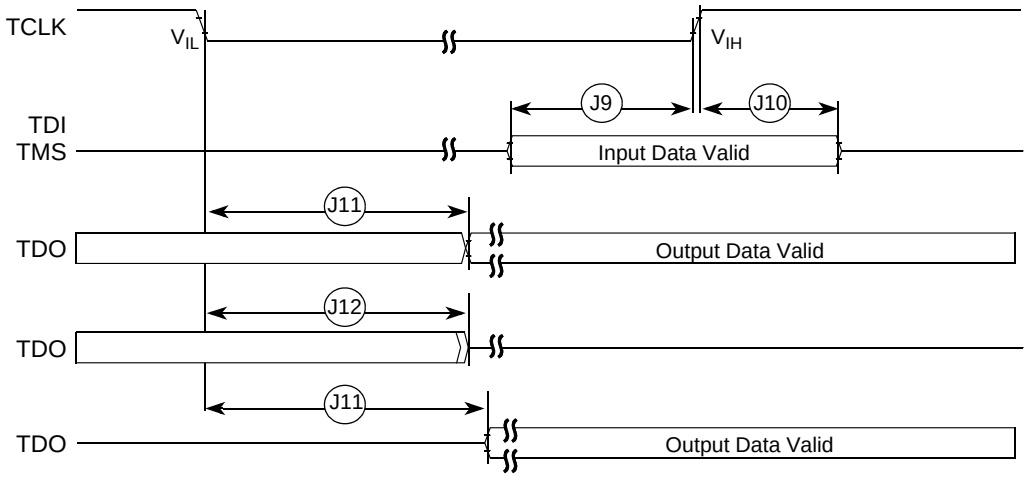


Figure 30. Test Access Port Timing

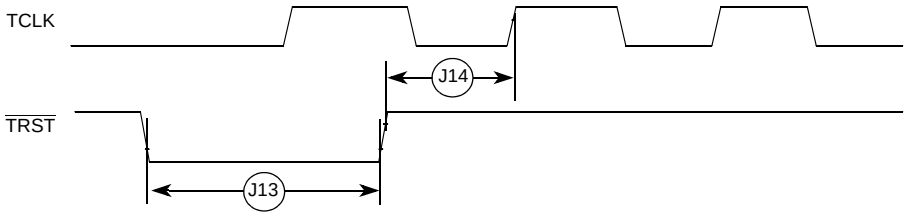


Figure 31. TRST Timing

5.18 Debug AC Timing Specifications

Table 34 lists specifications for the debug AC timing parameters shown in Figure 32.

Table 34. Debug AC Timing Specification

Num	Characteristic	Min	Max	Units
D0	PSTCLK cycle time	1	1	$1/f_{SYS}$
D1	PSTCLK rising to PSTDDATA valid	—	3.0	ns
D2	PSTCLK rising to PSTDDATA invalid	1.5	—	ns
D3	DSI-to-DSCLK setup	1	—	PSTCLK
D4[1]	DSCLK-to-DSO hold	4	—	PSTCLK
D5	DSCLK cycle time	5	—	PSTCLK
D6	BKPT assertion time	1	—	PSTCLK

1 DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of PSTCLK.

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Document Number: MCF52277
Rev. 8
09/2009

freescale™
semiconductor