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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	F <sup>2</sup> MC-16FX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I <sup>2</sup> C, LINbus, SCI, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	99
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/infineon-technologies/mb96f6c6rbpmc-gse1">https://www.e-xfl.com/product-detail/infineon-technologies/mb96f6c6rbpmc-gse1</a>

- Programmable loop-back mode for self-test operation

## USART

- Full duplex USARTs (SCI/LIN)
- Wide range of baud rate settings using a dedicated reload timer
- Special synchronous options for adapting to different synchronous serial protocols
- LIN functionality working either as master or slave LIN device
- Extended support for LIN-Protocol to reduce interrupt load

## I<sup>2</sup>C

- Up to 400kbps
- Master and Slave functionality, 7-bit and 10-bit addressing

## A/D converter

- SAR-type
- 8/10-bit resolution
- Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger, reload timers and PPGs
- Range Comparator Function
- Scan Disable Function
- ADC Pulse Detection Function

## Source Clock Timers

Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer)

## Hardware Watchdog Timer

- Hardware watchdog timer is active after reset
- Window function of Watchdog Timer is used to select the lower window limit of the watchdog interval

## Reload Timers

- 16-bit wide
- Prescaler with  $1/2^1$ ,  $1/2^2$ ,  $1/2^3$ ,  $1/2^4$ ,  $1/2^5$ ,  $1/2^6$  of peripheral clock frequency
- Event count function

## Free-Running Timers

- Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4)
- Prescaler with  $1$ ,  $1/2^1$ ,  $1/2^2$ ,  $1/2^3$ ,  $1/2^4$ ,  $1/2^5$ ,  $1/2^6$ ,  $1/2^7$ ,  $1/2^8$  of peripheral clock frequency

## Input Capture Units

- 16-bit wide

- Signals an interrupt upon external event
- Rising edge, Falling edge or Both (rising & falling) edges sensitive

## Output Compare Units

- 16-bit wide
- Signals an interrupt when a match with Free-running Timer occurs
- A pair of compare registers can be used to generate an output signal

## Programmable Pulse Generator

- 16-bit down counter, cycle and duty setting registers
- Can be used as  $2 \times 8$ -bit PPG
- Interrupt at trigger, counter borrow and/or duty match
- PWM operation and one-shot operation
- Internal prescaler allows  $1$ ,  $1/4$ ,  $1/16$ ,  $1/64$  of peripheral clock as counter clock or of selected Reload timer underflow as clock input
- Can be triggered by software or reload timer
- Can trigger ADC conversion
- Timing point capture
- Start delay

## Quadrature Position/Revolution Counter (QPRC)

- Up/down count mode, Phase difference count mode, Count mode with direction
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers with interrupt
- Detection edge of the three external event input pins AIN, BIN and ZIN is configurable

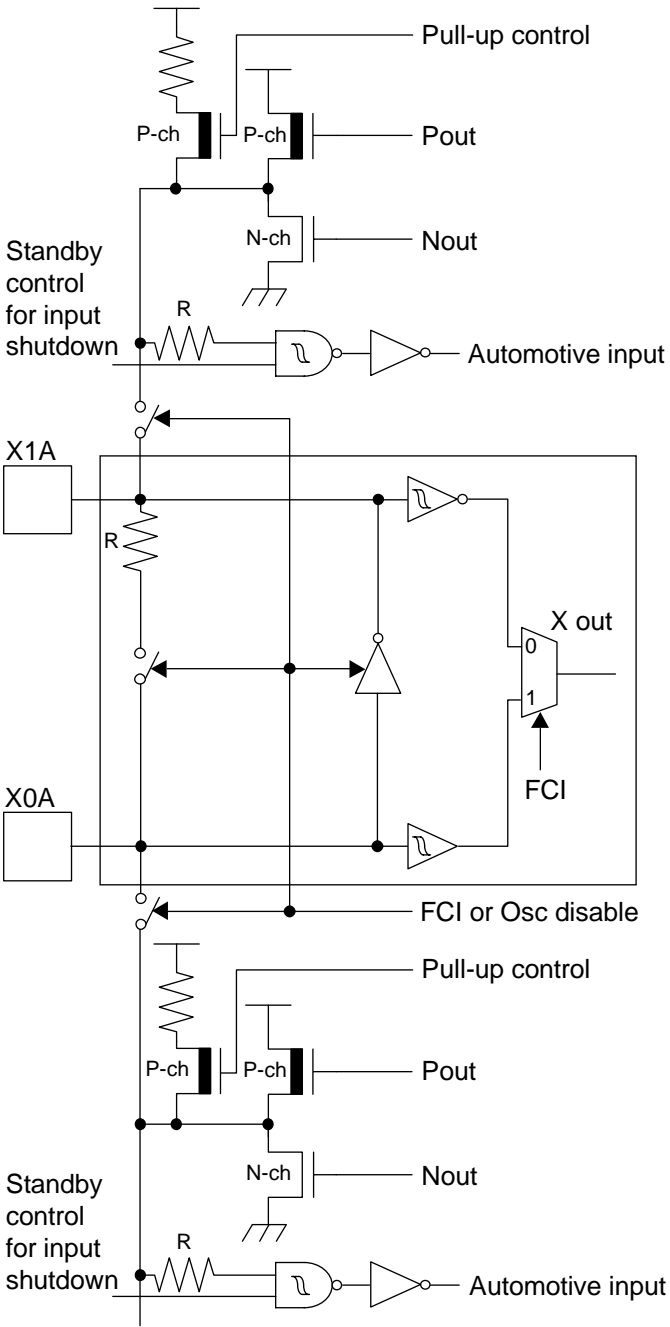
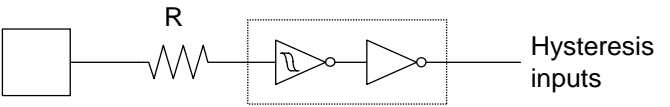
## LCD Controller

- LCD controller with up to  $4\text{COM} \times 44\text{SEG}$
- Internal or external voltage generation
- Duty cycle: Selectable from options:  $1/2$ ,  $1/3$  and  $1/4$
- Fixed  $1/3$  bias
- Programmable frame period
- Clock source selectable from four options (main clock, peripheral clock, subclock or RC oscillator clock)
- Internal divider resistors or external divider resistors
- On-chip data memory for display
- LCD display can be operated in Timer Mode
- Blank display: selectable

## 1. Product Lineup

Features		MB966C0	Remark
Product Type		Flash Memory Product	
Subclock		Subclock can be set by software	
Dual Operation Flash Memory	RAM	-	
128.5KB + 32KB	8KB	MB96F6C5R, MB96F6C5A	Product Options R: MCU with CAN A: MCU without CAN
256.5KB + 32KB	16KB	MB96F6C6R	
Package		LQFP-120 FPT-120P-M21	
DMA		4ch	
USART		5ch	LIN-USART 0 to 2/4/5
	with automatic LIN-Header transmission/reception	2ch	LIN-USART 0/1
	with 16 byte RX- and TX-FIFO		
I <sup>2</sup> C		1ch	I <sup>2</sup> C 0
8/10-bit A/D Converter		32ch	AN 0 to 31
	with Data Buffer	No	
	with Range Comparator	Yes	
	with Scan Disable	Yes	
	with ADC Pulse Detection	Yes	
16-bit Reload Timer (RLT)		5ch	RLT 0 to 3/6
16-bit Free-Running Timer (FRT)		2ch	FRT 0/1
16-bit Input Capture Unit (ICU)		8ch (5 channels for LIN-USART)	ICU 0 to 7 (ICU 0/1/4 to 6 for LIN-USART)
16-bit Output Compare Unit (OCU)		4ch	OCU 0 to 3
8/16-bit Programmable Pulse Generator (PPG)		12ch (16-bit) / 24ch (8-bit)	PPG 0 to 7/12 to 15
	with Timing point capture	Yes	
	with Start delay	Yes	
	with Ramp	No	
Quadrature Position/Revolution Counter (QPRC)		2ch	QPRC 0/1
CAN Interface		1ch	CAN 0 32 Message Buffers
External Interrupts (INT)		16ch	INT 0 to 15
Non-Maskable Interrupt (NMI)		1ch	
Sound Generator (SG)		2ch	SG 0/1
LCD Controller		4COM × 44SEG	COM 0 to 3 SEG 0 to 4/7 to 45
Real Time Clock (RTC)		1ch	
I/O Ports		97 (Dual clock mode) 99 (Single clock mode)	
Clock Calibration Unit (CAL)		1ch	
Clock Output Function		2ch	
Low Voltage Detection Function		Yes	Low voltage detection function can be disabled by software
Hardware Watchdog Timer		Yes	
On-chip RC-oscillator		Yes	
On-chip Debugger		Yes	

Note: All signals of the peripheral function in each product cannot be allocated by limiting the pins of package.  
 It is necessary to use the port relocate function of the general I/O port according to your function use.

Type	Circuit	Remarks
B	 <p>The diagram shows two identical circuit blocks. Each block features a pull-up resistor connected to a 'Pull-up control' line. Below this is a P-channel MOSFET labeled 'Pout' and an N-channel MOSFET labeled 'Nout'. A 'Standby control for input shutdown' line is connected to a resistor 'R' and an 'Automotive input' through an inverter. The input signal is also connected to a multiplexer 'X out' via a resistor 'R'. The multiplexer has two inputs, 'X1A' and 'X0A', and is controlled by 'FCI' or 'Osc disable'. The output of the multiplexer is 'X out'.</p>	<p>Low-speed oscillation circuit shared with GPIO functionality:</p> <ul style="list-style-type: none"> <li>■ Feedback resistor = approx. 5.0MΩ</li> <li>■ GPIO functionality selectable (CMOS level output (<math>I_{OL} = 4\text{mA}</math>, <math>I_{OH} = -4\text{mA}</math>), Automotive input with input shutdown function and programmable pull-up resistor)</li> </ul>
C	 <p>The diagram shows a single circuit block for a CMOS hysteresis input pin. It consists of a resistor 'R' connected to a hysteresis input block, which is represented by a dashed box containing an inverter and a buffer. The output of the hysteresis input block is labeled 'Hysteresis inputs'.</p>	<p>CMOS hysteresis input pin</p>

## 8. RAMSTART Addresses

Devices	Bank 0 RAM size	RAMSTART0
MB96F6C5	8KB	00:6200 <sub>H</sub>
MB96F6C6	16KB	00:4200 <sub>H</sub>

## 10. Serial Programming Communication Interface

USART pins for Flash serial programming (MD = 0, DEBUG I/F = 0, Serial Communication mode)

MB966C0		
Pin Number	USART Number	Normal Function
8	USART0	SIN0
9		SOT0
10		SCK0
3	USART1	SIN1
4		SOT1
5		SCK1
56	USART2	SIN2
57		SOT2
58		SCK2
101	USART4	SIN4
102		SOT4
103		SCK4

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
40	35C <sub>H</sub>	PPG2	Yes	40	Programmable Pulse Generator 2
41	358 <sub>H</sub>	PPG3	Yes	41	Programmable Pulse Generator 3
42	354 <sub>H</sub>	PPG4	Yes	42	Programmable Pulse Generator 4
43	350 <sub>H</sub>	PPG5	Yes	43	Programmable Pulse Generator 5
44	34C <sub>H</sub>	PPG6	Yes	44	Programmable Pulse Generator 6
45	348 <sub>H</sub>	PPG7	Yes	45	Programmable Pulse Generator 7
46	344 <sub>H</sub>	-	-	46	Reserved
47	340 <sub>H</sub>	-	-	47	Reserved
48	33C <sub>H</sub>	-	-	48	Reserved
49	338 <sub>H</sub>	-	-	49	Reserved
50	334 <sub>H</sub>	PPG12	Yes	50	Programmable Pulse Generator 12
51	330 <sub>H</sub>	PPG13	Yes	51	Programmable Pulse Generator 13
52	32C <sub>H</sub>	PPG14	Yes	52	Programmable Pulse Generator 14
53	328 <sub>H</sub>	PPG15	Yes	53	Programmable Pulse Generator 15
54	324 <sub>H</sub>	-	-	54	Reserved
55	320 <sub>H</sub>	-	-	55	Reserved
56	31C <sub>H</sub>	-	-	56	Reserved
57	318 <sub>H</sub>	-	-	57	Reserved
58	314 <sub>H</sub>	RLT0	Yes	58	Reload Timer 0
59	310 <sub>H</sub>	RLT1	Yes	59	Reload Timer 1
60	30C <sub>H</sub>	RLT2	Yes	60	Reload Timer 2
61	308 <sub>H</sub>	RLT3	Yes	61	Reload Timer 3
62	304 <sub>H</sub>	-	-	62	Reserved
63	300 <sub>H</sub>	-	-	63	Reserved
64	2FC <sub>H</sub>	RLT6	Yes	64	Reload Timer 6
65	2F8 <sub>H</sub>	ICU0	Yes	65	Input Capture Unit 0
66	2F4 <sub>H</sub>	ICU1	Yes	66	Input Capture Unit 1
67	2F0 <sub>H</sub>	ICU2	Yes	67	Input Capture Unit 2
68	2EC <sub>H</sub>	ICU3	Yes	68	Input Capture Unit 3
69	2E8 <sub>H</sub>	ICU4	Yes	69	Input Capture Unit 4
70	2E4 <sub>H</sub>	ICU5	Yes	70	Input Capture Unit 5
71	2E0 <sub>H</sub>	ICU6	Yes	71	Input Capture Unit 6
72	2DC <sub>H</sub>	ICU7	Yes	72	Input Capture Unit 7
73	2D8 <sub>H</sub>	-	-	73	Reserved
74	2D4 <sub>H</sub>	-	-	74	Reserved
75	2D0 <sub>H</sub>	-	-	75	Reserved
76	2CC <sub>H</sub>	-	-	76	Reserved
77	2C8 <sub>H</sub>	OCU0	Yes	77	Output Compare Unit 0
78	2C4 <sub>H</sub>	OCU1	Yes	78	Output Compare Unit 1
79	2C0 <sub>H</sub>	OCU2	Yes	79	Output Compare Unit 2
80	2BC <sub>H</sub>	OCU3	Yes	80	Output Compare Unit 3

#### ■ Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

- (1) Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
- (2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
- (3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).  
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
- (4) Ground all fixtures and instruments, or protect with anti-static measures.
- (5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

### 12.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

- (1) Humidity  
Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.
- (2) Discharge of Static Electricity  
When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.
- (3) Corrosive Gases, Dust, or Oil  
Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.
- (4) Radiation, Including Cosmic Radiation  
Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.
- (5) Smoke, Flame  
**CAUTION:** Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

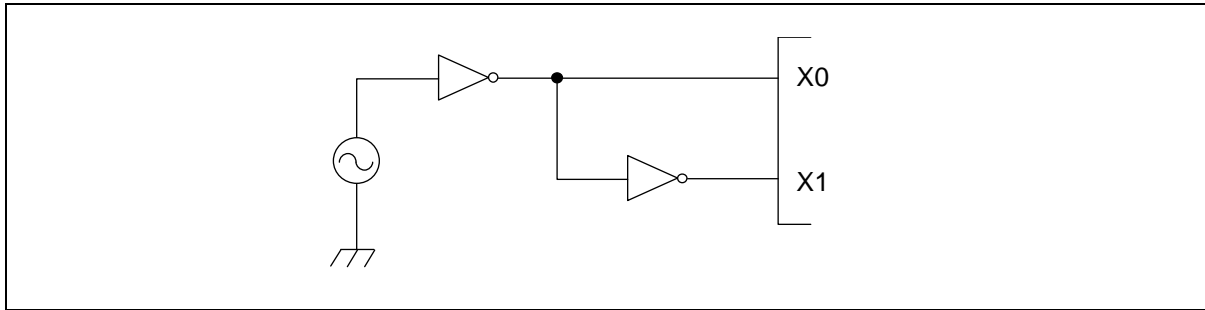


## (2) Single phase external clock for Sub oscillator

When using a single phase external clock for the Sub oscillator, "External clock mode" must be selected and X0A/P04\_0 pin must be driven. X1A/P04\_1 pin can be configured as GPIO.

## (3) Opposite phase external clock

When using an opposite phase external clock, X1 (X1A) pins must be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins. Supply level on X0 and X1 pins must be 1.8V.



## 4. Notes on PLL clock mode operation

If the microcontroller is operated with PLL clock mode and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

## 5. Power supply pins (Vcc/Vss)

It is required that all V<sub>CC</sub>-level as well as all V<sub>SS</sub>-level power supply pins are at the same potential. If there is more than one V<sub>CC</sub> or V<sub>SS</sub> level, the device may operate incorrectly or be damaged even within the guaranteed operating range.

V<sub>CC</sub> and V<sub>SS</sub> pins must be connected to the device from the power supply with lowest possible impedance.

The smoothing capacitor at V<sub>CC</sub> pin must use the one of a capacity value that is larger than C<sub>s</sub>.

Besides this, as a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1μF between V<sub>CC</sub> and V<sub>SS</sub> pins as close as possible to V<sub>CC</sub> and V<sub>SS</sub> pins.

## 6. Crystal oscillator and ceramic resonator circuit

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

## 7. Turn on sequence of power supply to A/D converter and analog inputs

It is required to turn the A/D converter power supply (AV<sub>CC</sub>, AVR<sub>H</sub>, AVR<sub>L</sub>) and analog inputs (AN<sub>n</sub>) on after turning the digital power supply (V<sub>CC</sub>) on.

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, AVR<sub>H</sub> must not exceed AV<sub>CC</sub>. Input voltage for ports shared with analog input ports also must not exceed AV<sub>CC</sub> (turning the analog and digital power supplies simultaneously on or off is acceptable).

## 8. Pin handling when not using the A/D converter

If the A/D converter is not used, the power supply pins for A/D converter should be connected such as AV<sub>CC</sub> = V<sub>CC</sub>, AV<sub>SS</sub> = AVR<sub>H</sub> = AVR<sub>L</sub> = V<sub>SS</sub>.

## 14. Electrical Characteristics

### 14.1 Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit	Remarks
			Min	Max		
Power supply voltage* <sup>1</sup>	V <sub>CC</sub>	-	V <sub>SS</sub> - 0.3	V <sub>SS</sub> + 6.0	V	
Analog power supply voltage* <sup>1</sup>	AV <sub>CC</sub>	-	V <sub>SS</sub> - 0.3	V <sub>SS</sub> + 6.0	V	V <sub>CC</sub> = AV <sub>CC</sub> * <sup>2</sup>
Analog reference voltage* <sup>1</sup>	AVRH, AVRL	-	V <sub>SS</sub> - 0.3	V <sub>SS</sub> + 6.0	V	AV <sub>CC</sub> ≥ AVRH, AV <sub>CC</sub> ≥ AVRL, AVRH > AVRL, AVRL ≥ AV <sub>SS</sub>
LCD power supply voltage* <sup>1</sup>	V0 to V3	-	V <sub>SS</sub> - 0.3	V <sub>SS</sub> + 6.0	V	V0 to V3 must not exceed V <sub>CC</sub>
Input voltage* <sup>1</sup>	V <sub>I</sub>	-	V <sub>SS</sub> - 0.3	V <sub>SS</sub> + 6.0	V	V <sub>I</sub> ≤ V <sub>CC</sub> + 0.3V* <sup>3</sup>
Output voltage* <sup>1</sup>	V <sub>O</sub>	-	V <sub>SS</sub> - 0.3	V <sub>SS</sub> + 6.0	V	V <sub>O</sub> ≤ V <sub>CC</sub> + 0.3V* <sup>3</sup>
Maximum Clamp Current	I <sub>CLAMP</sub>	-	-4.0	+4.0	mA	Applicable to general purpose I/O pins * <sup>4</sup>
Total Maximum Clamp Current	Σ I <sub>CLAMP</sub>	-	-	32	mA	Applicable to general purpose I/O pins * <sup>4</sup>
"L" level maximum output current	I <sub>OL</sub>	-	-	15	mA	Normal port
	I <sub>OLHCO</sub>	-	-	20	mA	High current port
"L" level average output current	I <sub>OLAV</sub>	-	-	4	mA	Normal port
	I <sub>OLAVHCO</sub>	-	-	15	mA	High current port
"L" level maximum overall output current	ΣI <sub>OL</sub>	-	-	80	mA	Normal port
	ΣI <sub>OLHCO</sub>	-	-	150	mA	High current port
"L" level average overall output current	ΣI <sub>OLAV</sub>	-	-	40	mA	Normal port
	ΣI <sub>OLAVHCO</sub>	-	-	100	mA	High current port
"H" level maximum output current	I <sub>OH</sub>	-	-	-15	mA	Normal port
	I <sub>OHCO</sub>	-	-	-20	mA	High current port
"H" level average output current	I <sub>OHAV</sub>	-	-	-4	mA	Normal port
	I <sub>OHAVHCO</sub>	-	-	-15	mA	High current port
"H" level maximum overall output current	ΣI <sub>OH</sub>	-	-	-80	mA	Normal port
	ΣI <sub>OHCO</sub>	-	-	-150	mA	High current port
"H" level average overall output current	ΣI <sub>OHAV</sub>	-	-	-40	mA	Normal port
	ΣI <sub>OHAVHCO</sub>	-	-	-100	mA	High current port
Power consumption* <sup>5</sup>	P <sub>D</sub>	T <sub>A</sub> = +125°C	-	446* <sup>6</sup>	mW	
Operating ambient temperature	T <sub>A</sub>	-	-40	+125* <sup>7</sup>	°C	
Storage temperature	T <sub>STG</sub>	-	-55	+150	°C	

\*1: This parameter is based on V<sub>SS</sub> = AV<sub>SS</sub> = 0V.

\*2: AV<sub>CC</sub> and V<sub>CC</sub> must be set to the same voltage. It is required that AV<sub>CC</sub> does not exceed V<sub>CC</sub> and that the voltage at the analog inputs does not exceed AV<sub>CC</sub> when the power is switched on.

\*3: V<sub>I</sub> and V<sub>O</sub> should not exceed V<sub>CC</sub> + 0.3V. V<sub>I</sub> should also not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I<sub>CLAMP</sub> rating supersedes the V<sub>I</sub> rating. Input/Output voltages of general I/O ports depend on V<sub>CC</sub>.

\*4: • Applicable to all general purpose I/O pins (Pnn\_m).  
• Use within recommended operating conditions.

- Use at DC voltage (current).
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the  $V_{CC}$  pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset.
- The DEBUG I/F pin has only a protective diode against  $V_{SS}$ . Hence it is only permitted to input a negative clamping current (4mA). For protection against positive input voltages, use an external clamping diode which limits the input voltage to maximum 6.0V.

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	$V_{OH4}$	4mA type	$4.5V \leq V_{CC} \leq 5.5V$ $I_{OH} = -4mA$	$V_{CC} - 0.5$	-	$V_{CC}$	V	
			$2.7V \leq V_{CC} < 4.5V$ $I_{OH} = -1.5mA$					
	$V_{OH20}$	High Drive type	$4.5V \leq V_{CC} \leq 5.5V$ $I_{OH} = -20mA$	$V_{CC} - 0.6$	-	$V_{CC}$	V	
			$2.7V \leq V_{CC} < 4.5V$ $I_{OH} = -13mA$					
	$V_{OH3}$	3mA type	$4.5V \leq V_{CC} \leq 5.5V$ $I_{OH} = -3mA$	$V_{CC} - 0.5$	-	$V_{CC}$	V	
			$2.7V \leq V_{CC} < 4.5V$ $I_{OH} = -1.5mA$					
"L" level output voltage	$V_{OL4}$	4mA type	$4.5V \leq V_{CC} \leq 5.5V$ $I_{OL} = +4mA$	-	-	0.4	V	
			$2.7V \leq V_{CC} < 4.5V$ $I_{OL} = +1.7mA$					
	$V_{OL20}$	High Drive type	$4.5V \leq V_{CC} \leq 5.5V$ $I_{OL} = +20mA$	-	-	0.6	V	
			$2.7V \leq V_{CC} < 4.5V$ $I_{OL} = +13mA$					
	$V_{OL3}$	3mA type	$2.7V \leq V_{CC} < 5.5V$ $I_{OL} = +3mA$	-	-	0.4	V	
	$V_{OLD}$	DEBUG I/F	$V_{CC} = 2.7V$ $I_{OL} = +25mA$	0	-	0.25	V	

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input leak current	$I_{IL}$	Pnn_m	$V_{SS} < V_I < V_{CC}$ $AV_{SS}, AV_{RL} < V_I < AV_{CC}, AV_{RH}$	- 1	-	+ 1	$\mu A$	
		P08_m, P09_m, P10_m	$V_{SS} < V_I < V_{CC}$ $AV_{SS}, AV_{RL} < V_I < AV_{CC}, AV_{RH}$	- 3	-	+ 3	$\mu A$	
Total LCD leak current	$\Sigma  I_{LCD} $	All SEG/ COM pin	$V_{CC} = 5.0V$	-	0.5	10	$\mu A$	Maximum leakage current of all LCD pins
Internal LCD divide resistance	$R_{LCD}$	Between V3 and V2, V2 and V1, V1 and V0	$V_{CC} = 5.0V$	6.25	12.5	25	$k\Omega$	
Pull-up resistance value	$R_{PU}$	Pnn_m	$V_{CC} = 5.0V \pm 10\%$	25	50	100	$k\Omega$	
Input capacitance	$C_{IN}$	Other than C, $V_{CC}$ , $V_{SS}$ , $AV_{CC}$ , $AV_{SS}$ , $AV_{RH}$ , $AV_{RL}$ , P08_m, P09_m, P10_m	-	-	5	15	pF	
		P08_m, P09_m, P10_m	-	-	15	30	pF	

\*: In the case of high current outputs, set "1" to the bit in the Port High Drive Register.

## 14.4.3 Built-in RC Oscillation Characteristics

( $V_{CC} = AV_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$ )

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Clock frequency	$f_{RC}$	50	100	200	kHz	When using slow frequency of RC oscillator
		1	2	4	MHz	When using fast frequency of RC oscillator
RC clock stabilization time	$t_{RCSTAB}$	80	160	320	$\mu s$	When using slow frequency of RC oscillator (16 RC clock cycles)
		64	128	256	$\mu s$	When using fast frequency of RC oscillator (256 RC clock cycles)

## 14.4.4 Internal Clock Timing

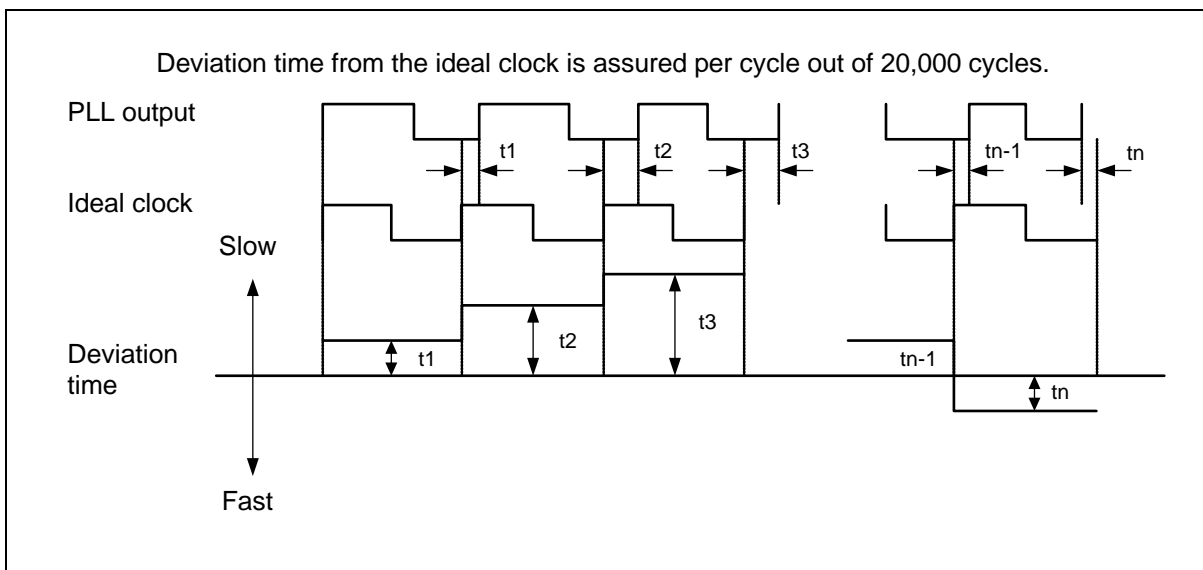
( $V_{CC} = AV_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$ )

Parameter	Symbol	Value		Unit
		Min	Max	
Internal System clock frequency (CLKS1 and CLKS2)	$f_{CLKS1}, f_{CLKS2}$	-	54	MHz
Internal CPU clock frequency (CLKB), Internal peripheral clock frequency (CLKP1)	$f_{CLKB}, f_{CLKP1}$	-	32	MHz
Internal peripheral clock frequency (CLKP2)	$f_{CLKP2}$	-	32	MHz

#### 14.4.5 Operating Conditions of PLL

( $V_{CC} = AV_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$ )

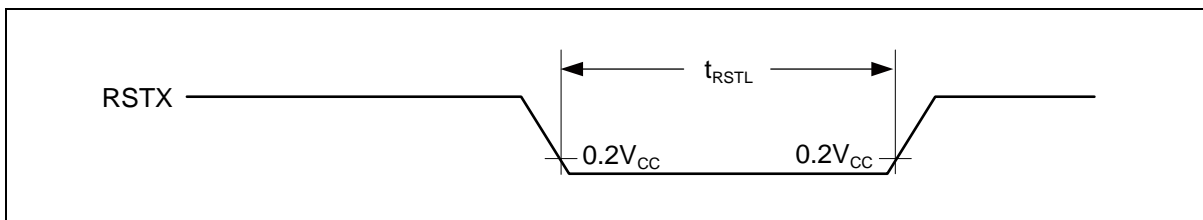
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time	$t_{LOCK}$	1	-	4	ms	For CLKMC = 4MHz
PLL input clock frequency	$f_{PLLI}$	4	-	8	MHz	
PLL oscillation clock frequency	$f_{CLKVCO}$	56	-	108	MHz	Permitted VCO output frequency of PLL (CLKVCO)
PLL phase jitter	$t_{PSKEW}$	-5	-	+5	ns	For CLKMC (PLL input clock) $\geq$ 4MHz



#### 14.4.6 Reset Input

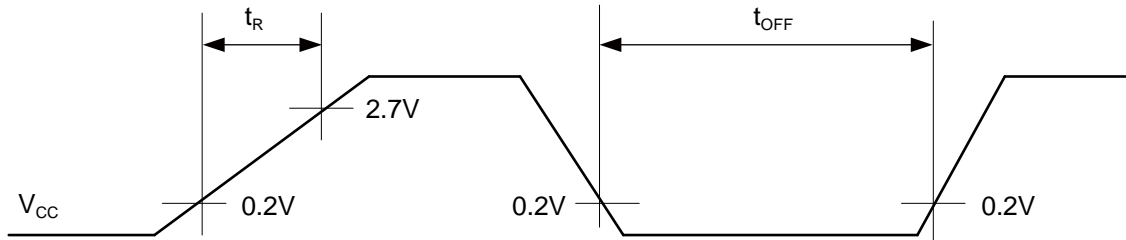
( $V_{CC} = AV_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$ )

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Reset input time	$t_{RSTL}$	RSTX	10	-	$\mu s$
Rejection of reset input time			1	-	$\mu s$

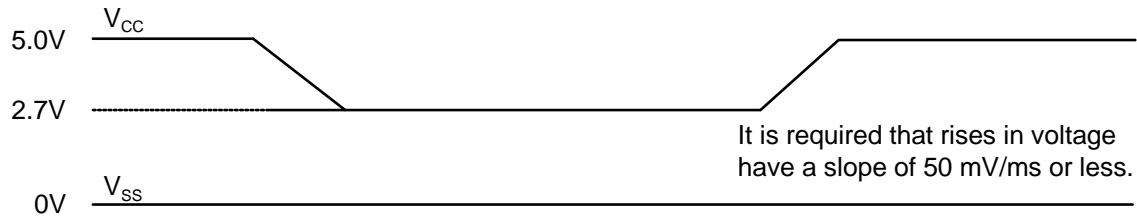


**14.4.7 Power-on Reset Timing**
 $(V_{CC} = AV_{CC} = 2.7V \text{ to } 5.5V, V_{SS} = AV_{SS} = 0V, T_A = -40^{\circ}C \text{ to } +125^{\circ}C)$ 

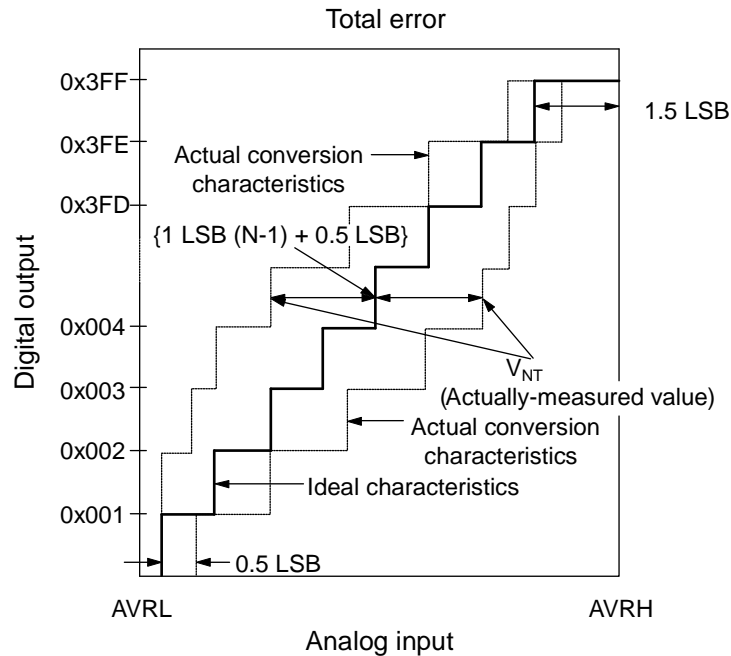
Parameter	Symbol	Pin name	Value			Unit
			Min	Typ	Max	
Power on rise time	$t_R$	V <sub>CC</sub>	0.05	-	30	ms
Power off time	$t_{OFF}$	V <sub>CC</sub>	1	-	-	ms



If the power supply is changed too rapidly, a power-on reset may occur. We recommend a smooth startup by restraining voltages when changing the power supply voltage during operation, as shown in the figure below.







$$1\text{LSB (Ideal value)} = \frac{\text{AVRH} - \text{AVRL}}{1024} \text{ [V]}$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\text{LSB} \times (N - 1) + 0.5\text{LSB}\}}{1\text{LSB}}$$

N : A/D converter digital output value.

$V_{NT}$  : Voltage at which the digital output changes from 0x(N + 1) to 0xN.

$V_{OT}$  (Ideal value) = AVRL + 0.5LSB[V]

$V_{FST}$  (Ideal value) = AVRH - 1.5LSB[V]

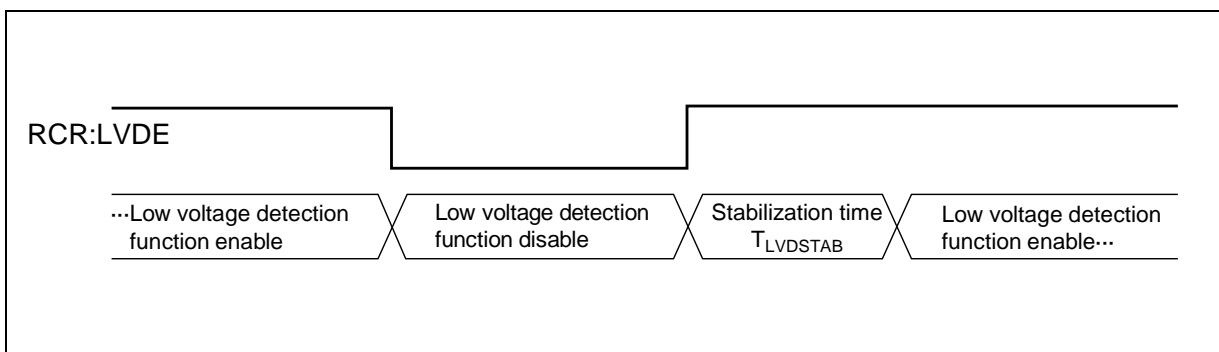
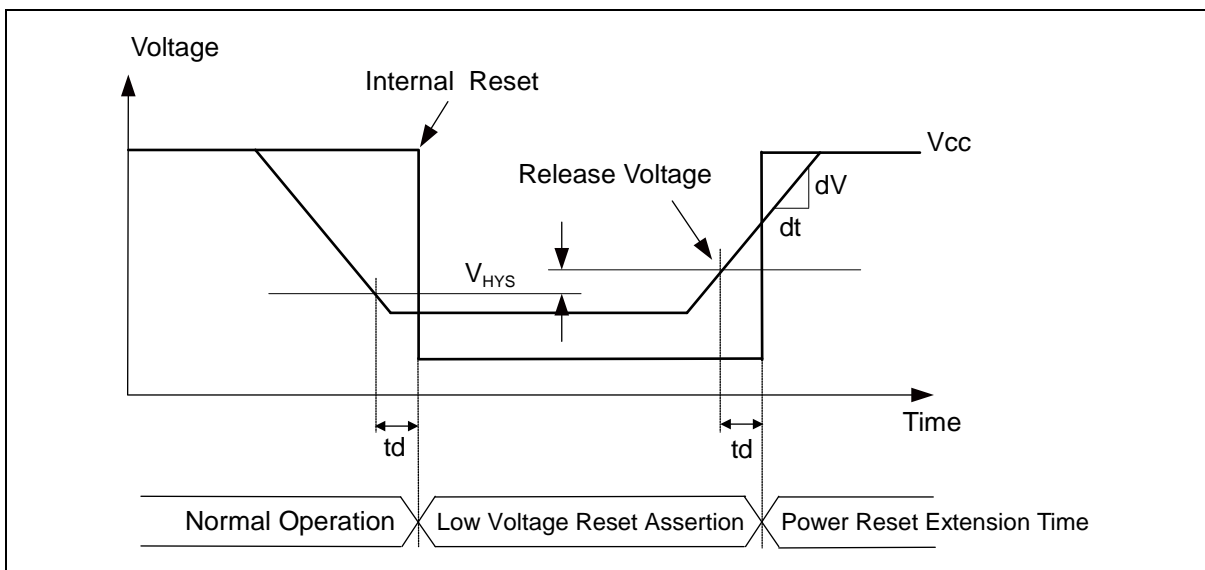
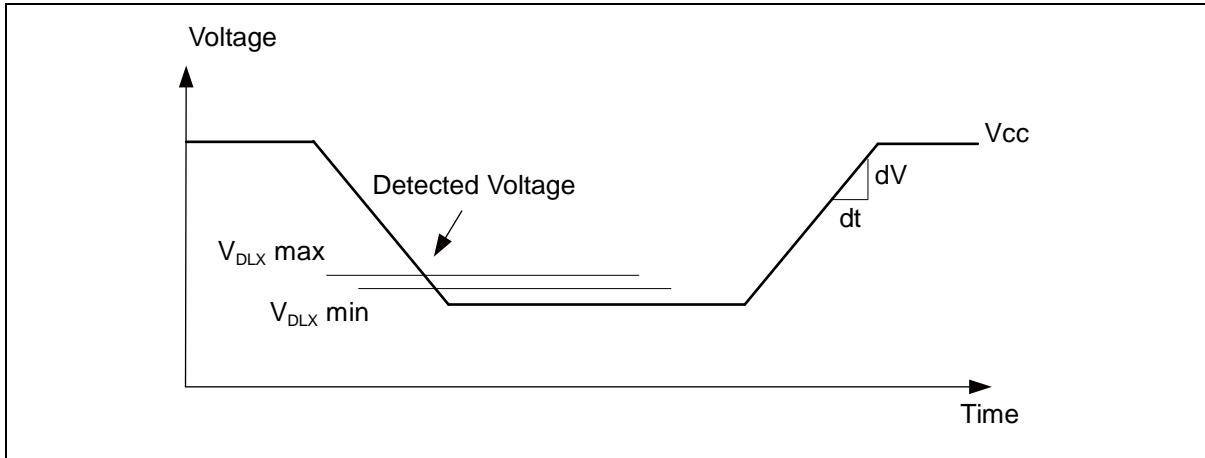
## 14.7 Low Voltage Detection Function Characteristics

( $V_{CC} = AV_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$ )

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Detected voltage <sup>*1</sup>	$V_{DL0}$	CILCR:LVL = 0000 <sub>B</sub>	2.70	2.90	3.10	V
	$V_{DL1}$	CILCR:LVL = 0001 <sub>B</sub>	2.79	3.00	3.21	V
	$V_{DL2}$	CILCR:LVL = 0010 <sub>B</sub>	2.98	3.20	3.42	V
	$V_{DL3}$	CILCR:LVL = 0011 <sub>B</sub>	3.26	3.50	3.74	V
	$V_{DL4}$	CILCR:LVL = 0100 <sub>B</sub>	3.45	3.70	3.95	V
	$V_{DL5}$	CILCR:LVL = 0111 <sub>B</sub>	3.73	4.00	4.27	V
	$V_{DL6}$	CILCR:LVL = 1001 <sub>B</sub>	3.91	4.20	4.49	V
Power supply voltage change rate <sup>*2</sup>	dV/dt	-	- 0.004	-	+ 0.004	V/ $\mu$ s
Hysteresis width	$V_{HYS}$	CILCR:LVHYS=0	-	-	50	mV
		CILCR:LVHYS=1	80	100	120	mV
Stabilization time	$T_{LVDSTAB}$	-	-	-	75	$\mu$ s
Detection delay time	$t_d$	-	-	-	30	$\mu$ s

\*1: If the power supply voltage fluctuates within the time less than the detection delay time ( $t_d$ ), there is a possibility that the low voltage detection will occur or stop after the power supply voltage passes the detection range.

\*2: In order to perform the low voltage detection at the detection voltage ( $V_{DLX}$ ), be sure to suppress fluctuation of the power supply voltage within the limits of the change ration of power supply voltage.



## 14.8 Flash Memory Write/Erase Characteristics

( $V_{CC} = AV_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$ )

Parameter		Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Sector erase time	Large Sector	$T_A \leq +105^{\circ}C$	-	1.6	7.5	s	Includes write time prior to internal erase.
	Small Sector	-	-	0.4	2.1	s	
	Security Sector	-	-	0.31	1.65	s	
Word (16-bit) write time	Large Sector	$T_A \leq +105^{\circ}C$	-	25	400	$\mu s$	Not including system-level overhead time.
	Small Sector	-	-	25	400	$\mu s$	
Chip erase time		$T_A \leq +105^{\circ}C$	-	8.31	40.05	s	Includes write time prior to internal erase.

Note: While the Flash memory is written or erased, shutdown of the external power ( $V_{CC}$ ) is prohibited. In the application system where the external power ( $V_{CC}$ ) might be shut down while writing or erasing, be sure to turn the power off by using a low voltage detection function.

To put it concrete, change the external power in the range of change ration of power supply voltage ( $-0.004V/\mu s$  to  $+0.004V/\mu s$ ) after the external power falls below the detection voltage ( $V_{DLX}$ )\*1.

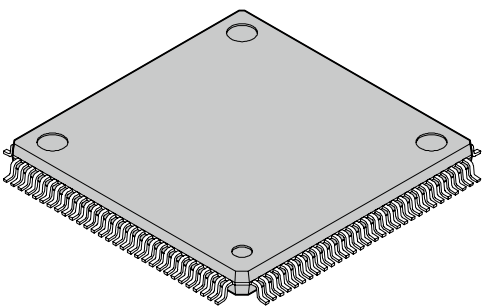
Write/Erase cycles and data hold time

Write/Erase cycles (cycle)	Data hold time (year)
1,000	$20^{-2}$
10,000	$10^{-2}$
100,000	$5^{-2}$

\*1: See "14.7. Low Voltage Detection Function Characteristics".

\*2: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at  $+85^{\circ}C$ ).

## 17. Package Dimension

<p>120-pin plastic LQFP</p>  <p>(FPT-120P-M21)</p>	Lead pitch	0.50 mm
	Package width × package length	16.0 × 16.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.88 g
	Code (Reference)	P-LFQFP120-16×16-0.50

