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Details	
Product Status	Not For New Designs
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Core Size	16-Bit
Speed	25MHz
Connectivity	SCI, SmartCard
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Number of I/O	70
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BFQFP
Supplier Device Package	100-QFP (14x14)
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Table 2.8 Branching Instructions

Instruction	Size	Function
Bcc	—	Branches to a specified address if address specified condition is met. The branching conditions are listed below.

Mnemonic	Description	Condition
BRA (BT)	Always (true)	Always
BRN (BF)	Never (false)	Never
BHI	High	$C \vee Z = 0$
BLS	Low or same	$C \vee Z = 1$
Bcc (BHS)	Carry clear (high or same)	$C = 0$
BCS (BLO)	Carry set (low)	$C = 1$
BNE	Not equal	$Z = 0$
BEQ	Equal	$Z = 1$
BVC	Overflow clear	$V = 0$
BVS	Overflow set	$V = 1$
BPL	Plus	$N = 0$
BMI	Minus	$N = 1$
BGE	Greater or equal	$N \oplus V = 0$
BLT	Less than	$N \oplus V = 1$
BGT	Greater than	$Z \vee (N \oplus V) = 0$
BLE	Less or equal	$Z \vee (N \oplus V) = 1$

JMP	—	Branches unconditionally to a specified address
BSR	—	Branches to a subroutine at a specified address
JSR	—	Branches to a subroutine at a specified address
RTS	—	Returns from a subroutine

Execution of BCLR Instruction

```
BCLR  #0, @P4DDR      ;Clear bit 0 in data direction register
```

After Execution of BCLR Instruction

	$P4_7$	$P4_6$	$P4_5$	$P4_4$	$P4_3$	$P4_2$	$P4_1$	$P4_0$
Input/output	Output	Output	Output	Output	Output	Output	Output	Input
DDR	1	1	1	1	1	1	1	0

Explanation: To execute the BCLR instruction, the CPU begins by reading P4DDR. Since P4DDR is a write-only register, it is read as H'FF, even though its true value is H'3F.

Next the CPU clears bit 0 of the read data, changing the value to H'FE.

Finally, the CPU writes this value (H'FE) back to P4DDR to complete the BCLR instruction.

As a result, $P4_0$DDR is cleared to 0, making $P4_0$ an input pin. In addition, $P4_7$DDR and $P4_6$DDR are set to 1, making $P4_7$ and $P4_6$ output pins.

The BCLR instruction can be used to clear flags in the on-chip registers to 0. In an interrupt-handling routine, for example, if it is known that the flag is set to 1, it is not necessary to read the flag ahead of time.

Bits 6 to 4—Standby Timer Select 2 to 0 (STS2 to STS0): These bits select the length of time the CPU and on-chip supporting modules wait for the internal clock oscillator to settle when software standby mode is exited by an external interrupt.

When using a crystal oscillator, set these bits so that the waiting time will be at least 7 ms at the system clock rate.

For further information about waiting time selection, see section 20.4.3, Selection of Waiting Time for Exit from Software Standby Mode.

Bit 6 STS2	Bit 5 STS1	Bit 4 STS0	Description	
0	0	0	Waiting time = 8,192 states	(Initial value)
0	0	1	Waiting time = 16,384 states	
0	1	0	Waiting time = 32,768 states	
0	1	1	Waiting time = 65,536 states	
1	0	0	Waiting time = 131,072 states	
1	0	1	Waiting time = 262,144 states	
1	1	0	Waiting time = 1,024 states	
1	1	1	Illegal setting	

Bit 3—User Bit Enable (UE): Selects whether to use the UI bit in the condition code register as a user bit or an interrupt mask bit.

Bit 3 UE	Description	
0	UI bit in CCR is used as an interrupt mask bit	
1	UI bit in CCR is used as a user bit	(Initial value)

Bit 2—NMI Edge Select (NMIEG): Selects the valid edge of the NMI input.

Bit 2 NMIEG	Description	
0	An interrupt is requested at the falling edge of NMI	(Initial value)
1	An interrupt is requested at the rising edge of NMI	

Interrupt Source	Origin	Vector Number	Vector Address*1		IPR	Priority
			Advanced Mode	Normal Mode*2		
IMIA2 (compare match/ input capture A2)	16-bit timer channel 2	32	H'0080 to H'0083	H'0040 to H'0041	IPRA0	High
IMIB2 (compare match/ input capture B2)		33	H'0084 to H'0087	H'0042 to H'0043		
OVI2 (overflow 2)		34	H'0088 to H'008B	H'0044 to H'0045		
Reserved	—	35	H'008C to H'008F	H'0046 to H'0047		
CMIA0 (compare match A0)	8-bit timer channel 0/1	36	H'0090 to H'0093	H'0048 to H'0049	IPRB7	
CMIB0 (compare match B0)		37	H'0094 to H'0097	H'004A to H'004B		
CMIA1/CMIB1 (compare match A1/B1)		38	H'0098 to H'009B	H'004C to H'004D		
TOVI0/TOVI1 (overflow 0/1)		39	H'009C to H'009F	H'004E to H'004F		
CMIA2 (compare match A2)	8-bit timer channel 2/3	40	H'00A0 to H'00A3	H'0050 to H'0051	IPRB6	
CMIB2 (compare match B2)		41	H'00A4 to H'00A7	H'0052 to H'0053		
CMIA3/CMIB3 (compare match A3/B3)		42	H'00A8 to H'00AB	H'0054 to H'0055		
TOVI2/TOVI3 (overflow 2/3)		43	H'00AC to H'00AF	H'0056 to H'0057		
DEND0A	DMAC	44	H'00B0 to H'00B3	H'0058 to H'0059	IPRB5	
DEND0B		45	H'00B4 to H'00B7	H'005A to H'005B		
DEND1A		46	H'00B8 to H'00BB	H'005C to H'005D		
DEND1B		47	H'00BC to H'00BF	H'005E to H'005F		
Reserved	—	48	H'00C0 to H'00C3	H'0060 to H'0061	—	
		49	H'00C4 to H'00C7	H'0062 to H'0063		
		50	H'00C8 to H'00CB	H'0064 to H'0065		
		51	H'00CC to H'00CF	H'0066 to H'0067		Low

Note: * Only 0 can be written to clear the flag.

Bit 7—Compare Match Flag (CMF): Status flag that indicates a match between the values of RTCNT and RTCOR.

Bit 7 CMF	Description	
0	[Clearing conditions] When the chip is reset and in standby mode Read CMF when CMF = 1, then write 0 in CMF	(Initial value)
1	[Setting condition] When RTCNT = RTCOR	

Bit 6—Compare Match Interrupt Enable (CMIE): Enables or disables the CMI interrupt requested when the CMF flag is set to 1 in RTMCSR. The CMIE bit is always cleared to 0 when any of areas 2 to 5 is designated as DRAM space.

Bit 6 CMIE	Description	
0	The CMI interrupt requested by CMF is disabled	(Initial value)
1	The CMI interrupt requested by CMF is enabled	

Bits 5 to 3—Refresh Counter Clock Select (CKS2 to CKS0): These bits select the clock to be input to RTCNT from among 7 clocks obtained by dividing the system clock (ϕ). When the input clock is selected with bits CKS2 to CKS0, RTCNT begins counting up.

Bit 5 CKS2	Bit 4 CKS1	Bit 3 CKS0	Description	
0	0	0	Count operation halted	(Initial value)
		1	ϕ/2 used as counter clock	
	1	0	ϕ/8 used as counter clock	
		1	ϕ/32 used as counter clock	
1	0	0	ϕ/128 used as counter clock	
		1	ϕ/512 used as counter clock	
	1	0	ϕ/2048 used as counter clock	
		1	ϕ/4096 used as counter clock	

Bits 2 to 0—Reserved: These bits cannot be modified and are always read as 1.

16-Bit, Two-State-Access Areas: Figures 6.14 to 6.16 show the timing of bus control signals for a 16-bit, two-state-access area. In these areas, the upper data bus (D_{15} to D_8) is used in accesses to even addresses and the lower data bus (D_7 to D_0) in accesses to odd addresses. Wait states cannot be inserted.

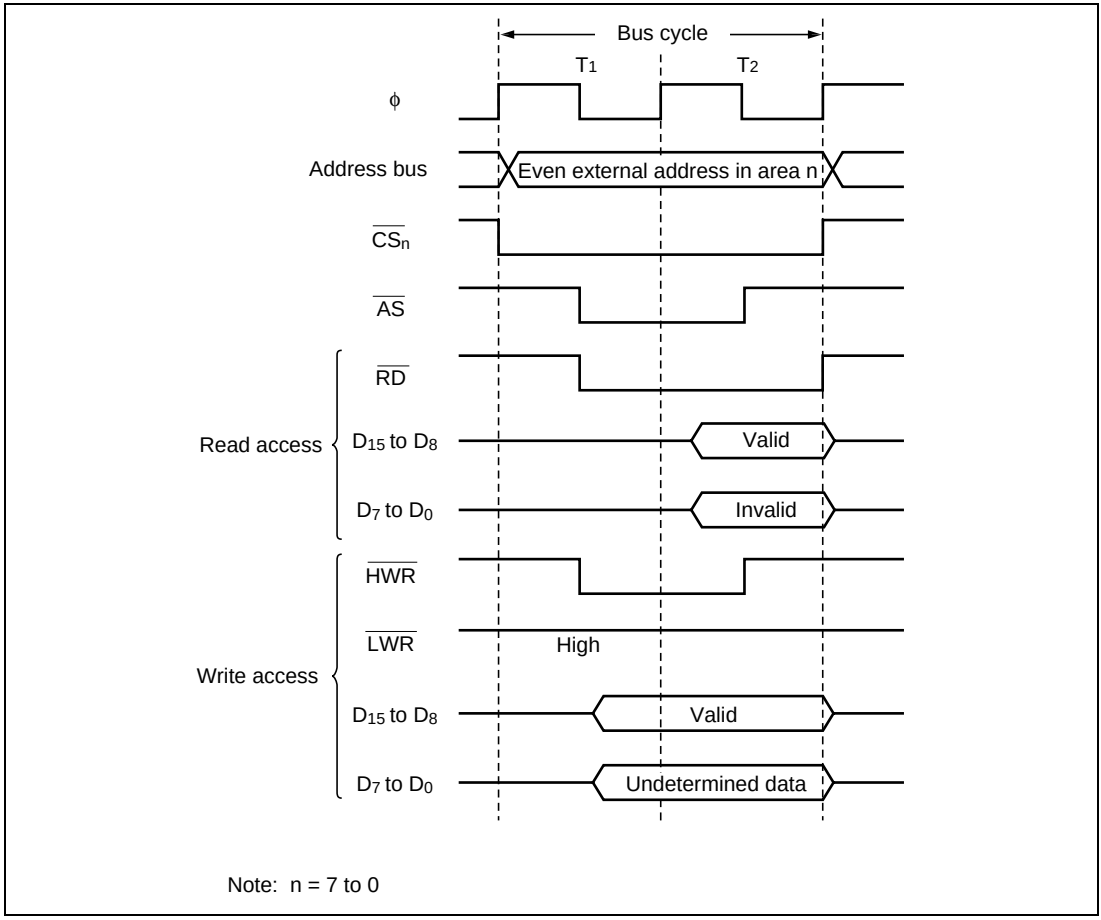


Figure 6.14 Bus Control Signal Timing for 16-Bit, Two-State-Access Area (1) (Byte Access to Even Address)

Table 6.6 Settings of Bits MXC1 and MXC0 and Address Multiplexing Method

	DRCRB		Column Address	Address Pins													
	MXC1	MXC0	Bits	A_{23} to A_{13}	A_{12}	A_{11}	A_{10}	A_{9}	A_{8}	A_{7}	A_{6}	A_{5}	A_{4}	A_{3}	A_{2}	A_{1}	A_{0}
Row address	0	0	8 bits	A_{23} to A_{13}	A_{20}*	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_{9}	A_{8}
		1	9 bits	A_{23} to A_{13}	A_{12}	A_{20}*	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_{9}
	1	0	10 bits	A_{23} to A_{13}	A_{12}	A_{11}	A_{20}*	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}
		1	Illegal setting	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Column address	—	—	—	A_{23} to A_{13}	A_{12}	A_{11}	A_{10}	A_{9}	A_{8}	A_{7}	A_{6}	A_{5}	A_{4}	A_{3}	A_{2}	A_{1}	A_{0}

Note: * Row address bit A_{20} is not multiplexed in 1-Mbyte mode.

6.5.4 Data Bus

If the bit in ABWCR corresponding to an area designated as DRAM space is set to 1, that area is designated as 8-bit DRAM space; if the bit is cleared to 0, the area is designated as 16-bit DRAM space. In 16-bit DRAM space, × 16-bit organization DRAM can be connected directly.

In 8-bit DRAM space the upper half of the data bus, D_{15} to D_{8}, is enabled, while in 16-bit DRAM space both the upper and lower halves of the data bus, D_{15} to D_{0}, are enabled.

Access sizes and data alignment are the same as for the basic bus interface: see section 6.4.2, Data Size and Data Alignment.

6.5.5 Pins Used for DRAM Interface

Table 6.7 shows the pins used for DRAM interfacing and their functions.

6.5.10 Burst Operation

With DRAM, in addition to full access (normal access) in which data is accessed by outputting a row address for each access, a fast page mode is also provided which can be used when making a number of consecutive accesses to the same row address. This mode enables fast (burst) access of data by simply changing the column address after the row address has been output. Burst access can be selected by setting the BE bit to 1 in DRCRA.

Burst Access (Fast Page Mode) Operation Timing: Figure 6.22 shows the operation timing for burst access. When there are consecutive access cycles for DRAM space, the column address and $\overline{CAS}$ signal output cycles (two states) continue as long as the row address is the same for consecutive access cycles. In burst access, too, the bus cycle can be extended by inserting wait states between T_{c1} and T_{c2}. The wait state insertion method and timing are the same as for full access: see section 6.5.8, Wait Control, for details.

The row address used for the comparison is determined by the bus width of the relevant area set in bits MXC1 and MXC0 in DRCRB, and in ABWCR. Table 6.9 shows the compared row addresses corresponding to the various settings of bits MXC1 and MXC0, and ABWCR.

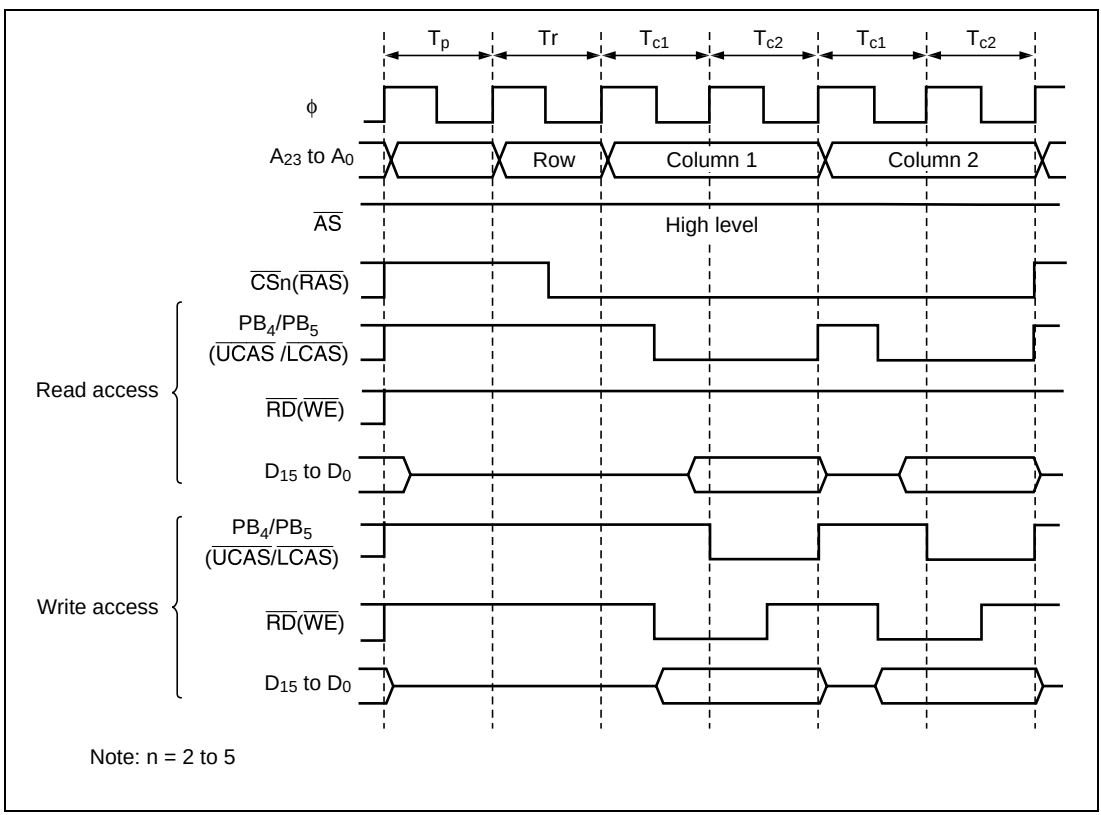


Figure 6.22 Operation Timing in Fast Page Mode

Bit 7—Data Transfer Enable (DTE): Together with the DTME bit in DTCRB, this bit enables or disables data transfer on the channel. When the DTME and DTE bits are both set to 1, the channel is enabled. If auto-request is specified, data transfer begins immediately. Otherwise, the channel waits for transfers to be requested. When the specified number of transfers have been completed, the DTE bit is automatically cleared to 0. When DTE is 0, the channel is disabled and does not accept transfer requests. DTE is set to 1 by reading the register when DTE is 0, then writing 1.

Bit 7 DTE	Description	
0	Data transfer is disabled (DTE is cleared to 0 when the specified number of transfers have been completed)	(Initial value)
1	Data transfer is enabled	

If DTIE is set to 1, a CPU interrupt is requested when DTE is cleared to 0.

Bit 6—Data Transfer Size (DTSZ): Selects the data size of each transfer.

Bit 6 DTSZ	Description	
0	Byte-size transfer	(Initial value)
1	Word-size transfer	

Bit 5—Source Address Increment/Decrement (SAID) and,
Bit 4—Source Address Increment/Decrement Enable (SAIDE): These bits select whether the source address register (MARA) is incremented, decremented, or held fixed during the data transfer.

Bit 5 SAID	Bit 4 SAIDE	Description	
0	0	MARA is held fixed	(Initial value)
	1	MARA is incremented after each data transfer • If DTSZ = 0, MARA is incremented by 1 after each transfer • If DTSZ = 1, MARA is incremented by 2 after each transfer	
1	0	MARA is held fixed	
	1	MARA is decremented after each data transfer • If DTSZ = 0, MARA is decremented by 1 after each transfer • If DTSZ = 1, MARA is decremented by 2 after each transfer	

9.5.3 Interrupt Sources

Each 16-bit timer channel can generate a compare match/input capture A interrupt, a compare match/input capture B interrupt, and an overflow interrupt. In total there are nine interrupt sources of three kinds, all independently vectored. An interrupt is requested when the interrupt request flag are set to 1.

The priority order of the channels can be modified in interrupt priority registers A (IPRA). For details see section 5, Interrupt Controller.

Table 9.6 lists the interrupt sources.

Table 9.6 16-bit timer Interrupt Sources

Channel	Interrupt Source	Description	Priority*
0	IMIA0	Compare match/input capture A0	High
	IMIB0	Compare match/input capture B0	
	OVI0	Overflow 0	
1	IMIA1	Compare match/input capture A1	
	IMIB1	Compare match/input capture B1	
	OVI1	Overflow 1	
2	IMIA2	Compare match/input capture A2	
	IMIB2	Compare match/input capture B2	
	OVI2	Overflow 2	Low

Note: * The priority immediately after a reset is indicated. Inter-channel priorities can be changed by settings in IPRA.

11.3.4 Non-Overlapping TPC Output

Sample Setup Procedure for Non-Overlapping TPC Output: Figure 11.6 shows a sample procedure for setting up non-overlapping TPC output.

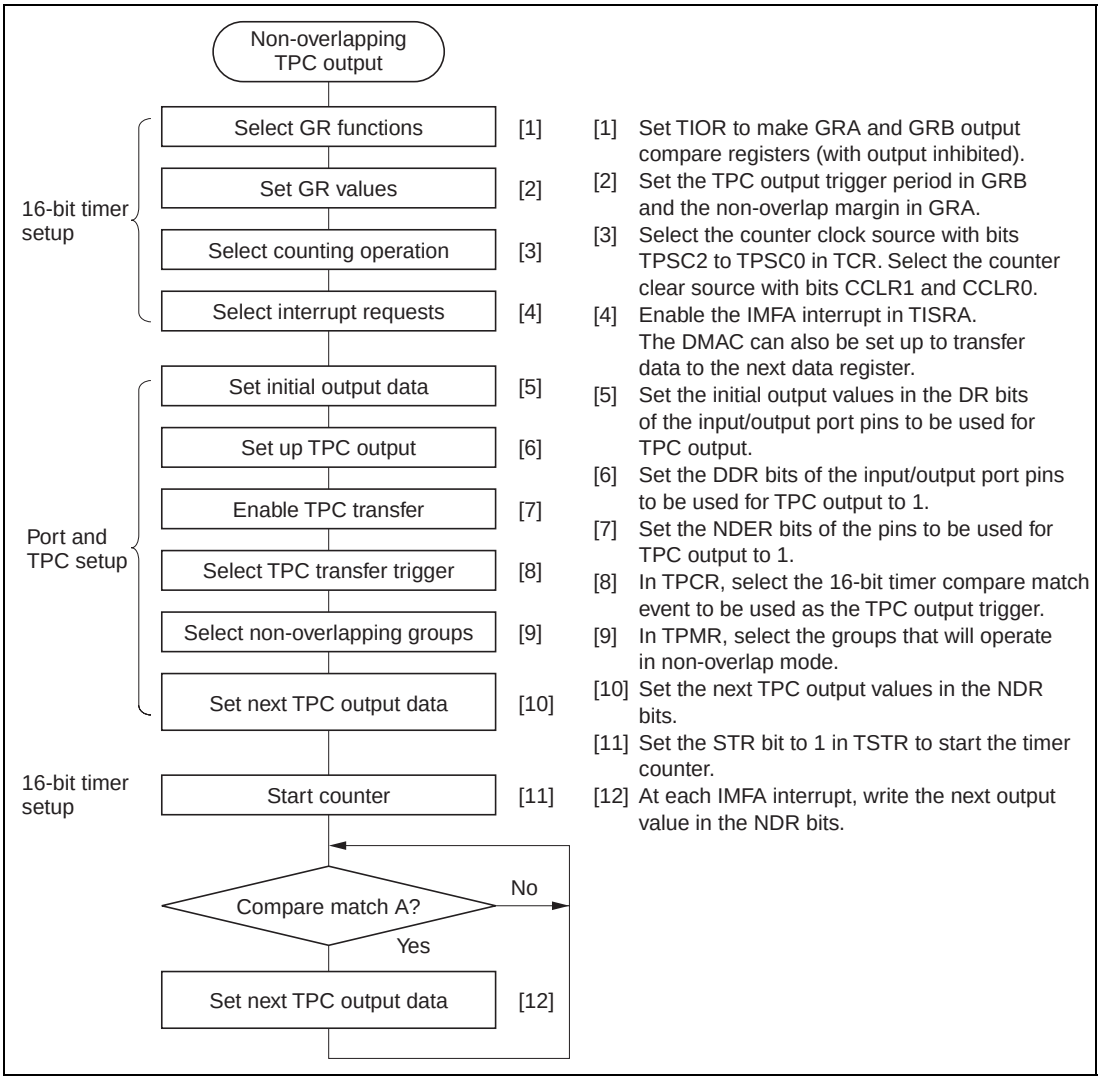


Figure 11.6 Setup Procedure for Non-Overlapping TPC Output (Example)

Bit 7—Watchdog Timer Reset (WRST): During watchdog timer operation, this bit indicates that TCNT has overflowed and generated a reset signal. This reset signal resets the entire H8/3069R chip internally.

Bit 7 WRST	Description	
0	[Clearing condition] Reset signal at $\overline{\text{RES}}$ pin. Read WRST when WRST =1, then write 0 in WRST.	(Initial value)
1	[Setting condition] Set when TCNT overflow generates a reset signal during watchdog timer operation	

Bit 6—Reserved: The write value should always be 0.

Bits 5 to 0—Reserved: These bits are always read as 1. The write value should always be 1.

12.2.4 Notes on Register Access

The watchdog timer's TCNT, TCSR, and RSTCSR registers differ from other registers in being more difficult to write. The procedures for writing and reading these registers are given below.

Writing to TCNT and TCSR: These registers must be written by a word transfer instruction. They cannot be written by byte instructions. Figure 12.2 shows the format of data written to TCNT and TCSR. TCNT and TCSR both have the same write address. The write data must be contained in the lower byte of the written word. The upper byte must contain H'5A (password for TCNT) or H'A5 (password for TCSR). This transfers the write data from the lower byte to TCNT or TCSR.

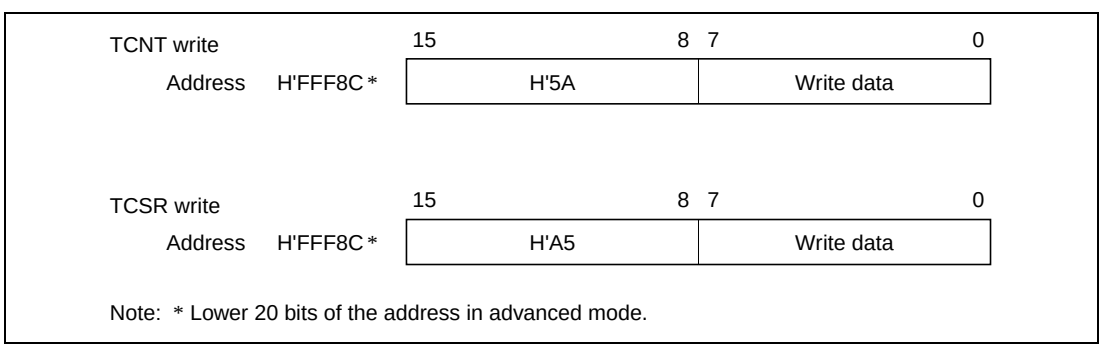


Figure 12.2 Format of Data Written to TCNT and TCSR

Bits 1 and 0—Clock Select 1 and 0 (CKS1/0): These bits select the clock source for the on-chip baud rate generator. Four clock sources are available: ϕ, $\phi/4$, $\phi/16$, and $\phi/64$.

For the relationship between the clock source, bit rate register setting, and baud rate, see section 13.2.8, Bit Rate Register (BRR).

Bit 1 CKS1	Bit 0 CKS0	Description
0	0	ϕ (Initial value)
0	1	$\phi/4$
1	0	$\phi/16$
1	1	$\phi/64$

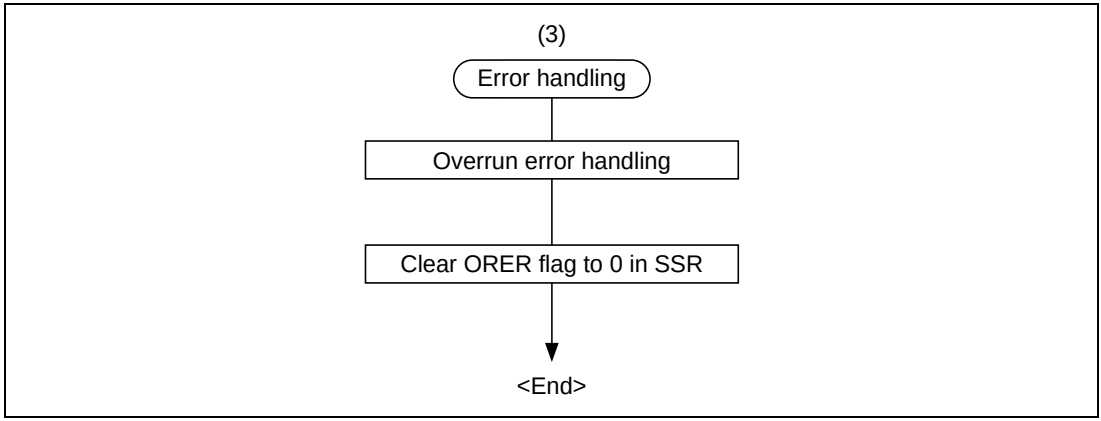


Figure 13.18 Sample Flowchart for Serial Receiving (2)

In receiving, the SCI operates as follows:

- The SCI synchronizes with serial clock input or output and synchronizes internally.
- Receive data is stored in RSR in order from LSB to MSB.

  After receiving the data, the SCI checks that the RDRF flag is 0, so that receive data can be transferred from RSR to RDR. If this check passes, the RDRF flag is set to 1 and the received data is stored in RDR. If the checks fails (receive error), the SCI operates as shown in table 13.11.

  When a receive error has been identified in the error check, subsequent transmit and receive operations are disabled.
- When the RDRF flag is set to 1, if the RIE bit is set to 1 in SCR, a receive-data-full interrupt (RXI) is requested. If the ORER flag is set to 1 and the RIE bit in SCR is also set to 1, a receive-error interrupt (ERI) is requested.

Bit 7—D/A Output Enable 1 (DAOE1): Controls D/A conversion and analog output.

Bit 7 DAOE1	Description
0	DA_1 analog output is disabled
1	Channel-1 D/A conversion and DA_1 analog output are enabled

Bit 6—D/A Output Enable 0 (DAOE0): Controls D/A conversion and analog output.

Bit 6 DAOE0	Description
0	DA_0 analog output is disabled
1	Channel-0 D/A conversion and DA_0 analog output are enabled

Bit 5—D/A Enable (DAE): Controls D/A conversion, together with bits DAOE0 and DAOE1. When the DAE bit is cleared to 0, analog conversion is controlled independently in channels 0 and 1. When the DAE bit is set to 1, analog conversion is controlled together in channels 0 and 1. Output of the conversion results is always controlled independently by DAOE0 and DAOE1.

Bit 7 DAOE1	Bit 6 DAOE0	Bit 5 DAE	Description
0	0	—	D/A conversion is disabled in channels 0 and 1
	1	0	D/A conversion is enabled in channel 0
			D/A conversion is disabled in channel 1
		1	D/A conversion is enabled in channels 0 and 1
1	0	0	D/A conversion is disabled in channel 0
			D/A conversion is enabled in channel 1
		1	D/A conversion is enabled in channels 0 and 1
	1	—	D/A conversion is enabled in channels 0 and 1

When the DAE bit is set to 1, even if bits DAOE0 and DAOE1 in DACR and the ADST bit in ADCSR are cleared to 0, the same current is drawn from the analog power supply as during A/D and D/A conversion.

Bits 4 to 0—Reserved: These bits cannot be modified and are always read as 1.

Table 18.9 Hardware Protection

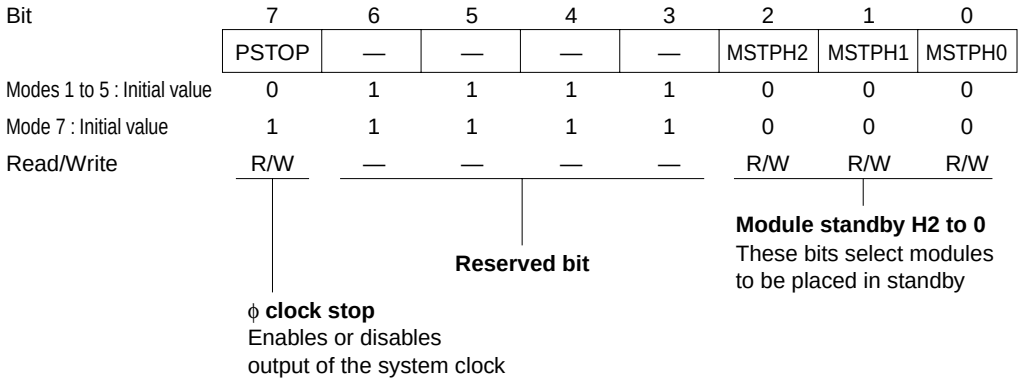
Item	Description	Function to be Protected	
		Download	Program/Erase
FWE-pin protection	• The input of a low-level signal on the FWE pin clears the FWE bit of FCCS and the device enters a program/erase-protected state.	—	○
Reset/standby protection	• A power-on reset (including a power-on reset by the WDT) and entry to standby mode reinitialize the program/erase interface register and the device enters a program/erase-protected state. • Resetting by means of the $\overline{\text{RES}}$ pin after power is initially supplied will not make the device enter the reset state unless the $\overline{\text{RES}}$ pin is held low until oscillation has stabilized. In the case of a reset during operation, hold the $\overline{\text{RES}}$ pin low for the RES pulse width that is specified in the section on AC characteristics section. If the device is reset during programming or erasure, data values in the flash memory are not guaranteed. In this case, after keeping the $\overline{\text{RES}}$ pin low for at least 100 µs, execute erasure and then execute programming again.	○	○

18.6.2 Software Protection

Software protection is set up in any of three ways: by disabling the downloading of on-chip programs for programming and erasing, by means of a key code, and by the RAM-emulation register.

20.2.2 Module Standby Control Register H (MSTCRH)

MSTCRH is an 8-bit readable/writable register that controls output of the system clock (ϕ). It also controls the module standby function, which places individual on-chip supporting modules in the standby state. Module standby can be designated for the SCI0, SCI1, SCI2.



In modes 1 to 5, MSTCRH is initialized to H'78 by a reset and in hardware standby mode, while in mode 7 it is initialized to H'F8. It is not initialized in software standby mode.

Bit 7—ϕ Clock Stop (PSTOP): Enables or disables output of the system clock (ϕ).

Bit 1 PSTOP	Description	
0	System clock output is enabled	(Initial value : When modes 1 to 5 are selected)
1	System clock output is disabled	(Initial value : When mode 7 is selected)

Bits 6 to 3—Reserved: These bits cannot be modified and are always read as 1.

Bit 2—Module Standby H2 (MSTPH2): Selects whether to place the SCI2 in standby.

Bit 2 MSTPH2	Description	
0	SCI2 operates normally	(Initial value)
1	SCI2 is in standby state	

21.2.6 Flash Memory Characteristics

Table 21.20 shows the flash memory characteristics.

Table 21.20 Flash Memory Characteristics

Conditions: V_{CC} = AV_{CC} = 4.5 V to 5.5 V, V_{SS} = AV_{SS} = 0 V,
T_a = 0°C to +85°C (operating temperature range for programming/erasing : Wide-range specifications)

Item	Symbol	Min	Typ	Max	Unit	Notes
Programming time*1 *2 *4	t_P	—	3	30	ms/ 128 bytes	
Erase time*1 *2 *4	t_E	—	80	800	ms/4k blocks	
		—	500	5000	ms/32k blocks	
		—	1000	10000	ms/64k blocks	
Programming time (total)*1 *2 *4	Σt_P	—	10	30	s/512k bytes	T_a = 25°C, all "0"
Erase time (total)*1 *2 *4	Σt_E	—	10	30	s/512k bytes	T_a = 25°C
Programming and erase time (total)*1 *2 *4	Σt_{PE}	—	20	60	s/512k bytes	T_a = 25°C
Reprogramming count	N_{WEC}	100*3	—	—	times	
Data retention time*4	t_{DRP}	10	—	—	year	

Notes: 1. Programming and erase time depend on the data size.
2. Programming and erase time excluded the data transfer time.
3. It is the number of times of min. which guarantees all the characteristics after reprogramming. (A guarantee is the range of a 1-min. value.)
4. It is the characteristic when reprogramming is performed by specification within the limits including a min. value.

Address (Low)	Register Name	Data Bus Width	Bit Names								Module Name
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'EE060	—		—	—	—	—	—	—	—	—	
H'EE061	—		—	—	—	—	—	—	—	—	
H'EE062	—		—	—	—	—	—	—	—	—	
H'EE063	—		—	—	—	—	—	—	—	—	
H'EE064	—		—	—	—	—	—	—	—	—	
H'EE065	—		—	—	—	—	—	—	—	—	
H'EE066	—		—	—	—	—	—	—	—	—	
H'EE067	—		—	—	—	—	—	—	—	—	
H'EE068	—		—	—	—	—	—	—	—	—	
H'EE069	—		—	—	—	—	—	—	—	—	
H'EE06A	—		—	—	—	—	—	—	—	—	
H'EE06B	—		—	—	—	—	—	—	—	—	
H'EE06C	—		—	—	—	—	—	—	—	—	
H'EE06D	—		—	—	—	—	—	—	—	—	
H'EE06E	—		—	—	—	—	—	—	—	—	
H'EE06F	—		—	—	—	—	—	—	—	—	
H'EE070	—		—	—	—	—	—	—	—	—	
H'EE071	—		—	—	—	—	—	—	—	—	
H'EE072	—		—	—	—	—	—	—	—	—	
H'EE073	—		—	—	—	—	—	—	—	—	
H'EE074	Reserved area (access prohibited)										
H'EE075											
H'EE076											
H'EE077	RAMCR	8	—	—	—	—	RAMS	RAM2	RAM1	RAM0	Flash memory*
H'EE078	—		—	—	—	—	—	—	—	—	
H'EE079	—		—	—	—	—	—	—	—	—	
H'EE07A	—		—	—	—	—	—	—	—	—	
H'EE07B	—		—	—	—	—	—	—	—	—	
H'EE07C	—		—	—	—	—	—	—	—	—	
H'EE07D	—		—	—	—	—	—	—	—	—	
H'EE07E	—		—	—	—	—	—	—	—	—	
H'EE07F	—		—	—	—	—	—	—	—	—	

Address (Low)	Register Name	Data Bus Width	Bit Names								Module Name
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFC0	SMR	8	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS1	CKS0	SCI channel 2
H'FFFC1	BRR	8									
H'FFFC2	SCR	8	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0	
H'FFFC3	TDR	8									
H'FFFC4	SSR	8	TDRE	RDRF	ORER	FER/ERS	PER	TEND	MPB	MPBT	
H'FFFC5	RDR	8									
H'FFFC6	SCMR	8	—	—	—	—	SDIR	SINV	—	SMIF	
H'FFFC7	Reserved area (access prohibited)										
H'FFFC8	—		—	—	—	—	—	—	—	—	
H'FFFC9	—		—	—	—	—	—	—	—	—	
H'FFFCA	—		—	—	—	—	—	—	—	—	
H'FFFCB	—		—	—	—	—	—	—	—	—	
H'FFFCC	—		—	—	—	—	—	—	—	—	
H'FFFCD	—		—	—	—	—	—	—	—	—	
H'FFFCE	—		—	—	—	—	—	—	—	—	
H'FFFCF	—		—	—	—	—	—	—	—	—	
H'FFFD0	P1DR	8	$P1_7$	$P1_6$	$P1_5$	$P1_4$	$P1_3$	$P1_2$	$P1_1$	$P1_0$	Port 1
H'FFFD1	P2DR	8	$P2_7$	$P2_6$	$P2_5$	$P2_4$	$P2_3$	$P2_2$	$P2_1$	$P2_0$	Port 2
H'FFFD2	P3DR	8	$P3_7$	$P3_6$	$P3_5$	$P3_4$	$P3_3$	$P3_2$	$P3_1$	$P3_0$	Port 3
H'FFFD3	P4DR	8	$P4_7$	$P4_6$	$P4_5$	$P4_4$	$P4_3$	$P4_2$	$P4_1$	$P4_0$	Port 4
H'FFFD4	P5DR	8	—	—	—	—	$P5_3$	$P5_2$	$P5_1$	$P5_0$	Port 5
H'FFFD5	P6DR	8	$P6_7$	$P6_6$	$P6_5$	$P6_4$	$P6_3$	$P6_2$	$P6_1$	$P6_0$	Port 6
H'FFFD6	P7DR	8	$P7_7$	$P7_6$	$P7_5$	$P7_4$	$P7_3$	$P7_2$	$P7_1$	$P7_0$	Port 7
H'FFFD7	P8DR	8	—	—	—	$P8_4$	$P8_3$	$P8_2$	$P8_1$	$P8_0$	Port 8
H'FFFD8	P9DR	8	—	—	$P9_5$	$P9_4$	$P9_3$	$P9_2$	$P9_1$	$P9_0$	Port 9
H'FFFD9	PADR	8	PA_7	PA_6	PA_5	PA_4	PA_3	PA_2	PA_1	PA_0	Port A
H'FFFDA	PBDR	8	PB_7	PB_6	PB_5	PB_4	PB_3	PB_2	PB_1	PB_0	Port B
H'FFFDB	—		—	—	—	—	—	—	—	—	
H'FFFDC	—		—	—	—	—	—	—	—	—	
H'FFFDD	—		—	—	—	—	—	—	—	—	
H'FFFDE	—		—	—	—	—	—	—	—	—	
H'FFFDF	—		—	—	—	—	—	—	—	—	