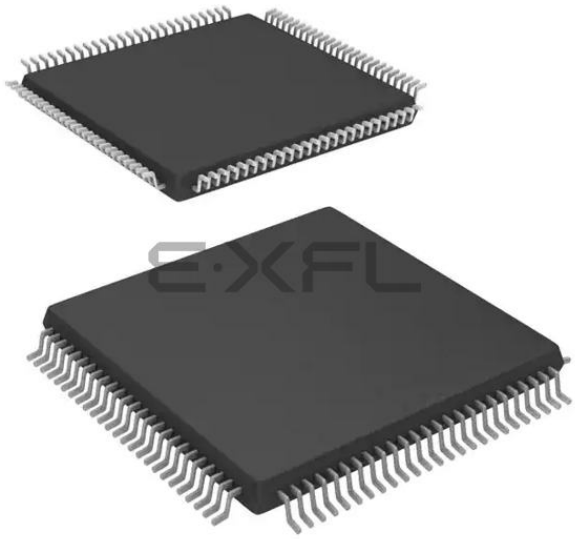

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8/300H
Core Size	16-Bit
Speed	25MHz
Connectivity	SCI, SmartCard
Peripherals	DMA, PWM, WDT
Number of I/O	70
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df3069rx25v

Bit 3—Priority Level A3 (IPRA3): Selects the priority level of WDT, DRAM interface, and A/D converter interrupt requests.

Bit 3 IPRA3	Description
0	WDT, DRAM interface, and A/D converter interrupt requests have priority level 0 (low priority) (Initial value)
1	WDT, DRAM interface, and A/D converter interrupt requests have priority level 1 (high priority)

Bit 2—Priority Level A2 (IPRA2): Selects the priority level of 16-bit timer channel 0 interrupt requests.

Bit 2 IPRA2	Description
0	16-bit timer channel 0 interrupt requests have priority level 0 (low priority) (Initial value)
1	16-bit timer channel 0 interrupt requests have priority level 1 (high priority)

Bit 1—Priority Level A1 (IPRA1): Selects the priority level of 16-bit timer channel 1 interrupt requests.

Bit 1 IPRA1	Description
0	16-bit timer channel 1 interrupt requests have priority level 0 (low priority) (Initial value)
1	16-bit timer channel 1 interrupt requests have priority level 1 (high priority)

Bit 0—Priority Level A0 (IPRA0): Selects the priority level of 16-bit timer channel 2 interrupt requests.

Bit 0 IPRA0	Description
0	16-bit timer channel 2 interrupt requests have priority level 0 (low priority) (Initial value)
1	16-bit timer channel 2 interrupt requests have priority level 1 (high priority)

Figure 5.5 shows the transitions among the above states.

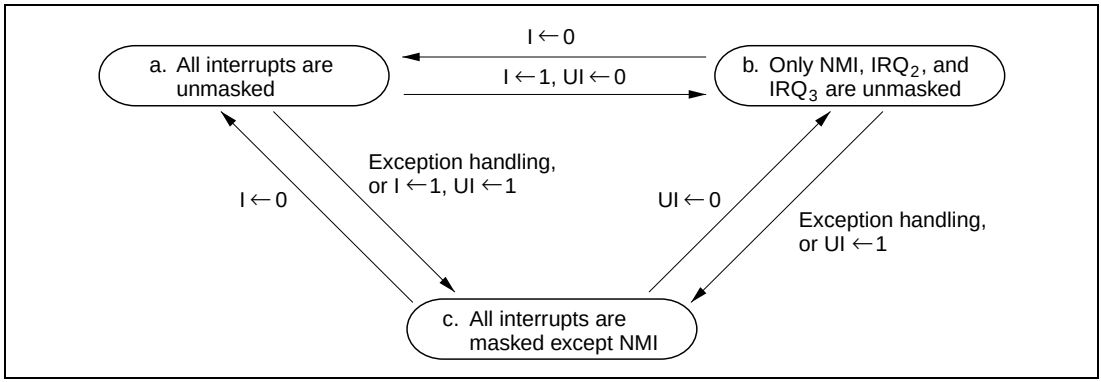


Figure 5.5 Interrupt Masking State Transitions (Example)

Figure 5.6 is a flowchart showing how interrupts are accepted when UE = 0.

- If an interrupt condition occurs and the corresponding interrupt enable bit is set to 1, an interrupt request is sent to the interrupt controller.
- When the interrupt controller receives one or more interrupt requests, it selects the highest-priority request, following the IPR interrupt priority settings, and holds other requests pending. If two or more interrupts with the same IPR setting are requested simultaneously, the interrupt controller follows the priority order shown in table 5.3.
- The interrupt controller checks the I bit. If the I bit is cleared to 0, the selected interrupt request is accepted regardless of its IPR setting, and regardless of the UI bit. If the I bit is set to 1 and the UI bit is cleared to 0, only NMI and interrupts with priority level 1 are accepted; interrupt requests with priority level 0 are held pending. If the I bit and UI bit are both set to 1, only NMI is accepted; all other interrupt requests are held pending.
- When an interrupt request is accepted, interrupt exception handling starts after execution of the current instruction has been completed.
- In interrupt exception handling, PC and CCR are saved to the stack area. The PC value that is saved indicates the address of the first instruction that will be executed after the return from the interrupt service routine.
- The I and UI bits are set to 1 in CCR, masking all interrupts except NMI.
- The vector address of the accepted interrupt is generated, and the interrupt service routine starts executing from the address indicated by the contents of the vector address.

Cautions: When using address update modes, the following points should be noted.

- When address update mode 2 is selected, the address in an internal space (on-chip memory or internal I/O) access cycle is not output externally.
- In order to secure address holding with respect to the rise of $\overline{RD}$, when address update mode 2 is used an external space read access must be completed within a single access cycle. For example, in a word access to 8-bit access space, the bus cycle is split into two as shown in figure 6.6, and so there is not a single access cycle. In this case, address holding is not guaranteed at the rise of $\overline{RD}$ between the first (even address) and second (odd address) access cycles (area inside the ellipse in the figure).

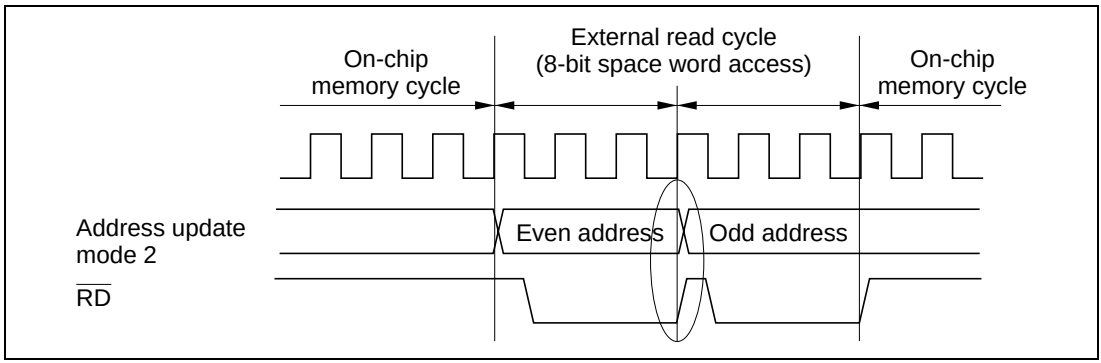


Figure 6.6 Example of Consecutive External Space Accesses in Address Update Mode 2

- When address update mode 2 is selected, in a DRAM space CAS-before-RAS (CBR) refresh cycle the previous address is retained (the area 2 start address is not output).

6.4.5 Basic Bus Control Signal Timing

8-Bit, Three-State-Access Areas

Figure 6.9 shows the timing of bus control signals for an 8-bit, three-state-access area. The upper data bus (D_{15} to D_8) is used in accesses to these areas. The $\overline{LWR}$ pin is always high. Wait states can be inserted.

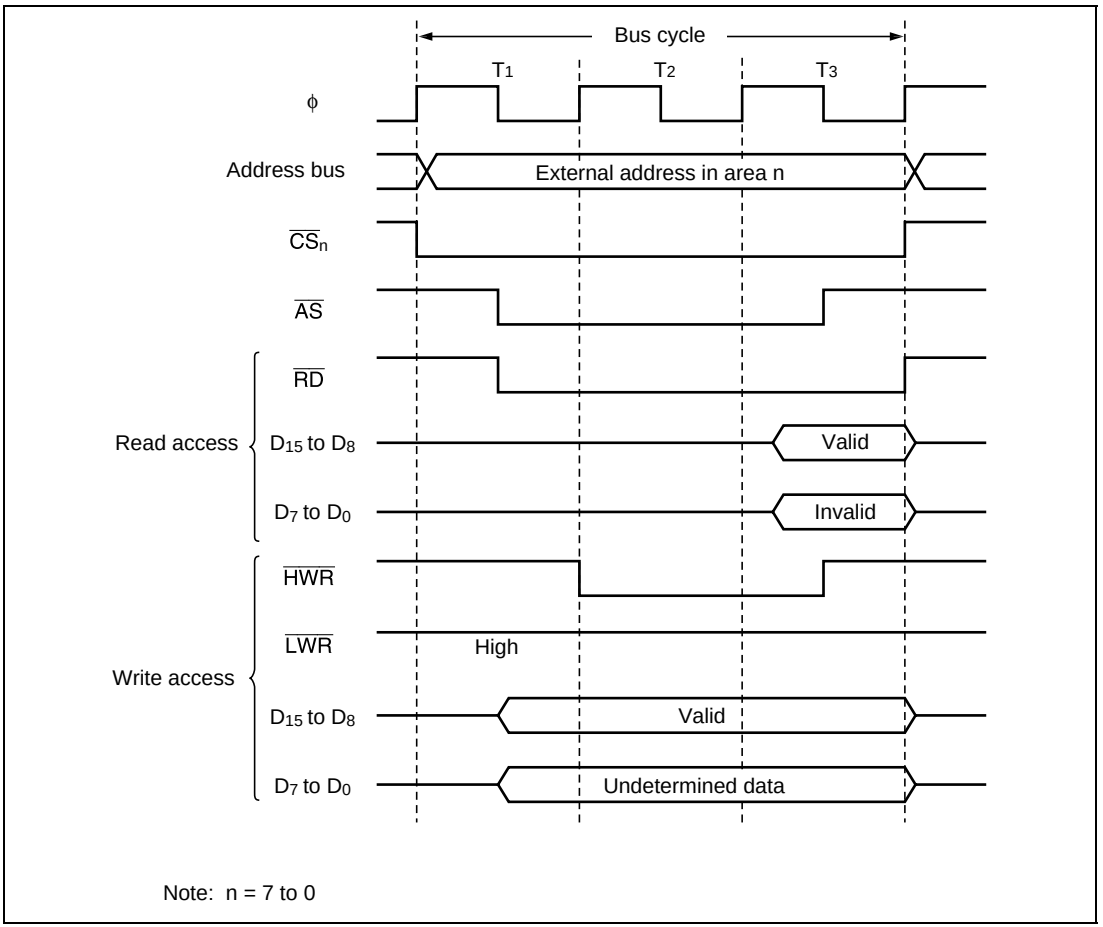


Figure 6.9 Bus Control Signal Timing for 8-Bit, Three-State-Access Area

When RAS down mode is selected, the CAS-before-RAS refresh function provided with this DRAM interface must always be used as the DRAM refreshing method. When a refresh operation is performed, the $\overline{RAS}$ signal goes high immediately beforehand. The refresh interval setting must be made so that the maximum DRAM $\overline{RAS}$ pulse width specification is observed.

When the self-refresh function is used, the RDM bit must be cleared to 0, and RAS up mode selected, before executing a SLEEP instruction in order to enter software standby mode. Select RAS down mode again after exiting software standby mode.

Note that RAS down mode cannot be used when $\overline{HWR}$ and $\overline{LWR}$ are selected for $\overline{UCAS}$ and $\overline{LCAS}$, a device other than DRAM is connected to external space, and $\overline{HWR}$ and $\overline{LWR}$ are used as write strobes.

- RAS Up Mode

  To select RAS up mode, clear the RDM bit to 0 in DRCRA. Each time access to DRAM space is interrupted and another space is accessed, the $\overline{RAS}$ signal returns to the high level. Burst operation is only performed if DRAM space is continuous. Figure 6.25 shows an example of the timing in RAS up mode.

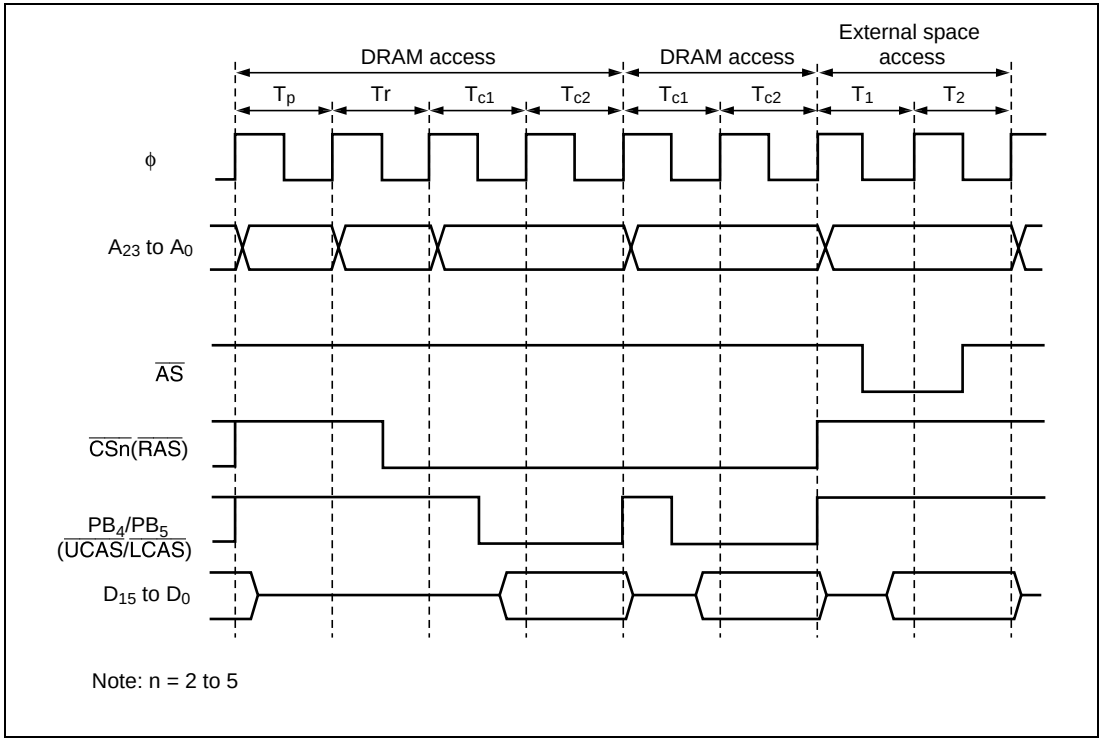


Figure 6.25 Example of Operation Timing in RAS Up Mode

8.5 Port 4

8.5.1 Overview

Port 4 is an 8-bit input/output port also used for data bus, with the pin configuration shown in figure 8.4. The pin functions differ depending on the operating mode.

In modes 1 to 5 (expanded modes), when the bus width control register (ABWCR) designates areas 0 to 7 all as 8-bit-access areas, the chip operates in 8-bit bus mode and port 4 is a generic input/output port. When at least one of areas 0 to 7 is designated as a 16-bit-access area, the chip operates in 16-bit bus mode and port 4 becomes part of the data bus. In mode 7 (single-chip mode), port 4 is a generic input/output port.

Port 4 has software-programmable built-in pull-up transistors.

Pins in port 4 can drive one TTL load and a 90-pF capacitive load. They can also drive a darlington transistor pair.

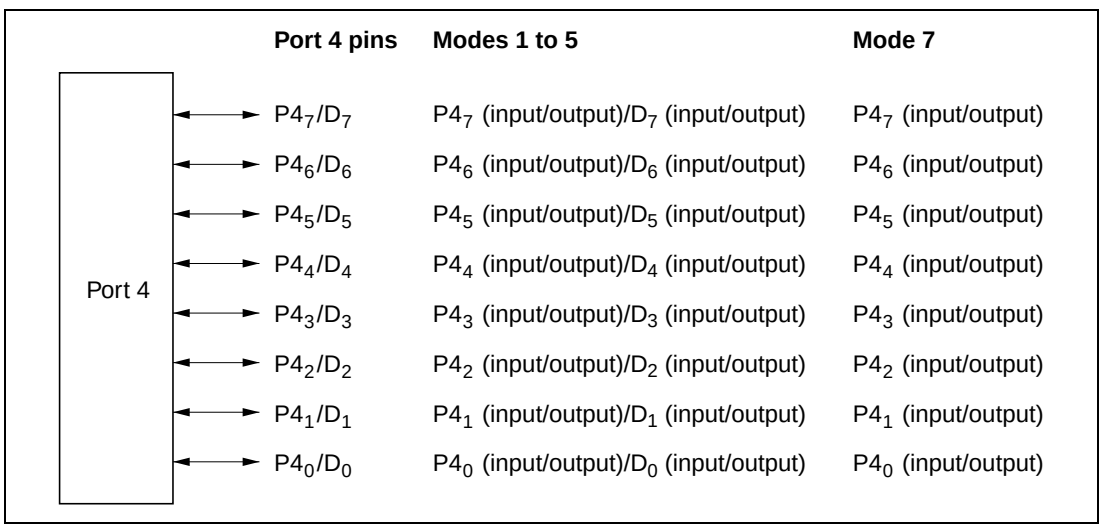


Figure 8.4 Port 4 Pin Configuration

Port 5 Data Direction Register (P5DDR): P5DDR is an 8-bit write-only register that can select input or output for each pin in port 5.

Bits 7 to 4 are reserved. They are fixed at 1, and cannot be modified.

Bit		7	6	5	4	3	2	1	0
		—	—	—	—	$P5_3DDR$	$P5_2DDR$	$P5_1DDR$	$P5_0DDR$
Modes 1 to 4	Initial value	1	1	1	1	1	1	1	1
	Read/Write	—	—	—	—	—	—	—	—
Modes 5 and 7	Initial value	1	1	1	1	0	0	0	0
	Read/Write	—	—	—	—	W	W	W	W

Reserved bits

Port 5 data direction 3 to 0
These bits select input or output for port 5 pins

Modes 1 to 4 (Expanded Modes with On-Chip ROM Disabled): P5DDR values are fixed at 1. Port 5 functions as an address bus.

Mode 5 (Expanded Mode with On-Chip ROM Enabled): Following a reset, port 5 is an input port. A pin in port 5 becomes an address output pin if the corresponding P5DDR bit is set to 1, and an input port if this bit is cleared to 0.

Mode 7 (Single-Chip Mode): Port 5 functions as an input/output port. A pin in port 5 becomes an output port if the corresponding P5DDR bit is set to 1, and an input port if this bit is cleared to 0.

In modes 1 to 4, P5DDR bits are always read as 1, and cannot be modified.

In modes 5 and 7, P5DDR is a write-only register. Its value cannot be read. All bits return 1 when read.

P5DDR is initialized to H'FF in modes 1 to 4, and to H'F0 in modes 5 and 7, by a reset and in hardware standby mode. In software standby mode it retains its previous setting. Therefore, if a transition is made to software standby mode while port 5 is functioning as an input/output port and a P5DDR bit is set to 1, the corresponding pin maintains its output state.

Pin	Pin Functions and Selection Method
PA_4/TP_4/ $TIOCA_1$	Bit PWM1 in TMDR, bits IOA2 to IOA0 in TIOR1, bit NDER4 in NDERA, and bit PA_4DDR select the pin function as follows.

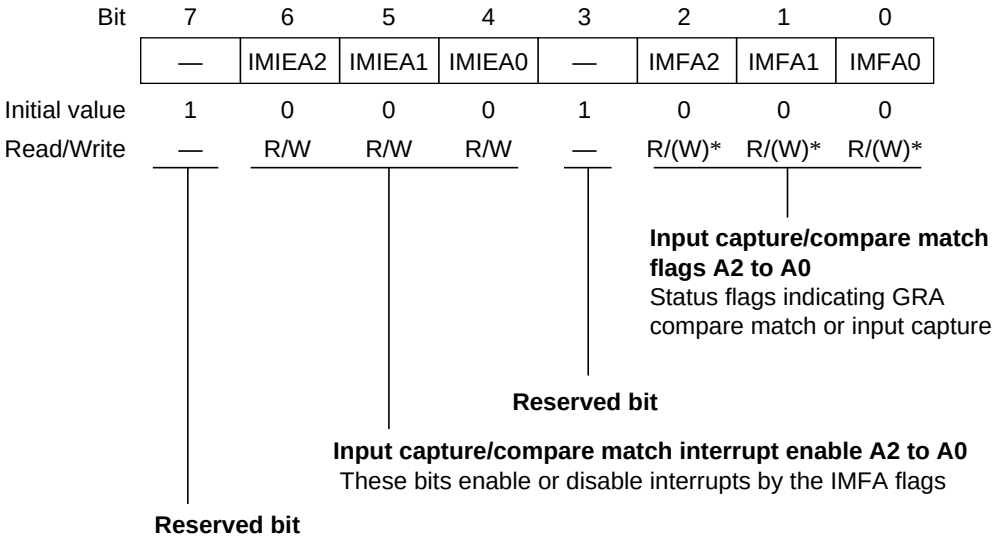
16-bit timer channel 1 settings	(1) in table below	(2) in table below		
PA_4DDR	—	0	1	1
NDER4	—	—	0	1
Pin function	$TIOCA_1$ output	PA_4 input	PA_4 output	TP_4 output
		$TIOCA_1$ input*		

Note: * $TIOCA_1$ input when IOA2 = 1.

16-bit timer channel 1 settings	(2)	(1)		(2)	(1)
PWM1	0				1
IOA2	0			1	—
IOA1	0	0	1	—	—
IOA0	0	1	—	—	—

9.2.4 Timer Interrupt Status Register A (TISRA)

TISRA is an 8-bit readable/writable register that indicates GRA compare match or input capture and enables or disables GRA compare match and input capture interrupt requests.



Note: * Only 0 can be written, to clear the flag.

TISRA is initialized to H'88 by a reset and in standby mode.

Bit 7—Reserved: This bit cannot be modified and is always read as 1.

Bit 6—Input Capture/Compare Match Interrupt Enable A2 (IMIEA2): Enables or disables the interrupt requested by the IMFA2 when IMFA2 flag is set to 1.

Bit 6 IMIEA2	Description	
0	IMIA2 interrupt requested by IMFA2 flag is disabled	(Initial value)
1	IMIA2 interrupt requested by IMFA2 flag is enabled	

- Examples of waveform output

  Figure 9.18 shows examples of 0 and 1 output. 16TCNT operates as a free-running counter, 0 output is selected for compare match A, and 1 output is selected for compare match B. When the pin is already at the selected output level, the pin level does not change.

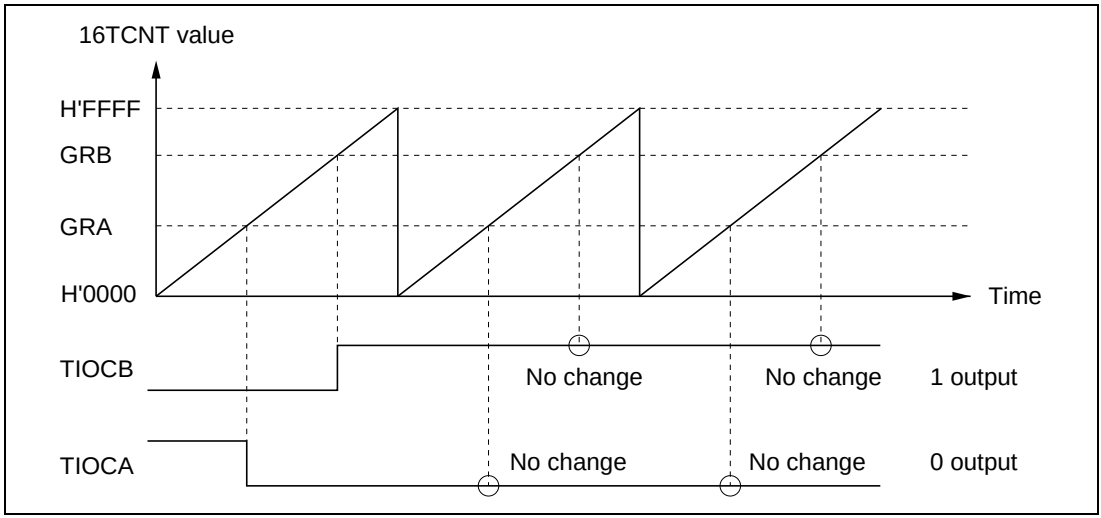


Figure 9.18 0 and 1 Output (TOA = 1, TOB = 0)

Figure 9.19 shows examples of toggle output. 16TCNT operates as a periodic counter, cleared by compare match B. Toggle output is selected for both compare match A and B.

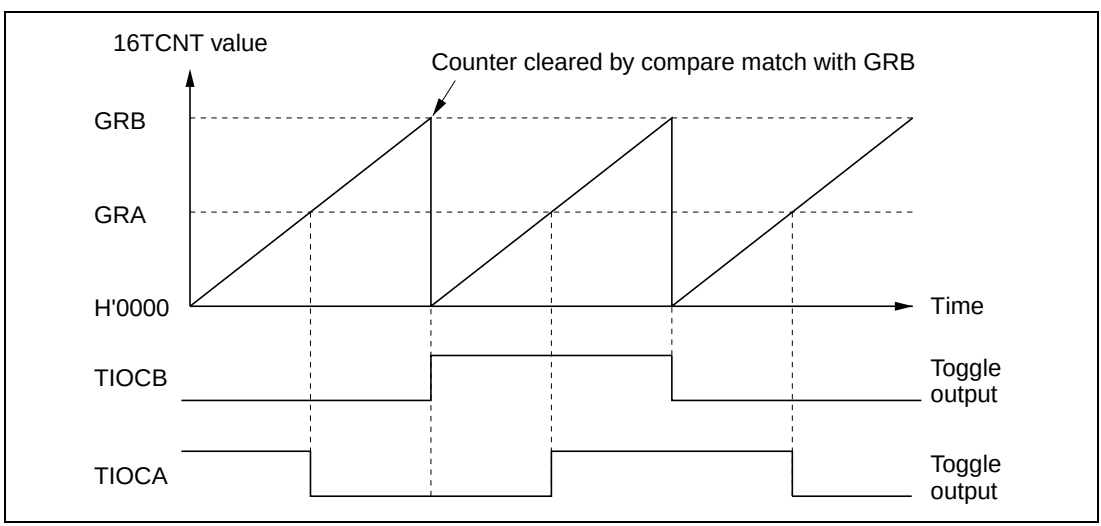


Figure 9.19 Toggle Output (TOA = 1, TOB = 0)

10.1.3 Pin Configuration

Table 10.1 summarizes the input/output pins of the 8-bit timer module.

Table 10.1 8-Bit Timer Pins

Group	Channel	Name	Abbreviation	I/O	Function
0	0	Timer output	TMO_0	Output	Compare match output
		Timer clock input	TCLKC	Input	Counter external clock input
	1	Timer input/output	$TMIO_1$	I/O	Compare match output/input capture input
		Timer clock input	TCLKA	Input	Counter external clock input
1	2	Timer output	TMO_2	Output	Compare match output
		Timer clock input	TCLKD	Input	Counter external clock input
	3	Timer input/output	$TMIO_3$	I/O	Compare match output/input capture input
		Timer clock input	TCLKB	Input	Counter external clock input

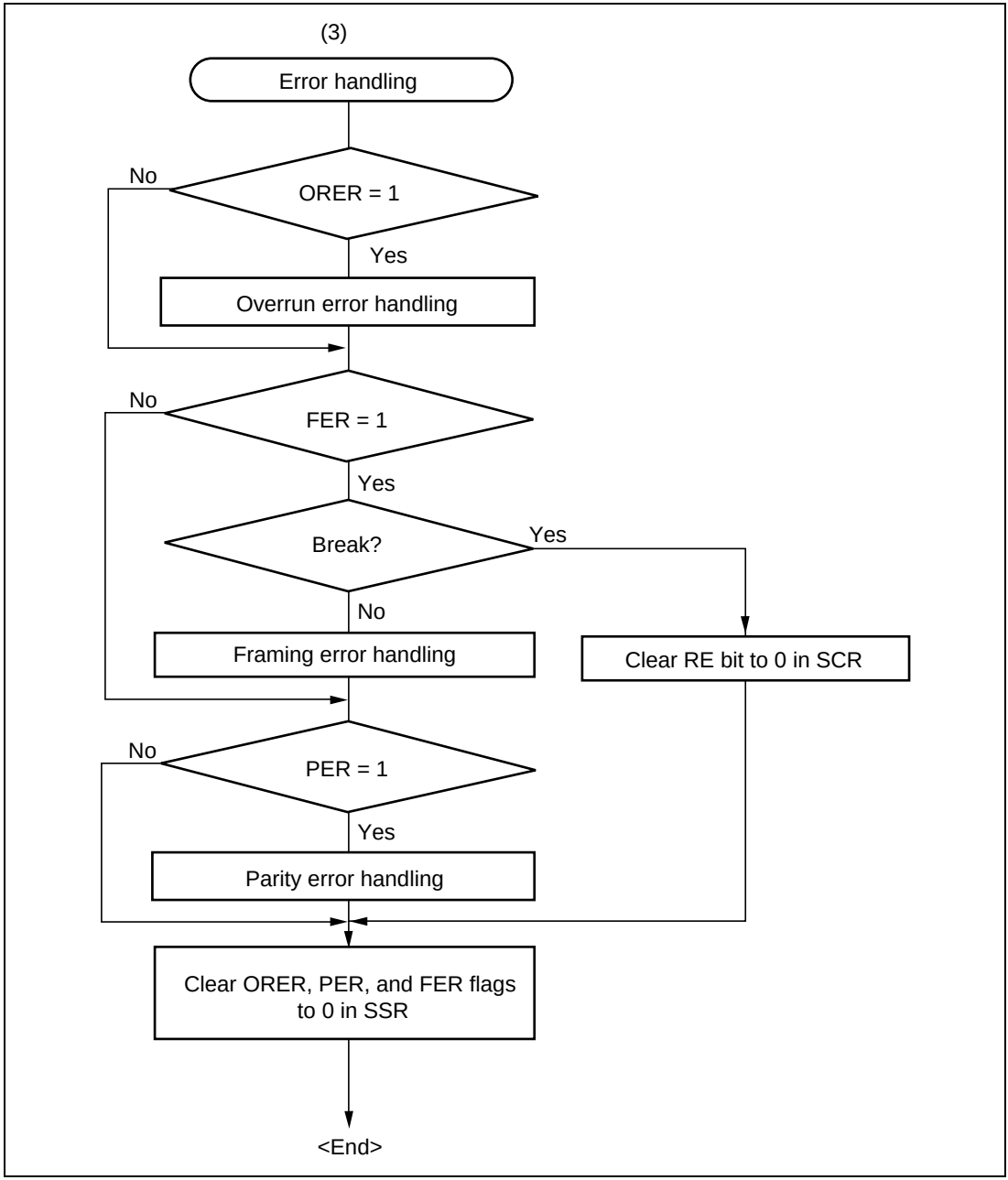


Figure 13.7 Sample Flowchart for Receiving Serial Data (2)

Table 18.4 (2) Parameter Configuration

Name	Abbreviation	R/W	Initial Value	Address	Access Size
Download pass/fail result	DPFR	R/W	Undefined	On-chip RAM*	8, 16, 32
Flash pass/fail result	FPFR	R/W	Undefined	R0L of CPU	8, 16, 32
Flash multipurpose address area	FMPAR	R/W	Undefined	ER1 of CPU	8, 16, 32
Flash multipurpose data destination area	FMPDR	R/W	Undefined	ER0 of CPU	8, 16, 32
Flash erase block select	FEBS	R/W	Undefined	ER0 of CPU	8, 16, 32
Flash program and erase frequency control	FPEFEQ	R/W	Undefined	ER0 of CPU	8, 16, 32
Flash user branch address set parameter	FUBRA	R/W	Undefined	ER1 of CPU	8, 16, 32

Note: * One byte of the start address in the on-chip RAM area specified by FTDAR is valid.

18.8 Switching between User MAT and User Boot MAT

It is possible to alternate between the user MAT and user boot MAT. However, the following procedure is required because these MATs are allocated to address 0.
(Switching to the user boot MAT disables programming and erasing. Programming of the user boot MAT should take place in boot mode or PROM mode.)

(1) MAT switching by the FMATS register should always be executed from the on-chip RAM.

(2) To ensure that the MAT that has been switched to is accessible, execute 4 NOP instructions in the on-chip RAM immediately before or after writing to the FMATS register of the on-chip RAM (this prevents access to the flash memory during MAT switching).

(3) If an interrupt has occurred during switching, there is no guarantee of which memory MAT is being accessed. Always mask the maskable interrupts before switching between MATs. In addition, configure the system so that NMI interrupts do not occur during MAT switching.

(4) After the MATs have been switched, take care because the interrupt vector table will also have been switched. If interrupt processing is to be the same before and after MAT switching, transfer the interrupt-processing routines to the on-chip RAM, and use the settings of the FVACR and FVADR registers to place the interrupt-vector table in the on-chip RAM .

(5) Memory sizes of the user MAT and user boot MAT are different. When accessing the user boot MAT, do not access addresses above the top of its 8-kbyte memory space. If access goes beyond the 8-kbyte space, the values read are undefined.

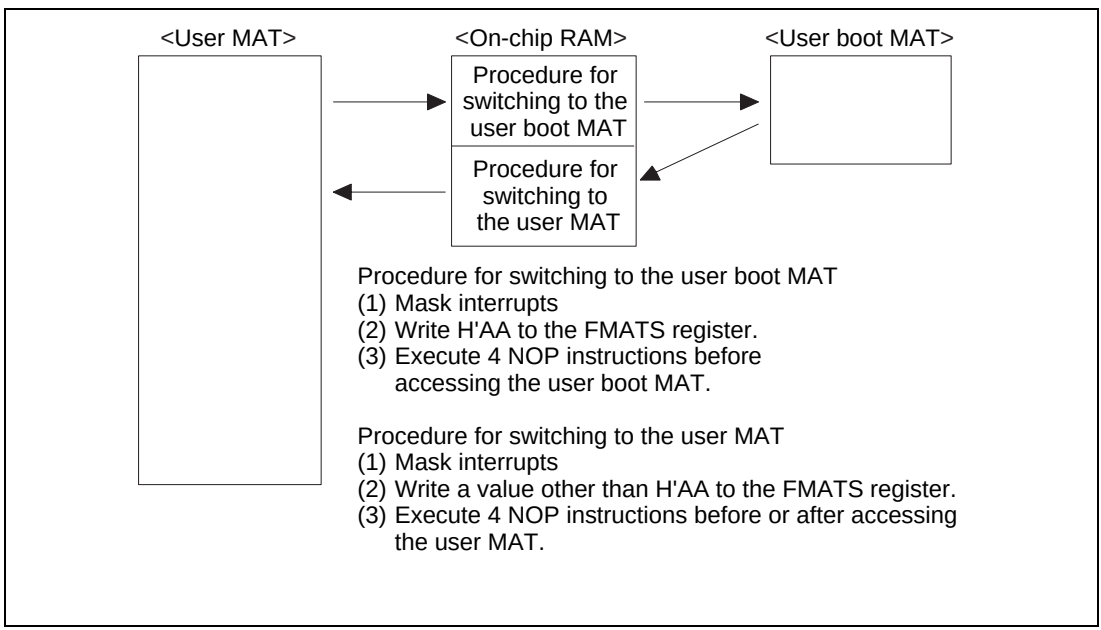


Figure 18.20 Switching between the User MAT and User Boot MAT

21.1 Electrical Characteristics of HD64F3069RF25 and HD64F3069RTE25

21.1.1 Absolute Maximum Ratings

Table 21.1 lists the absolute maximum ratings.

Table 21.1 Absolute Maximum Ratings

Item	Symbol	Value	Unit
Power supply voltage	V_{CC}*[1]	–0.3 to +7.0	V
Input voltage (FWE)*[2]	V_{in}	–0.3 to V_{CC} +0.3	V
Input voltage (except for port 7)*[2]	V_{in}	–0.3 to V_{CC} +0.3	V
Input voltage (port 7)	V_{in}	–0.3 to AV_{CC} +0.3	V
Reference voltage	V_{REF}	–0.3 to AV_{CC} +0.3	V
Analog power supply voltage	AV_{CC}	–0.3 to +7.0	V
Analog input voltage	V_{AN}	–0.3 to AV_{CC} +0.3	V
Operating temperature	T_{opr}	Regular specifications: –20 to +75*[3]	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution: Permanent damage to the chip may result if absolute maximum ratings are exceeded.

Notes: 1. Do not apply the power supply voltage to the V_{CL} pin. Connect an external capacitor between this pin and GND.

2. 12 V must not be applied to any pin, as this may cause permanent damage to the device.

3. The operating temperature range for flash memory programming/erasing is T_a = 0 to +75°C (Regular specifications).

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Reference current	During A/D conversion	AI_{CC}	—	0.45	0.8	mA	
	During A/D and D/A conversion		—	1.8	3.0	mA	
	Idle		—	0.05	5.0	µA	DASTE = 0
RAM standby voltage		V_{RAM}	3.0	—	—	V	
V_{CL} output voltage*[5]	Normal operation	V_{CL}	1.5	1.9	2.3	V	V_{CC} = 5.0V T_a = 25°C
V_{CC} start voltage*[6]		$V_{CC\ START}$	—	0	0.8	V	
V_{CC} rise rate*[6]		SV_{CC}	0.05	—	—	V/ms	

Notes: 1. If the A/D converter is not used, do not leave the AV_{CC}, V_{REF}, and AV_{SS} pins open. Connect AV_{CC} and V_{REF} to V_{CC}, and connect AV_{SS} to V_{SS}.

2. Current dissipation values are for V_{IH} min = V_{CC} – 0.5 V and V_{IL} max = 0.5 V with all output pins unloaded and the on-chip MOS pull-up transistors in the off state.

3. I_{CC} max. (normal operation) = 15 (mA) + 0.15 (mA/(MHz × V)) × V_{CC} × f
   I_{CC} max. (sleep mode) = 15 (mA) + 0.13 (mA/(MHz × V)) × V_{CC} × f
   I_{CC} max. (sleep mode + module standby mode)
   = 15 (mA) + 0.07 (mA/(MHz × V)) × V_{CC} × f
   The Typ values for power consumption are reference values.

4. Sum of current dissipation in normal operation and current dissipation in program/erase operations.

5. This value is applied when the external capacitor of 0.1 µF is connected. This characteristic does not specify the permissible range of voltage input from the external circuit but specifies the voltage output by the LSI.

6. These characteristics are applied under the condition in which the $\overline{RES}$ pin goes low when powering on.

Mnemonic	Operand Size	Addressing Mode and Instruction Length (bytes)									Operation	Condition Code						No. of States*1	
		#xx	Rn	@ERn	@(d, ERn)	@–ERn/@ERn+	@aa	@(d, PC)	@@aa	|		I	H	N	Z	V	C	Normal	Advanced
BLD #xx:3, @ERd	B			4							(#xx:3 of @ERd) → C	—	—	—	—	—	↕	6	
BLD #xx:3, @aa:8	B						4				(#xx:3 of @aa:8) → C	—	—	—	—	—	↕	6	
BILD #xx:3, Rd	B		2								¬ (#xx:3 of Rd8) → C	—	—	—	—	—	↕	2	
BILD #xx:3, @ERd	B			4							¬ (#xx:3 of @ERd) → C	—	—	—	—	—	↕	6	
BILD #xx:3, @aa:8	B						4				¬ (#xx:3 of @aa:8) → C	—	—	—	—	—	↕	6	
BST #xx:3, Rd	B		2								C → (#xx:3 of Rd8)	—	—	—	—	—	—	2	
BST #xx:3, @ERd	B			4							C → (#xx:3 of @ERd24)	—	—	—	—	—	—	8	
BST #xx:3, @aa:8	B						4				C → (#xx:3 of @aa:8)	—	—	—	—	—	—	8	
BIST #xx:3, Rd	B		2								¬ C → (#xx:3 of Rd8)	—	—	—	—	—	—	2	
BIST #xx:3, @ERd	B			4							¬ C → (#xx:3 of @ERd24)	—	—	—	—	—	—	8	
BIST #xx:3, @aa:8	B						4				¬ C → (#xx:3 of @aa:8)	—	—	—	—	—	—	8	
BAND #xx:3, Rd	B		2								C∧(#xx:3 of Rd8) → C	—	—	—	—	—	↕	2	
BAND #xx:3, @ERd	B			4							C∧(#xx:3 of @ERd24) → C	—	—	—	—	—	↕	6	
BAND #xx:3, @aa:8	B						4				C∧(#xx:3 of @aa:8) → C	—	—	—	—	—	↕	6	
BIAND #xx:3, Rd	B		2								C∧ ¬ (#xx:3 of Rd8) → C	—	—	—	—	—	↕	2	
BIAND #xx:3, @ERd	B			4							C∧ ¬ (#xx:3 of @ERd24) → C	—	—	—	—	—	↕	6	
BIAND #xx:3, @aa:8	B						4				C∧ ¬ (#xx:3 of @aa:8) → C	—	—	—	—	—	↕	6	
BOR #xx:3, Rd	B		2								C∨(#xx:3 of Rd8) → C	—	—	—	—	—	↕	2	
BOR #xx:3, @ERd	B			4							C∨(#xx:3 of @ERd24) → C	—	—	—	—	—	↕	6	
BOR #xx:3, @aa:8	B						4				C∨(#xx:3 of @aa:8) → C	—	—	—	—	—	↕	6	
BIOR #xx:3, Rd	B		2								C∨ ¬ (#xx:3 of Rd8) → C	—	—	—	—	—	↕	2	
BIOR #xx:3, @ERd	B			4							C∨ ¬ (#xx:3 of @ERd24) → C	—	—	—	—	—	↕	6	
BIOR #xx:3, @aa:8	B						4				C∨ ¬ (#xx:3 of @aa:8) → C	—	—	—	—	—	↕	6	
BXOR #xx:3, Rd	B		2								C⊕(#xx:3 of Rd8) → C	—	—	—	—	—	↕	2	
BXOR #xx:3, @ERd	B			4							C⊕(#xx:3 of @ERd24) → C	—	—	—	—	—	↕	6	
BXOR #xx:3, @aa:8	B						4				C⊕(#xx:3 of @aa:8) → C	—	—	—	—	—	↕	6	
BIXOR #xx:3, Rd	B		2								C⊕ ¬ (#xx:3 of Rd8) → C	—	—	—	—	—	↕	2	
BIXOR #xx:3, @ERd	B			4							C⊕ ¬ (#xx:3 of @ERd24) → C	—	—	—	—	—	↕	6	
BIXOR #xx:3, @aa:8	B						4				C⊕ ¬ (#xx:3 of @aa:8) → C	—	—	—	—	—	↕	6	

A.3 Number of States Required for Execution

The tables in this section can be used to calculate the number of states required for instruction execution by the H8/300H CPU. Table A.4 indicates the number of instruction fetch, data read/write, and other cycles occurring in each instruction. Table A.3 indicates the number of states required per cycle according to the bus size. The number of states required for execution of an instruction can be calculated from these two tables as follows:

Number of states = $I \bullet S_I + J \bullet S_J + K \bullet S_K + L \bullet S_L + M \bullet S_M + N \bullet S_N$

Examples of Calculation of Number of States Required for Execution

Examples: Advanced mode, stack located in external address space, on-chip supporting modules accessed with 8-bit bus width, external devices accessed in three states with one wait state and 16-bit bus width.

BSET #0, @FFFFC7:8

From table A.4, I = L = 2 and J = K = M = N = 0
From table A.3, $S_I = 4$ and $S_L = 3$
Number of states = $2 \bullet 4 + 2 \bullet 3 = 14$

JSR @@30

From table A.4, I = J = K = 2 and L = M = N = 0
From table A.3, $S_I = S_J = S_K = 4$
Number of states = $2 \bullet 4 + 2 \bullet 4 + 2 \bullet 4 = 24$

B.2 Addresses (cont)

Address (Low)	Register Name	Data Bus Width	Bit Names								Module Name
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFEE0	SMR	8	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS1	CKS0	SCI channel 0
H'FFEE1	BRR	8									
H'FFEE2	SCR	8	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0	
H'FFEE3	TDR	8									
H'FFEE4	SSR	8	TDRE	RDRF	ORER	FER/ERS	PER	TEND	MPB	MPBT	
H'FFEE5	RDR	8									
H'FFEE6	SCMR	8	—	—	—	—	SDIR	SINV	—	SMIF	
H'FFEE7	Reserved area (access prohibited)										
H'FFEE8	SMR	8	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS1	CKS0	SCI channel 1
H'FFEE9	BRR	8									
H'FFEEA	SCR	8	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0	
H'FFEEB	TDR	8									
H'FFEEC	SSR	8	TDRE	RDRF	ORER	FER/ERS	PER	TEND	MPB	MPBT	
H'FFEED	RDR	8									
H'FFEEE	SCMR	8	—	—	—	—	SDIR	SINV	—	SMIF	
H'FFEEF	Reserved area (access prohibited)										
H'FFEF0	SMR	8	C/$\overline{A}$	CHR	PE	O/$\overline{E}$	STOP	MP	CKS1	CKS0	SCI channel 2
H'FFEF1	BRR	8									
H'FFEF2	SCR	8	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0	
H'FFEF3	TDR	8									
H'FFEF4	SSR	8	TDRE	RDRF	ORER	FER/ERS	PER	TEND	MPB	MPBT	
H'FFEF5	RDR	8									
H'FFEF6	SCMR	8	—	—	—	—	SDIR	SINV	—	SMIF	
H'FFEF7	Reserved area (access prohibited)										
H'FFEF8	TPMR	8	—	—	—	—	G3NOV	G2NOV	G1NOV	G0NOV	TPC
H'FFEF9	TPCR	8	G3CMS1	G3CMS0	G2CMS1	G2CMS0	G1CMS1	G1CMS0	G0CMS1	G0CMS0	
H'FFEFA	NDERB	8	NDER15	NDER14	NDER13	NDER12	NDER11	NDER10	NDER9	NDER8	
H'FFEFB	NDERA	8	NDER7	NDER6	NDER5	NDER4	NDER3	NDER2	NDER1	NDER0	
H'FFEFC	NDRB*	8	NDR15	NDR14	NDR13	NDR12	NDR11	NDR10	NDR9	NDR8	
			NDR15	NDR14	NDR13	NDR12	—	—	—	—	
H'FFEFD	NDRA*	8	NDR7	NDR6	NDR5	NDR4	NDR3	NDR2	NDR1	NDR0	
			NDR7	NDR6	NDR5	NDR4	—	—	—	—	
H'FFEFE	NDRB*	8	—	—	—	—	—	—	—	—	
			—	—	—	—	NDR11	NDR10	NDR9	NDR8	
H'FFEFF	NDRA*	8	—	—	—	—	—	—	—	—	
			—	—	—	—	NDR3	NDR2	NDR1	NDR0	

Bit	7	6	5	4	3	2	1	0
	MXC1	MXC0	CSEL	RCYCE	—	TPC	RCW	RLW
Initial value	0	0	0	0	1	0	0	0
Read/Write	R/W	R/W	R/W	R/W	—	R/W	R/W	R/W

Refresh cycle wait control

0	Wait state (T_{RW}) insertion is disabled
1	1 wait state (T_{RW}) is inserted

$\overline{RAS}$-$\overline{CAS}$ wait

0	Wait state (T_{rw}) insertion is disabled
1	1 wait state (T_{rw}) is inserted

TP cycle control

0	1-state precharge cycle is inserted
1	2-state precharge cycle is inserted

Refresh cycle enable

0	Refresh cycles are disabled
1	DRAM refresh cycles are enabled

$\overline{CAS}$ output pin select

0	PB4 and PB5 selected as $\overline{UCAS}$ and $\overline{LCAS}$ output pins
1	$\overline{HWR}$ and $\overline{LWR}$ selected as $\overline{UCAS}$ and $\overline{LCAS}$ output pins

Multiplex control 1 and 0

MXC1	MXC0	Description
0	0	Column address: 8 bits Compared address: Modes 1, 2 — 8-bit access space — A_{19} to A_8 16-bit access space — A_{19} to A_9 Modes 3, 4, 5 — 8-bit access space — A_{23} to A_8 16-bit access space — A_{23} to A_9
	1	Column address: 9 bits Compared address: Modes 1, 2 — 8-bit access space — A_{19} to A_9 16-bit access space — A_{19} to A_{10} Modes 3, 4, 5 — 8-bit access space — A_{23} to A_9 16-bit access space — A_{23} to A_{10}
1	0	Column address: 10 bits Compared address: Modes 1, 2 — 8-bit access space — A_{19} to A_{10} 16-bit access space — A_{19} to A_{11} Modes 3, 4, 5 — 8-bit access space — A_{23} to A_{10} 16-bit access space — A_{23} to A_{11}
	1	Illegal setting