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Program Memory Type	-
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	-
Data Converters	-
Oscillator Type	-
Operating Temperature	-
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aducm3027bcpz-rl

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REVISION HISTORY

3/2017—Revision 0: Initial Version

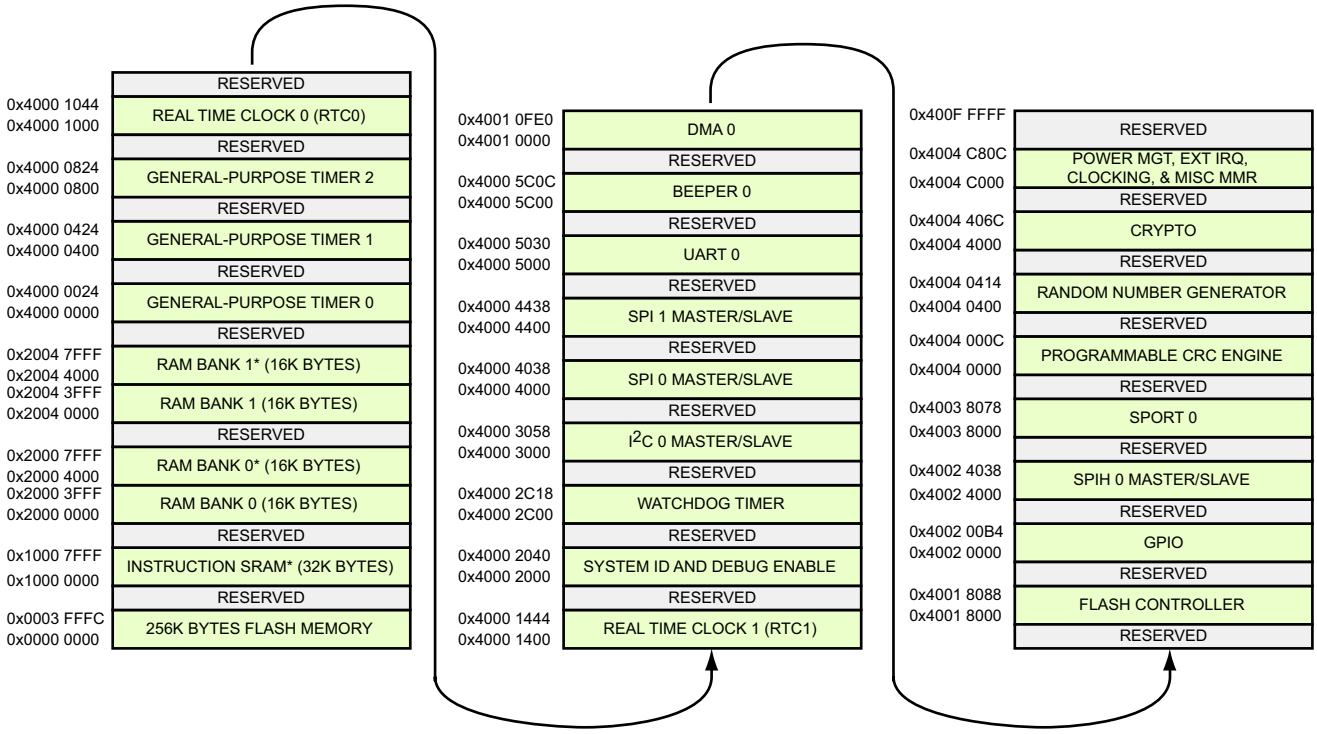

Figure 2. ADuCM3027/ADuCM3029 Memory Map

Cache Controller

The ADuCM3027/ADuCM3029 MCUs have an optional 4 KB instruction cache. In certain applications, enabling the cache and executing the code can result in lower power consumption than operating directly from flash. When the cache controller is enabled, 4 KB of instruction SRAM is reserved as cache memory. In hibernate mode, the cache memory is not retained.

SYSTEM AND INTEGRATION FEATURES

The ADuCM3027/ADuCM3029 MCUs provide several features that ease system integration.

Reset

There are four types of resets: external, power-on, watchdog timeout, and software system reset. The software system reset is provided as part of the Cortex-M3 core.

The $\overline{\text{SYS\_HWRST}}$ pin is toggled to perform a hardware reset.

Booting

The ADuCM3027/ADuCM3029 MCUs support two boot modes: booting from internal flash and upgrading software through UART download. If the SYS_BMODE0 pin (GPIO17) is pulled low during power-up or a hard reset, the MCU enters into serial download mode.

In this mode, an on-chip loader routine initiates in the kernel, which configures the UART port and communicates with the host to manage the firmware upgrade via a specific serial download protocol.

Table 2. Boot Modes

Boot Mode	Description
0	UART download mode.
1	Flash boot. Boot from integrated flash memory.

Power Management

The ADuCM3027/ADuCM3029 MCUs have an integrated power management system that optimizes performance and extends battery life of the devices.

The power management system consists of the following:

- Integrated 1.2 V low dropout regulator (LDO) and optional capacitive buck regulator
- Integrated power switches for low standby current in hibernate and shutdown modes

Cryptographic Accelerator

The cryptographic accelerator is a 32-bit APB DMA capable peripheral. There are two 32-bit buffers provided for data input/output operations. These buffers read in or read out 128 bits in four data accesses. Big endian and little endian data formats are supported, as are the following modes:

- Electronic code book (ECB) mode—AES mode
- Counter (CTR) mode
- Cipher block chaining (CBC) mode
- Message authentication code (MAC) mode
- Cipher block chaining-message authentication code (CCM/CCM*) mode
- SHA-256 modes

True Random Number Generator (TRNG)

The TRNG is used during operations where nondeterministic values are required. This can include generating challenges for secure communication or keys for an encrypted communication channel. The generator can run multiple times to generate a sufficient number of bits for the strength of the intended operation. The TRNG can seed a deterministic random bit generator.

Reliability and Robustness Features

The ADuCM3027/ADuCM3029 MCUs provide a number of features that can enhance or help achieve certain levels of system safety and reliability. While the level of safety is mainly dominated by system considerations, the following features are provided to enhance robustness:

- ECC enabled flash memory. The entire flash array can be protected to either correct single-bit errors or detect two-bit errors per 64-bit flash data (enabled by default).
- Multiparity bit protected SRAM. Each word of the SRAM and cache memory is protected by multiple parity bits to allow detection of random soft errors.
- Software watchdog. The on-chip watchdog timer can provide software-based supervision of the ADuCM3027/ADuCM3029.

Cyclic Redundancy Check (CRC) Accelerator

The CRC accelerator computes the CRC for a block of memory locations. The exact memory location can be in the SRAM, flash, or any combination of MMRs. The CRC accelerator generates a checksum that can be compared with an expected signature.

The main features of the CRC include the following:

- Generates a CRC signature for a block of data.
- Supports programmable polynomial length of up to 32 bits.
- Operates on 32 bits of data at a time.
- Supports MSB first and LSB first CRC implementations.
- Various data mirroring capabilities.
- Initial seed to be programmed by user.
- DMA controller (memory to memory transfer) used for data transfer to offload the MCU.

Programmable GPIOs

The ADuCM3027/ADuCM3029 MCUs have 44 and 36 GPIO pins in the LFCSP and WLCSP packages, respectively, with multiple, configurable functions defined by user code. They can be configured as an input/output and have programmable pull-up resistors. All GPIO pins are functional over the full supply range.

In deep sleep mode, GPIO pins retain their state. On reset, they tristate.

Timers

The ADuCM3027/ADuCM3029 MCUs have three general-purpose timers and a watchdog timer.

General-Purpose Timers

The ADuCM3027/ADuCM3029 MCUs have three identical general-purpose timers, each with a 16-bit up and down counter. The up and down counter can be clocked from one of four user selectable clock sources. Any selected clock source can be scaled down using a prescaler of 1, 16, 64, or 256.

Watchdog Timer (WDT)

The WDT is a 16-bit count down timer with a programmable prescaler. The prescaler source is selectable and can be scaled by a factor of 1, 16, or 256. The watchdog timer is clocked by the 32 kHz on-chip oscillator (LFOSC) and recovers from an illegal software state. The WDT requires periodic servicing to prevent it from forcing a reset or interrupt to the MCU.

Analog-to-Digital Converter (ADC) Subsystem

The ADuCM3027/ADuCM3029 MCUs integrate a 12-bit SAR ADC with up to eight external channels. Conversions can be performed in single or autocycle mode. In single mode, the ADC can be configured to convert on a particular channel by selecting one of the channels. Autocycle mode is provided to reduce MCU overhead of sampling and reading individual channel registers. The ADC can also be used for temperature sensing and measuring battery voltage using dedicated channels. Temperature sensing and battery monitoring cannot be included with external channels in autocycle mode.

A digital comparator triggers an interrupt if ADC input is above or below a programmable threshold. The ADC0_VIN0, ADC0_VIN1, ADC0_VIN2, and ADC0_VIN3 input channels can be used with the digital comparator.

Use the ADC in DMA mode to reduce MCU overhead by moving ADC results directly into SRAM with a single interrupt asserted when the required number of ADC conversions has been completely logged to memory.

The main features of the ADC subsystem include the following:

- 12-bit resolution.
- Programmable ADC update rate from 10 KSPS to 1.8 MSPS.
- Integrated input multiplexer that supports up to eight channels.
- Temperature sensing support.
- Battery monitoring support.
- Software selectable on-chip reference voltage generation—1.25 V and 2.5 V.
- Software selectable internal or external reference.
- Autocycle mode—ability to automatically select a sequence of input channels for conversion.
- Averaging function—converted data on single or multiple channels can be averaged up to 256 samples.
- Alert function—internal digital comparator for ADC0_VIN0, ADC0_VIN1, ADC0_VIN2, and ADC0_VIN3 channels. An interrupt is generated if the digital comparator detects an ADC result above or below a user defined threshold.
- Dedicated DMA channel support.
- Each channel, including temperature sensor and battery monitoring, has a data register for conversion result.

Clocking

The ADuCM3027/ADuCM3029 MCUs have the following clocking options:

- 26 MHz
  - Internal oscillator—HFOSC (26 MHz)
  - External crystal oscillator—HFXTAL (26 MHz or 16 MHz)
  - GPIO clock in—SYS_CLKIN
- 32 kHz
  - Internal oscillator—LFOSC
  - External crystal oscillator—LFXTAL

The clock options have software configurability with the following exceptions:

- HFOSC cannot be disabled when using an internal buck regulator.
- LFOSC cannot be disabled even if using LFXTAL.

Real-Time Clock (RTC)

The ADuCM3027/ADuCM3029 MCUs have two real-time clock blocks—RTC0 and RTC1 (FLEX_RTC). The clock blocks share a low power crystal oscillation circuit that operates in conjunction with a 32,768 Hz external crystal.

The RTC has an alarm that interrupts the core when the programmed alarm value matches the RTC count. The software enables and configures the RTC.

The RTC also has a digital trim capability to allow a positive or negative adjustment to the RTC count at fixed intervals.

The FLEX_RTC supports SensorStrobe mechanism. Using this mechanism, the ADuCM3027/ADuCM3029 MCUs can be used as a programmable clock generator in some power modes, including hibernate mode. In this way, the external sensors can have their timing domains mastered by the ADuCM3027/ADuCM3029 MCUs, as SensorStrobe can output a programmable divider from the FLEX_RTC, which can operate up to a resolution of 30.7 µs. The sensors and MCU are in sync, which removes the need for additional resampling of data to time align it.

In the absence of this mechanism,

- The external sensor uses an RC oscillator (~±30% typical variation). The MCU must sample the data and resample it on the time domain of the MCU before using it.

Or

- The MCU remains in a higher power state and drives each data conversion on the sensor side.

This mechanism allows the ADuCM3027/ADuCM3029 MCUs to be in a lower power state for a long duration and avoids unnecessary data processing which extends the battery life of the end product.

The key differences between RTC0 and RTC1 (FLEX_RTC) are shown in Table 3.

Table 3. RTC Features

Features	RTC0	RTC1 (FLEX_RTC)
Resolution of Time Base (Prescaling)	Counts time at 1 Hz in units of seconds. Operationally, always prescales to 1 Hz (for example, divide by 32,768) and always counts real time in units of seconds.	Can prescale the clock by any power of two from 0 to 15. It can count time in units of any of these 16 possible prescale settings. For example, the clock can be prescaled by 1, 2, 4, 8, …, 16384, or 32768.
Source Clock	LFXTAL.	Depending on the low frequency multiplexer (LFMUX) configuration, the RTC is clocked by the LFXTAL or the LFOSC.
Wake-Up Timer	Wake-up time is specified in units of seconds.	Supports alarm times down to a resolution of 30.7 µs, that is, where the time is specified down to a specific 32 kHz clock cycle.
Number of Alarms	One alarm only. Uses an absolute, nonrepeating alarm time, specified in units of 1 sec.	Two alarms. One absolute alarm time and one periodic alarm, repeating every 60 prescaled time units.
SensorStrobe Mechanism	Not available.	SensorStrobe is an alarm mechanism in the RTC that causes an output pulse to be sent via GPIOs to an external device to instruct the device to take a measurement or perform some action at a specific time. SensorStrobe events are scheduled at a specific target time relative to the real-time count of the RTC. SensorStrobe can be enabled in active, Flexi, and hibernate modes.
Input Capture	Not available.	Input capture takes a snapshot of the RTC when an external device signals an event via a transition on one of the GPIO inputs to the ADuCM3027/ ADuCM3029. Typically, an input-capture event is triggered by an autonomous measurement or action on such a device, which then signals to the ADuCM3027/ ADuCM3029 that the RTC must take a snapshot of time corresponding to the event. Taking the snapshot can wake up the ADuCM3027/ ADuCM3029 and cause an interrupt to the CPU. The CPU can subsequently obtain information from the RTC on the exact 32 kHz cycle on which the input capture event occurred.

Beeper Driver

The ADuCM3027/ADuCM3029 MCUs have an integrated audio driver for a beeper.

The beeper driver module in the ADuCM3027/ADuCM3029 MCUs generate a differential square wave of programmable frequency. It drives an external piezoelectric sound component with two terminals that connect to the differential square wave output.

The beeper driver consists of a module that can deliver frequencies ranging from 8 kHz to ~0.25 kHz. It operates on a fixed independent 32 kHz clock source that is unaffected by changes in system clocks.

It allows programmable tone durations from 4 ms to 1.02 sec in 4 ms increments. Pulse (single-tone) and sequence (multitone) modes provide versatile playback options.

In sequence mode, the beeper can be programmed to play any number of tone pairs from 1 to 254 (2 to 508 tones) or be programmed to play forever (until stopped by the user). Interrupts are available to indicate the start or end of any beep, the end of a sequence, or when the sequence is nearing completion.

Debug Capability

The ADuCM3027/ADuCM3029 MCUs support SWD.

ON-CHIP PERIPHERAL FEATURES

The ADuCM3027/ADuCM3029 MCUs have a rich set of peripherals connected to the core via several concurrent high bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see Figure 1).

The ADuCM3027/ADuCM3029 MCUs contain high speed serial ports, an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources, and power management control functions to tailor the performance and power characteristics of the MCU and system to many application scenarios.

Serial Ports (SPORT)

The ADuCM3027/ADuCM3029 MCUs provide two single direction half SPORTs or one bidirectional full SPORT. The synchronous serial ports provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as Analog Devices audio codecs, ADCs, and DACs. The serial ports contain two data lines, a clock, and a frame sync. The data lines can be programmed to either transmit or receive, and each data line has a dedicated DMA channel.

Serial port data can be automatically transferred to and from on-chip memory or external memory via dedicated DMA channels. The frame sync and clock can be shared. Some of the ADCs and DACs require two control signals for their conversion process. To interface with such devices, the SPT0_ACNV and SPT0_BCNV signals are provided. To use these signals, enable the timer enable mode. In this mode, a PWM timer inside the module generates the programmable SPT0_ACNV and SPT0_BCNV signals.

Serial ports operate in two modes:

- Standard digital signal processor (DSP) serial mode
- Timer enable mode

Serial Peripheral Interface (SPI) Ports

The ADuCM3027/ADuCM3029 MCUs provide three SPIs. SPI is an industry standard, full-duplex, synchronous serial interface that allows eight bits of data to be synchronously transmitted and simultaneously received. Each SPI incorporates two DMA channels that interface with the DMA controller. One DMA channel transmits and the other receives. The SPI on the MCU eases interfacing to external serial flash devices.

The SPI features include the following:

- Serial clock phase mode and serial clock polarity mode
- Loopback mode
- Continuous and repeated transfer mode
- Wired OR output mode
- Read command mode for half-duplex operation (transmit followed by receive)
- Flow control support in read command mode
- Support for 3-pin SPI in read command mode
- Multiple $\overline{CS}$ line support
- $\overline{CS}$ software override support

UART Port

The ADuCM3027/ADuCM3029 MCUs provide a full-duplex UART port, which is fully compatible with PC standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA, and asynchronous transfers of serial data. The UART port includes support for five to eight data bits, and none, even, or odd parity. A frame is terminated by one, one and a half, or two stop bits.

I^2C

The ADuCM3027/ADuCM3029 MCUs provide an I^2C bus peripheral that has two pins for data transfer. SCL is a serial clock pin and SDA is a serial data pin. The pins are configured in a wired AND format that allows arbitration in a multimaster system. A master device can be configured to generate the serial clock. The frequency is programmed by the user in the serial clock divisor register. The master channel can operate in fast mode (400 kHz) or standard mode (100 kHz).

DEVELOPMENT SUPPORT

Development support for the ADuCM3027/ADuCM3029 MCUs includes documentation, evaluation hardware, and development software tools.

Documentation

The ADuCM302x Ultra Low Power ARM Cortex-M3 MCU with Integrated Power Management Hardware Reference details the functionality of each block on the ADuCM3027/ADuCM3029 MCUs. It includes power management, clocking, memories, and peripherals.

ADC SPECIFICATIONS

Table 9. ADC Specifications

Parameter[1, 2]	VBAT/VREF (V)	Package	Typ	Unit	Conditions
NO MISSING CODE	1.8/1.25 (internal/external)	64-lead LFCSP	12	Bits	F_{in} = 1068 Hz, F_s = 100 KSPS, internal reference in low power mode, 400,000 samples end point method used
	1.8/1.25 (internal/external)	54-ball WLCSP	12	Bits	
	3.0/2.5 (internal/external)	64-lead LFCSP	12	Bits	
INTEGRAL NONLINEARITY ERROR	1.8/1.25 (internal/external)	64-lead LFCSP	±1.6	LSB	
	1.8/1.25 (internal/external)	54-ball WLCSP	±1.8	LSB	
	3.0/2.5 (internal/external)	64-lead LFCSP	±1.4	LSB	
DIFFERENTIAL NONLINEARITY ERROR	1.8/1.25 (internal/external)	64-lead LFCSP	−0.7, +1.15	LSB	
	1.8/1.25 (internal/external)	54-ball WLCSP	−0.75, +1.2	LSB	
	3.0/2.5 (internal/external)	64-lead LFCSP	−0.7, +1.1	LSB	
OFFSET ERROR	1.8/1.25 (external)	64-lead LFCSP	±0.5	LSB	
	1.8/1.25 (external)	54-ball WLCSP	±0.5	LSB	
	3.0/2.5 (external)	64-lead LFCSP	±0.5	LSB	
GAIN ERROR	1.8/1.25 (external)	64-lead LFCSP	±2.5	LSB	
	1.8/1.25 (external)	54-ball WLCSP	±3.0	LSB	
	3.0/2.5 (external)	64-lead LFCSP	±0.5	LSB	
I_{VBAT_ADC}[3]	1.8/1.25 (internal)	64-lead LFCSP	104	µA	F_{in} = 1068 Hz, F_s = 100 KSPS, internal reference in low power mode
	1.8/1.25 (internal)	54-ball WLCSP	108	µA	
	3.0/2.5 (internal)	64-lead LFCSP	131	µA	

[1] The ADC is characterized in standalone mode without core activity and minimal or no switching on the adjacent ADC channels and digital inputs/outputs.
[2] The specifications are characterized after performing internal ADC offset calibration.
[3] Current consumption from VBAT_ADC supply when ADC is performing the conversion.

FLASH SPECIFICATIONS

Table 10. Flash Specifications

Parameter	Min	Typ	Max	Unit	Conditions
FLASH					
Endurance	10,000			Cycles	
Data Retention		10		Years	

Serial Ports

To determine whether communication is possible between two devices at a particular clock speed, confirm the following specifications:

- Frame sync delay and frame sync setup and hold
- Data delay and data setup and hold
- Serial clock (SPT_CLK) width

In Figure 6, use the rising edge or the falling edge of SPT_CLK (external or internal) as the active sampling edge.

When externally generated, the SPORT clock is called $f_{SPTCLKEXT}$.

$$t_{SPTCLKEXT} = \frac{1}{f_{SPTCLKEXT}}$$

When internally generated, the programmed SPORT clock ($f_{SPTCLKPROG}$) frequency is set by the following equation:

$$f_{SPTCLKPROG} = \frac{f_{PCLK}}{2 \times (CLKDIV + 1)}$$

where CLKDIV is a field in the SPORT_DIV register that can be set from 0 to 65535.

Table 15. Serial Ports—External Clock

Parameter		Min	Max	Unit
TIMING REQUIREMENTS				
t_{SFSE}	Frame Sync Setup Before SPT_CLK (Externally Generated Frame Sync in Transmit or Receive Mode)[1]	5		ns
t_{HFSE}	Frame Sync Hold After SPT_CLK (Externally Generated Frame Sync in Transmit or Receive Mode)[1]	5		ns
t_{SDRE}	Receive Data Setup Before Receive SPT_CLK[1]	5		ns
t_{HDRE}	Receive Data Hold After SPT_CLK[1]	8		ns
t_{SCLKW}	SPT_CLK Width[2]	38.5		ns
t_{SPTCLK}	SPT_CLK Period[2]	77		ns
SWITCHING CHARACTERISTICS				
t_{DFSE}	Frame Sync Delay After SPT_CLK (Internally Generated Frame Sync in Transmit or Receive Mode)[3]		20	ns
t_{HOFSE}	Frame Sync Hold After SPT_CLK (Internally Generated Frame Sync in Transmit or Receive Mode)[3]	2		ns
t_{DDTE}	Transmit Data Delay After Transmit SPT_CLK[3]		20	ns
t_{HDTE}	Transmit Data Hold After Transmit SPT_CLK[3]	1		ns

[1] This specification is referenced to the sample edge.
[2] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external SPT_CLK.
[3] This specification is referenced to the drive edge.

Table 16. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
TIMING REQUIREMENTS				
t_{SDRI}	Receive Data Setup Before SPT_CLK[1]	25		ns
t_{HDRI}	Receive Data Hold After SPT_CLK[1]	0		ns
SWITCHING CHARACTERISTICS				
t_{DFSI}	Frame Sync Delay After SPT_CLK (Internally Generated Frame Sync in Transmit or Receive Mode)[2]		20	ns
t_{HOFSI}	Frame Sync Hold After SPT_CLK (Internally Generated Frame Sync in Transmit or Receive Mode)[2]	–8		ns
t_{DDTI}	Transmit Data Delay After SPT_CLK[2]		20	ns
t_{HDTI}	Transmit Data Hold After SPT_CLK[2]	–7		ns
t_{SCLKIW}	SPT_CLK Width	t_{PCLK} – 1.5		ns
t_{SPTCLK}	SPT_CLK Period	2 × t_{PCLK} – 1		ns

[1] This specification is referenced to the sample edge.
[2] This specification is referenced to the drive edge.

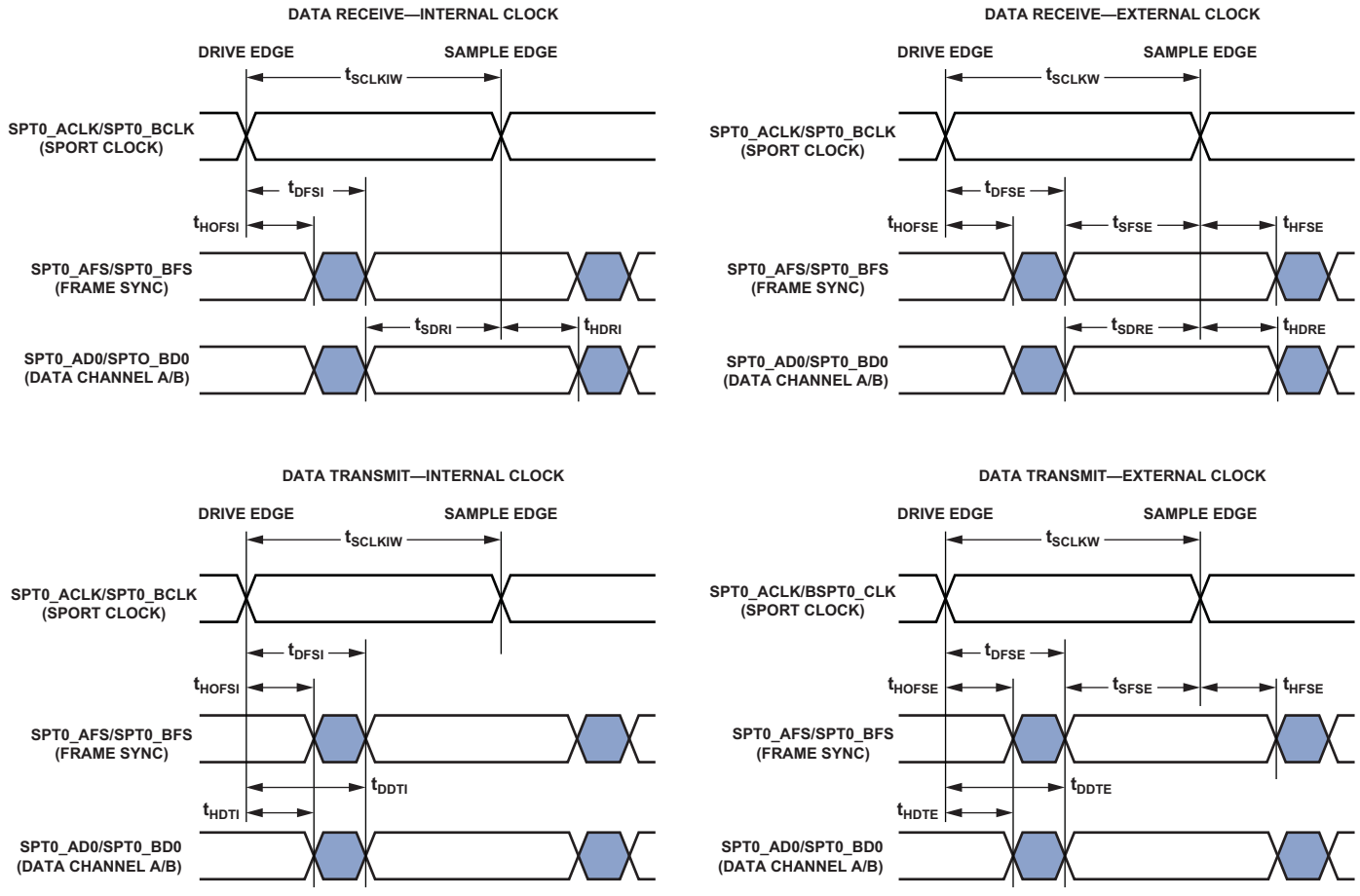

Figure 6. Serial Ports

Table 17. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
SWITCHING CHARACTERISTICS				
t_{DDTIN}	Data Enable From Internal Transmit SPT_CLK[1]	5		ns
t_{DDTTI}	Data Disable From Internal Transmit SPT_CLK[1]		160	ns

[1] This specification is referenced to the drive edge.

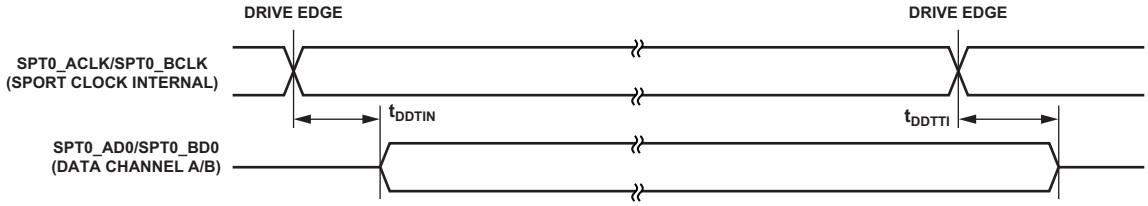

Figure 7. Serial Ports—Enable and Three-State

SPI Timing

Table 18, Figure 8, and Figure 9 (for master mode) and Table 19, Figure 10, and Figure 11 (for slave mode) describe SPI timing specifications. High speed SPI (SPIH) can be used for high data rate peripherals.

Table 18. SPI Master Mode Timing[1]

Parameter		Min	Max	Unit
TIMING REQUIREMENTS				
t_{CS}	$\overline{CS}$ to SCLK Edge	$0.5 \times t_{PCLK} - 3$		ns
t_{SL}	SCLK Low Pulse Width	$t_{PCLK} - 3.5$		ns
t_{SH}	SCLK High Pulse Width	$t_{PCLK} - 3.5$		ns
t_{DSU}	Data Input Setup Time Before SCLK Edge	5		ns
t_{DHD}	Data Input Hold Time After SCLK Edge	20		ns
SWITCHING CHARACTERISTICS				
t_{DAV}	Data Output Valid After SCLK Edge		25	ns
t_{DOSU}	Data Output Setup Before SCLK Edge	$t_{PCLK} - 2.2$		ns
t_{SFS}	$\overline{CS}$ High After SCLK Edge	$0.5 \times t_{PCLK} - 3$		ns

[1] This specification is characterized with respect to double drive strength.

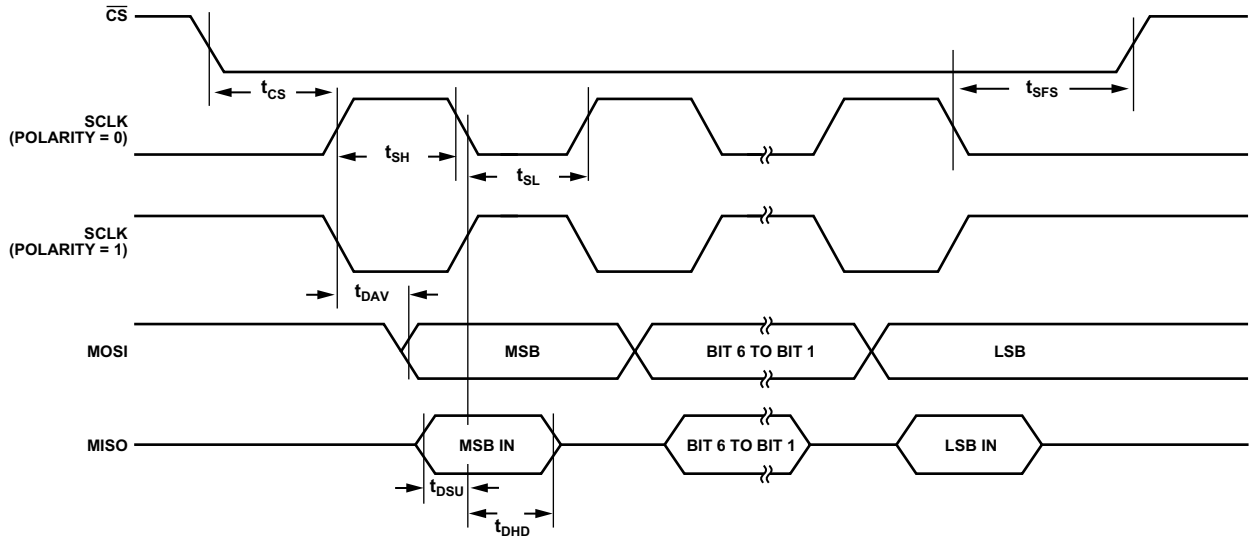

Figure 8. SPI Master Mode Timing (Phase Mode = 1)

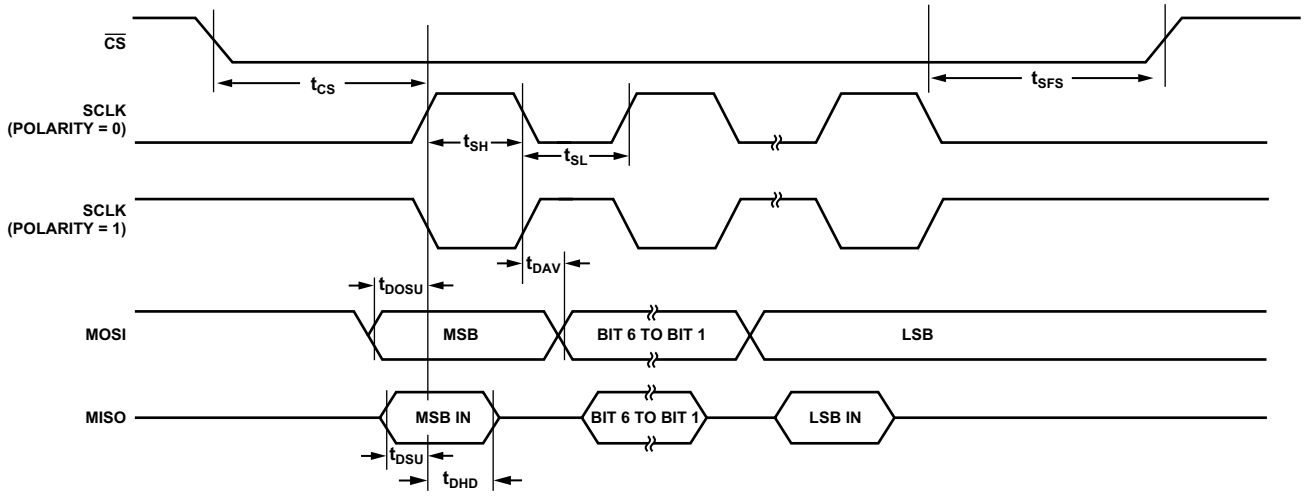

Figure 9. SPI Master Mode Timing (Phase Mode = 0)

Table 19. SPI Slave Mode Timing

Parameter		Min	Max	Unit
TIMING REQUIREMENTS				
t_{CS}	$\overline{CS}$ to SCLK Edge	38.5		ns
t_{SL}	SCLK Low Pulse Width	38.5		ns
t_{SH}	SCLK High Pulse Width	38.5		ns
t_{DSU}	Data Input Setup Time Before SCLK Edge	6		ns
t_{DHD}	Data Input Hold Time After SCLK Edge	8		ns
SWITCHING CHARACTERISTICS				
t_{DAV}	Data Output Valid After SCLK Edge	25		ns
t_{DOCS}	Data Output Valid After $\overline{CS}$ Edge		20	ns
t_{SFS}	$\overline{CS}$ High After SCLK Edge	38.5		ns

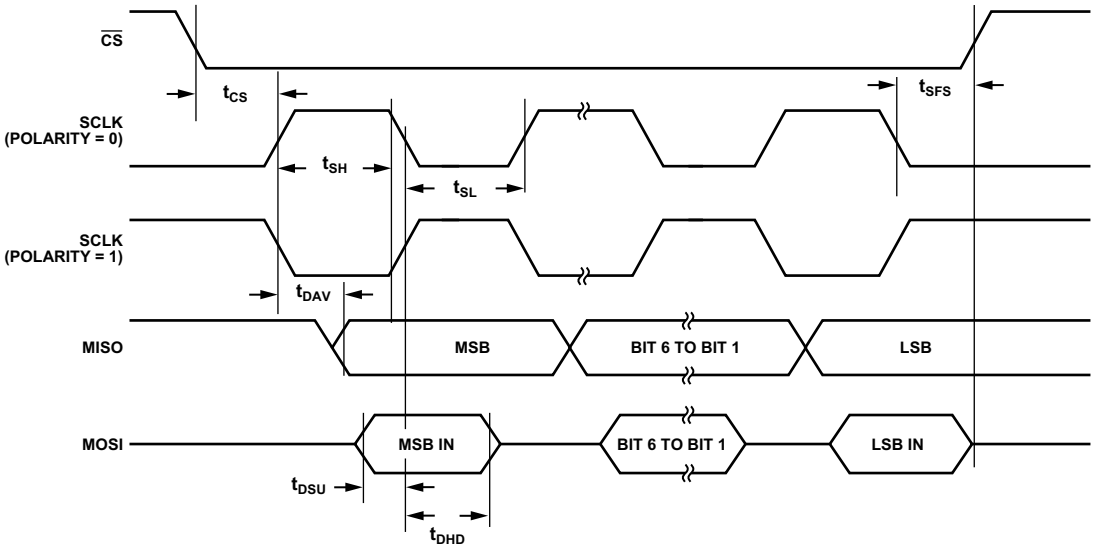

Figure 10. SPI Slave Mode Timing (Phase Mode = 1)

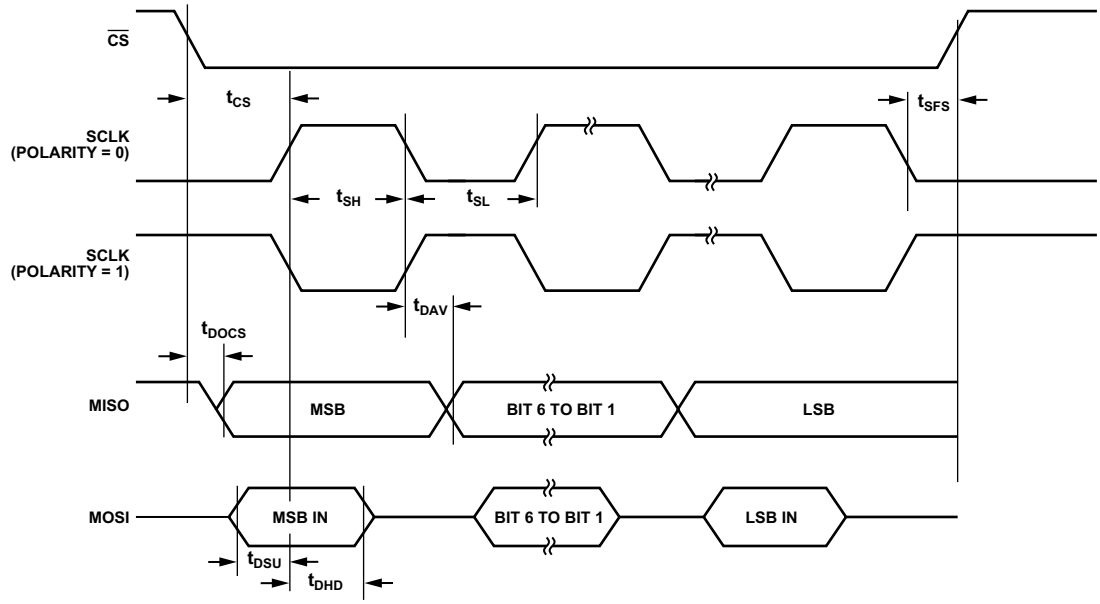

Figure 11. SPI Slave Mode Timing (Phase Mode = 0)

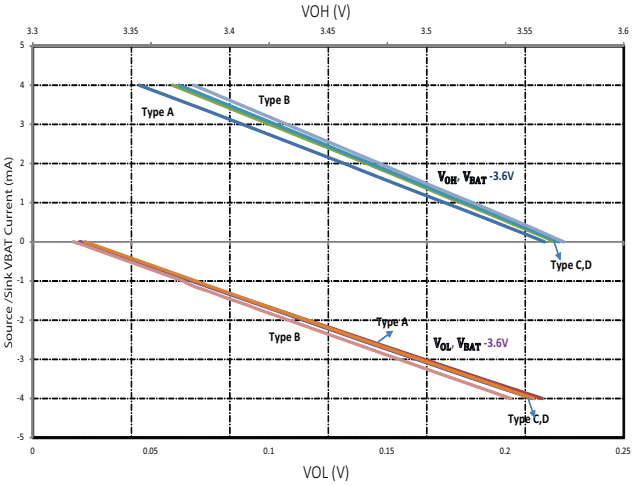

Figure 20. Output Double Drive Strength Characteristics (VBAT = 3.6 V)

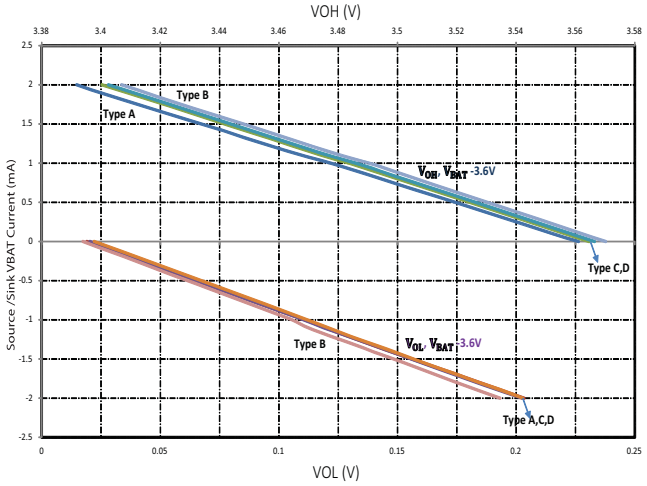

Figure 21. Output Single Drive Strength Characteristics (VBAT = 3.6 V)

ENVIRONMENTAL CONDITIONS

Table 23. Thermal Characteristics (64-Lead LFCSP)

Parameter	Typ	Unit
θ_{JA}	28.2	°C/W
θ_{JC}	5.4	°C/W

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first-order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:
T_A is ambient temperature (°C).
T_J is junction temperature (°C).
P_D is power dissipation (To calculate P_D, see the Power Supply Current section).

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heat sink is required.

Figure 23 shows an overview of signal placement on the 54-Ball WLCSP.

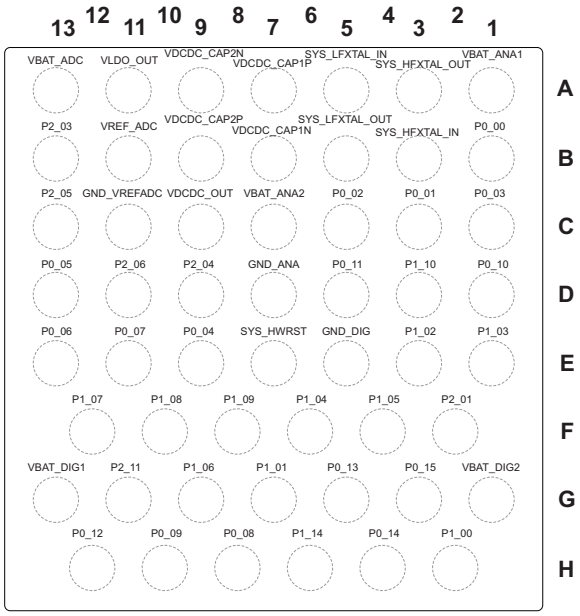

Figure 23. 54-Ball WLCSP Configuration

Table 24 lists the signal descriptions of the ADuCM3027/ADuCM3029 MCUs.

Table 24. Signal Functional Descriptions

GPIO Signal Name	Description
SPIn_CLK	SPI Clock. n = 0, 1, 2.
SPIn_MOSI	SPI Master Out Slave In. n = 0, 1, 2.
SPIn_MISO	SPI Master In Slave Out. n = 0, 1, 2.
SPIn_RDY	SPI Ready Signal. n = 0, 1, 2.
SPIn_CSm	SPI Chip Select Signal. n = 0, 1, 2 and m = 0, 1, 2, 3.
SPT0_ACLK	SPORT A Clock Signal.
SPT0_AFS	SPORT A Frame Sync.
SPT0_AD0	SPORT A Data Pin 0.
SPT0_ACNV	SPORT A Converter Signal for Interface with ADC.
SPT0_BCLK	SPORT B Clock Signal.
SPT0_BFS	SPORT B Frame Sync.
SPT0_BD0	SPORT B Data Pin 0.
SPT0_BCNV	SPORT B Converter Signal for Interface with ADC.
I2C0_SCL	I^2C Clock.
I2C0_SDA	I^2C Data.
SWD0_CLK	Serial Wire Debug Clock.
SWD0_DATA	Serial Wire Debug Data.
BPR0_TONE_N	Beeper Tone Negative Pin.
BPR0_TONE_P	Beeper Tone Positive Pin.
UART0_TX	UART Transmit Pin.
UART0_RX	UART Receive Pin.
UART0_SOUT_EN	UART Serial Data Out Pin.
XINT0_WAKEn	System Wake-Up Pin. Wake Up from Flexi/Hibernate/Shutdown Modes[1]. n = 0, 1, 2, 3.
TMRn_OUT	Timer Output Pin. n = 0, 1, 2.
SYS_BMODE0	Boot Mode Pin.
SYS_CLKIN	External Clock In Pin.
SYS_CLKOUT	External Clock Out Pin.
RTC1_SS1	RTC1 SensorStrobe Pin.
ADC0_VINn	ADC Voltage Input Pin. n = 0, 1, 2, 3, 4, 5, 6, 7.

[1] For shutdown, XINT0_WAKE3 is not capable of waking the device from shutdown mode.

Table 25 lists the 64-Lead LFCSP_WQ package by pin number for the ADuCM3027/ADuCM3029 MCUs.

Table 25. Pin Function Descriptions, 64-Lead LFCSP_WQ

Pin No.	GPIO	Signal Name	Description	GPIO Pull
1		VBAT_ANA1	Analog 3 V Supply.	
2		SYS_HFXTAL_IN	26 MHz High Frequency Crystal.	
3		SYS_HFXTAL_OUT	26 MHz High Frequency Crystal.	
4		SYS_LFXTAL_IN	32 kHz Low Frequency Crystal.	
5		SYS_LFXTAL_OUT	32 kHz Low Frequency Crystal.	
6		VDCDC_CAP1N	Buck Fly Capacitor.	
7		VDCDC_CAP1P	Buck Fly Capacitor.	
8		VBAT_ANA2	Analog 3 V Supply.	
9		VDCDC_OUT	Buck Output Capacitor.	
10		VDCDC_CAP2N	Buck Fly Capacitor.	
11		VDCDC_CAP2P	Buck Fly Capacitor.	
12		VLDO_OUT	LDO Output Capacitor.	
13		VREF_ADC	Analog Reference Voltage for ADC.	
14		VBAT_ADC	Analog 3 V Supply for ADC.	
15		GND_VREFADC	Reference Ground for ADC.	
16	P2_03	ADC0_VIN0/GPIO35		PU
17	P2_04	ADC0_VIN1/GPIO36		PU
18	P2_05	ADC0_VIN2/GPIO37		PU
19	P2_06	ADC0_VIN3/GPIO38		PU
20	P2_07	ADC0_VIN4/SPI2_CS3/GPIO39		PU
21	P2_08	ADC0_VIN5/SPI0_CS2/GPIO40		PU
22	P2_09	ADC0_VIN6/SPI0_CS3/GPIO41		PU
23	P2_10	ADC0_VIN7/SPI2_CS2/GPIO42		PU
24	P0_05	I2C0_SDA/GPIO05		PU
25		$\overline{\text{SYS\_HWRST}}$	System Hardware Reset.	
26	P0_04	I2C0_SCL/GPIO04		PU
27	P0_07	GPIO07/SWD0_DATA		PU
28	P0_06	GPIO06/SWD0_CLK		PD
29	P1_09	SPI1_CS0/GPIO25		PU
30	P1_08	SPI1_MISO/GPIO24		PU
31	P1_07	SPI1_MOSI/GPIO23		PU
32	P1_06	SPI1_CLK/GPIO22		PU
33	P2_11	SPI1_CS1/SYS_CLKOUT/GPIO43/RTC1_SS1		PU
34		VBAT_DIG1	Digital 3 V Supply.	
35	P0_12	SPT0_AD0/GPIO12		PU
36	P2_00	SPT0_AFS/GPIO32		PU
37	P1_15	SPT0_ACLK/GPIO31		PU
38	P1_01	GPIO17/SYS_BMODE0		PU
39	P0_09	BPR0_TONE_P/SPI2_CS1/GPIO09		PU
40	P0_08	BPR0_TONE_N/GPIO08		PU
41	P1_11	TMR1_OUT/GPIO27		PU
42	P1_12	GPIO28		PU
43	P1_13	GPIO29		PU
44	P1_14	SPI0_RDY/GPIO30		PU
45	P2_02	SPT0_ACNV/SPI1_CS2/GPIO34		PU

Table 26 lists the 54-Ball WLCSP package by ball number for the ADuCM3027/ADuCM3029 MCUs.

Table 26. Pin Function Descriptions, 54-Ball WLCSP

Ball No.	GPIO	Pin Label	Description	GPIO Pull
A01		VBAT_ANA1	Analog 3 V Supply.	
A03		SYS_HFXTAL_OUT	26 MHz High Frequency Crystal.	
A05		SYS_LFXTAL_IN	32 kHz Low Frequency Crystal.	
A07		VDCDC_CAP1P	Buck Fly Capacitor.	
A09		VDCDC_CAP2N	Buck Fly Capacitor.	
A11		VLDO_OUT	LDO Output Capacitor	
A13		VBAT_ADC	Analog 3 V Supply for ADC.	
B01	P0_00	SPI0_CLK/SPT0_BCLK/GPIO00		PU
B03		SYS_HFXTAL_IN	26 MHz High Frequency Crystal.	
B05		SYS_LFXTAL_OUT	32 kHz Low Frequency Crystal.	
B07		VDCDC_CAP1N	Buck Fly Capacitor.	
B09		VDCDC_CAP2P	Buck Fly Capacitor.	
B11		VREF_ADC	Analog Reference Voltage for ADC.	
B13	P2_03	ADC0_VIN0/GPIO35		PU
C01	P0_03	SPI0_CS0/SPT0_BCNV/SPI2_RDY/GPIO03		PU
C03	P0_01	SPI0_MOSI/SPT0_BFS/GPIO01		PU
C05	P0_02	SPI0_MISO/SPT0_BD0/GPIO02		PU
C07		VBAT_ANA2	Analog 3 V Supply.	
C09		VDCDC_OUT	Buck Output Capacitor.	
C11		GND_VREFADC	Reference Ground for ADC.	
C13	P2_05	ADC0_VIN2/GPIO37		PU
D01	P0_10	UART0_TX/GPIO10		PU
D03	P1_10	SPI0_CS1/SYS_CLKIN/SPI1_CS3/GPIO26		PU
D05	P0_11	UART0_RX/GPIO11		PU
D07		GND_ANA	Analog Ground.	
D09	P2_04	ADC0_VIN1/GPIO36		PU
D11	P2_06	ADC0_VIN3/GPIO38		PU
D13	P0_05	I2C0_SDA/GPIO05		PU
E01	P1_03	SPI2_MOSI/GPIO19		PU
E03	P1_02	SPI2_CLK/GPIO18		PU
E05		GND_DIG	Digital Ground.	
E07		$\overline{\text{SYS\_HWRST}}$	System Hardware Reset.	
E09	P0_04	I2C0_SCL/GPIO04		PU
E11	P0_07	GPIO07/SWD0_DATA		PU
E13	P0_06	GPIO06/SWD0_CLK		PD
F02	P2_01	XINT0_WAKE3/TMR2_OUT/GPIO33		PU
F04	P1_05	SPI2_CS0/GPIO21		PU
F06	P1_04	SPI2_MISO/GPIO20		PU
F08	P1_09	SPI1_CS0/GPIO25		PU
F10	P1_08	SPI1_MISO/GPIO24		PU
F12	P1_07	SPI1_MOSI/GPIO23		PU
G01		VBAT_DIG2	Digital 3 V Supply.	
G03	P0_15	XINT0_WAKE0/GPIO15		PU

Table 26. Pin Function Descriptions, 54-Ball WLCSP (Continued)

Ball No.	GPIO	Pin Label	Description	GPIO Pull
G05	P0_13	XINT0_WAKE2/GPIO13		PU
G07	P1_01	GPIO17/SYS_BMODE0		PU
G09	P1_06	SPI1_CLK/GPIO22		PU
G11	P2_11	SPI1_CS1/SYS_CLKOUT/GPIO43/RTC1_SS1		PU
G13		VBAT_DIG1	Digital 3 V Supply.	
H02	P1_00	XINT0_WAKE1/GPIO16		PU
H04	P0_14	TMR0_OUT/SPI1_RDY/GPIO14		PU
H06	P1_14	SPI0_RDY/GPIO30		PU
H08	P0_08	BPR0_TONE_N/GPIO08		PU
H10	P0_09	BPR0_TONE_P/SPI2_CS1/GPIO09		PU
H12	P0_12	SPT0_AD0/GPIO12/UART0_SOUT_EN		PU