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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	26MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	36
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	1.74V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	54-UFBGA, WLCSP
Supplier Device Package	54-WLCSP (2.76x2.76)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aducm3029bcbz-rl

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REVISION HISTORY

3/2017—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADuCM3027/ADuCM3029 microcontroller units (MCUs) are ultra low power microcontroller systems with integrated power management for processing, control, and connectivity. The MCU system is based on the ARM Cortex-M3 processor, a collection of digital peripherals, embedded SRAM and flash memory, and an analog subsystem which provides clocking, reset, and power management capability in addition to an analog-to-digital converter (ADC) subsystem. For a feature comparison across the ADuCM3027/ADuCM3029 product offerings, see Table 1.

Table 1. Product Flash Memory Options

Device	Embedded Flash Memory Size
ADuCM3029	256 KB
ADuCM3027	128 KB

System features that are common across the ADuCM3027/ADuCM3029 MCUs include the following:

- Up to 26 MHz ARM Cortex-M3 processor
- Up to 256 KB of embedded flash memory with error correction code (ECC)
- Optional 4 KB cache for lower active power
- 64 KB system SRAM with parity
- Power management unit (PMU)
- Multilayer advanced microcontroller bus architecture (AMBA) bus matrix
- Central direct memory access (DMA) controller
- Beeper interface
- Serial port (SPORT), serial peripheral interface (SPI), inter-integrated circuit (I^2C), and universal asynchronous receiver/transmitter (UART) peripheral interfaces
- Cryptographic hardware support with advanced encryption standard (AES) and secure hash algorithm (SHA) -256
- Real-time clock (RTC)
- General-purpose and watchdog timers
- Programmable general-purpose input/output (GPIO) pins
- Hardware cyclic redundancy check (CRC) calculator with programmable generator polynomial
- Power-on reset (POR) and power supply monitor (PSM)
- 12-bit successive approximation register (SAR) ADC
- True random number generator (TRNG)

To support low dynamic and hibernate power management, the ADuCM3027/ADuCM3029 MCUs provide a collection of power modes and features, such as dynamic and software controlled clock gating and power gating.

For full details on the ADuCM3027/ADuCM3029 MCUs, refer to the ADuCM302x Ultra Low Power ARM Cortex-M3 MCU with Integrated Power Management Hardware Reference.

HIGHLIGHTS

The following are the key features of the ADuCM3027/ADuCM3029 MCUs**:**

- Industry leading ultralow power consumption.
- Robust operation.
  - Full voltage monitoring in deep sleep modes.
  - ECC support on flash.
  - Parity error detection on SRAM memory.
- Leading edge security.
  - Fast encryption provides read protection to customer algorithms.
  - Write protection prevents device reprogramming by unauthorized code.
- Failure detection of 32 kHz LFXTAL via interrupt.
- SensorStrobe for precise time synchronized sampling of external sensors.
  - Works in hibernate mode, resulting in drastic current reduction in system solutions. Current consumption reduces by 10 times when using, for example, the ADXL363 accelerometer.
  - Software intervention is not required after setup.
  - No pulse drift due to software execution.

ARM CORTEX-M3 PROCESSOR

The ARM Cortex-M3 core is a 32-bit reduced instruction set computer (RISC). The length of the data can be 8 bits, 16 bits, or 32 bits. The length of the instruction word is 16 bits or 32 bits.

The processor has the following features:

- Cortex-M3 architecture
  - Thumb-2 instruction set architecture (ISA) technology
  - Three-stage pipeline with branch speculation
  - Low latency interrupt processing with tail chaining
  - Single-cycle multiply
  - Hardware divide instructions
  - Nested vectored interrupt controller (NVIC) (64 interrupts and 8 priorities)
  - Two hardware breakpoints and one watchpoint (unlimited software breakpoints using Segger JLink)
- Memory protection unit (MPU)
  - Eight-region MPU with subregions and background region
  - Programmable clock generator unit

Additional power management features include the following:

- Customized clock gating for active and Flexi modes
- Power gating to reduce leakage in hibernate and shutdown modes
- Flexible sleep modes
- Shutdown mode with no retention
- Optional high efficiency buck converter to reduce power
- Integrated low power oscillators

Power Modes

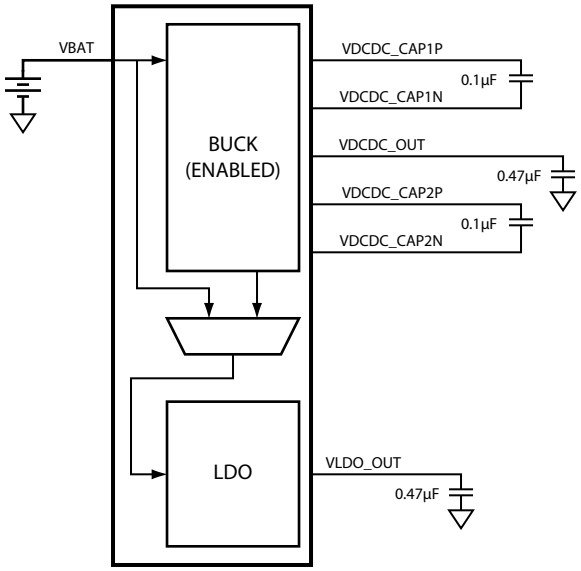
The PMU provides control of the ADuCM3027/ADuCM3029 power modes and allows the ARM Cortex-M3 to control the clocks and power gating to reduce the power consumption.

Several power modes are available. Each mode provides an additional low power benefit with a corresponding reduction in functionality.

- Active mode. All peripherals can be enabled. Active power is managed by optimized clock management. See Table 4 for details on active mode power.
- Flexi mode. The ARM Cortex-M3 core is clock gated, but the remainder of the system is active. No instructions can be executed in this mode, but DMA transfers can continue between peripherals and memory as well as memory to memory. See Table 5 for details on Flexi mode power.
- Hibernate mode. This mode provides state retention, configurable SRAM and port pin retention, a limited number of wake-up interrupts (XINT0_WAKEn and UART0_RX), and, optionally, two RTCs—RTC0 and RTC1 (FLEX_RTC).
- Shutdown mode. This mode is the deepest sleep mode, in which all the digital and analog circuits are powered down with an option to wake from four possible wake-up sources: three external interrupts and RTC0. The RTC0 can be optionally enabled in this mode and the device can be periodically woken up by the RTC0 interrupt. See Table 6 for deep sleep (hibernate and shutdown) mode specifications.

The following features are available for power management and control:

- A voltage range of 1.74 V to 3.6 V, using a single supply (such as the CR2032 coin cell battery).
- GPIOs are driven directly from the battery. The pin state is retained in hibernate and shutdown modes. The GPIO configuration is only retained in hibernate mode.
- Wake-up from external interrupt (via GPIOs), UART0_RX interrupt, and RTCs for hibernate mode.
- Wake-up from external interrupt (via GPIOs) and RTC0 for shutdown mode.
- Optional high power buck converter for 1.2 V full on support; for MCU usage only. See Figure 3 for the suggested external circuitry.



Note: For designs in which the optional buck is not used, the following pins must be left unconnected—VDCDC_CAP1P, VDCDC_CAP1N, VDCDC_OUT, VDCDC_CAP2P, and VDCDC_CAP2N.

Figure 3. Buck Enabled Design

Security Features

The ADuCM3027/ADuCM3029 MCUs provide a combination of hardware and software protection mechanisms that lock out access to the devices in secure mode, but grant access in open mode. These mechanisms include password protected slave boot mode (UART), as well as password protected serial wire debug (SWD) interfaces.

Mechanisms are provided to protect the device contents (flash, SRAM, CPU registers, and peripheral registers) from being read through an external interface by an unauthorized user. This is referred to as read protection.

It is possible to protect the device from being reprogrammed in circuit with unauthorized code. This is referred to as in circuit write protection.

CAUTION
This product includes security features that can be used to protect embedded nonvolatile memory contents and prevent execution of unauthorized code. When security is enabled on this device (either by the ordering party or the subsequent receiving parties), the ability of Analog Devices to conduct failure analysis on returned devices is limited. Contact Analog Devices for details on the failure analysis limitations for this device.

The devices can be configured with no protection, read protection, or read and in circuit write protection. It is not necessary to provide in circuit write protection without read protection.

The main features of the ADC subsystem include the following:

- 12-bit resolution.
- Programmable ADC update rate from 10 KSPS to 1.8 MSPS.
- Integrated input multiplexer that supports up to eight channels.
- Temperature sensing support.
- Battery monitoring support.
- Software selectable on-chip reference voltage generation—1.25 V and 2.5 V.
- Software selectable internal or external reference.
- Autocycle mode—ability to automatically select a sequence of input channels for conversion.
- Averaging function—converted data on single or multiple channels can be averaged up to 256 samples.
- Alert function—internal digital comparator for ADC0_VIN0, ADC0_VIN1, ADC0_VIN2, and ADC0_VIN3 channels. An interrupt is generated if the digital comparator detects an ADC result above or below a user defined threshold.
- Dedicated DMA channel support.
- Each channel, including temperature sensor and battery monitoring, has a data register for conversion result.

Clocking

The ADuCM3027/ADuCM3029 MCUs have the following clocking options:

- 26 MHz
  - Internal oscillator—HFOSC (26 MHz)
  - External crystal oscillator—HFXTAL (26 MHz or 16 MHz)
  - GPIO clock in—SYS_CLKIN
- 32 kHz
  - Internal oscillator—LFOSC
  - External crystal oscillator—LFXTAL

The clock options have software configurability with the following exceptions:

- HFOSC cannot be disabled when using an internal buck regulator.
- LFOSC cannot be disabled even if using LFXTAL.

Real-Time Clock (RTC)

The ADuCM3027/ADuCM3029 MCUs have two real-time clock blocks—RTC0 and RTC1 (FLEX_RTC). The clock blocks share a low power crystal oscillation circuit that operates in conjunction with a 32,768 Hz external crystal.

The RTC has an alarm that interrupts the core when the programmed alarm value matches the RTC count. The software enables and configures the RTC.

The RTC also has a digital trim capability to allow a positive or negative adjustment to the RTC count at fixed intervals.

The FLEX_RTC supports SensorStrobe mechanism. Using this mechanism, the ADuCM3027/ADuCM3029 MCUs can be used as a programmable clock generator in some power modes, including hibernate mode. In this way, the external sensors can have their timing domains mastered by the ADuCM3027/ADuCM3029 MCUs, as SensorStrobe can output a programmable divider from the FLEX_RTC, which can operate up to a resolution of 30.7 µs. The sensors and MCU are in sync, which removes the need for additional resampling of data to time align it.

In the absence of this mechanism,

- The external sensor uses an RC oscillator (~±30% typical variation). The MCU must sample the data and resample it on the time domain of the MCU before using it.

Or

- The MCU remains in a higher power state and drives each data conversion on the sensor side.

This mechanism allows the ADuCM3027/ADuCM3029 MCUs to be in a lower power state for a long duration and avoids unnecessary data processing which extends the battery life of the end product.

The key differences between RTC0 and RTC1 (FLEX_RTC) are shown in Table 3.

Table 3. RTC Features

Features	RTC0	RTC1 (FLEX_RTC)
Resolution of Time Base (Prescaling)	Counts time at 1 Hz in units of seconds. Operationally, always prescales to 1 Hz (for example, divide by 32,768) and always counts real time in units of seconds.	Can prescale the clock by any power of two from 0 to 15. It can count time in units of any of these 16 possible prescale settings. For example, the clock can be prescaled by 1, 2, 4, 8, …, 16384, or 32768.
Source Clock	LFXTAL.	Depending on the low frequency multiplexer (LFMUX) configuration, the RTC is clocked by the LFXTAL or the LFOSC.
Wake-Up Timer	Wake-up time is specified in units of seconds.	Supports alarm times down to a resolution of 30.7 µs, that is, where the time is specified down to a specific 32 kHz clock cycle.
Number of Alarms	One alarm only. Uses an absolute, nonrepeating alarm time, specified in units of 1 sec.	Two alarms. One absolute alarm time and one periodic alarm, repeating every 60 prescaled time units.
SensorStrobe Mechanism	Not available.	SensorStrobe is an alarm mechanism in the RTC that causes an output pulse to be sent via GPIOs to an external device to instruct the device to take a measurement or perform some action at a specific time. SensorStrobe events are scheduled at a specific target time relative to the real-time count of the RTC. SensorStrobe can be enabled in active, Flexi, and hibernate modes.
Input Capture	Not available.	Input capture takes a snapshot of the RTC when an external device signals an event via a transition on one of the GPIO inputs to the ADuCM3027/ ADuCM3029. Typically, an input-capture event is triggered by an autonomous measurement or action on such a device, which then signals to the ADuCM3027/ ADuCM3029 that the RTC must take a snapshot of time corresponding to the event. Taking the snapshot can wake up the ADuCM3027/ ADuCM3029 and cause an interrupt to the CPU. The CPU can subsequently obtain information from the RTC on the exact 32 kHz cycle on which the input capture event occurred.

Hardware

The ADuCM3029 EZ-KIT® is available to prototype sensor configurations with the ADuCM3027/ADuCM3029 MCUs.

Software

The ADuCM3029 EZ-KIT includes a complete development and debug environment for the ADuCM3027/ADuCM3029 MCUs. The board support package (BSP) for the ADuCM3027/ADuCM3029 is provided for the IAR Embedded Workbench for ARM, Keil™, and CrossCore® embedded studio (CCES) environments.

The BSP also includes operating system (OS) aware drivers and example code for all the peripherals on the devices.

ADDITIONAL INFORMATION

The following publications that describe the ADuCM3027/ADuCM3029 MCUs can be ordered from any Analog Devices sales office or accessed electronically on the Analog Devices website:

- ADuCM302x Ultra Low Power ARM Cortex-M3 MCU with Integrated Power Management Hardware Reference.
- ADuCM3027/ADuCM3029 Anomaly List

This data sheet describes the ARM Cortex-M3 core and memory architecture used on the ADuCM3027/ADuCM3029 MCUs, but does not provide detailed programming information for the ARM processor. For more information about programming the ARM processor, visit the ARM Infocenter web page.

The applicable documentation for programming the ARM Cortex-M3 processor include the following:

- *ARM Cortex-M3 Devices Generic User Guide*
- *ARM Cortex-M3 Technical Reference Manual*

REFERENCE DESIGNS

The Circuits from the Lab® page provides the following:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

SECURITY FEATURES DISCLAIMER

To our knowledge, the Security Features, when used in accordance with the data sheet and hardware reference manual specifications, provide a secure method of implementing code and data safeguards. However, Analog Devices does not guarantee that this technology provides absolute security. ACCORDINGLY, ANALOG DEVICES HEREBY DISCLAIMS ANY AND ALL EXPRESS AND IMPLIED WARRANTIES THAT THE SECURITY FEATURES CANNOT BE BREACHED, COMPROMISED, OR OTHERWISE CIRCUMVENTED AND IN NO EVENT SHALL ANALOG DEVICES BE LIABLE FOR ANY LOSS, DAMAGE, DESTRUCTION, OR RELEASE OF DATA, INFORMATION, PHYSICAL PROPERTY, OR INTELLECTUAL PROPERTY.

SYSTEM CLOCKS/TIMERS

Table 7 and Table 8 show the system clock specifications for the ADuCM3027/ADuCM3029 MCUs.

Platform External Crystal Oscillator

Table 7. Platform External Crystal Oscillator Specifications

Parameter	Min	Typ	Max	Unit	Conditions
LOW FREQUENCY EXTERNAL CRYSTAL OSCILLATOR (LFXTAL)					
$C_{EXT1} = C_{EXT2}$	6		10	pF	External capacitor, $C_{EXT1} = C_{EXT2}$ (symmetrical load), for $C_L \leq 5$ pF (maximum) and ESR = 30 kΩ (maximum). C_{EXT1}, C_{EXT2} must be selected considering the printed circuit board (PCB) trace capacitance due to routing.
Frequency		32,768		Hz	
HIGH FREQUENCY EXTERNAL CRYSTAL OSCILLATOR (HFXTAL)					
$C_{EXT1} = C_{EXT2}$			20	pF	External capacitor, $C_{EXT1} = C_{EXT2}$ (symmetrical load), for C_L = 10 pF (maximum) and ESR = 50 Ω (maximum). C_{EXT1}, C_{EXT2} must be selected considering the PCB trace capacitance due to routing.
Frequency		26		MHz	

On-Chip RC Oscillator

Table 8. On-Chip RC Oscillator Specifications

Parameter	Min	Typ	Max	Unit	Conditions
HIGH FREQUENCY RC OSCILLATOR (HFOSC)					
Frequency	25.09	26	26.728	MHz	
LOW FREQUENCY RC OSCILLATOR (LFOSC)					
Frequency	30,800	32,768	34,407	Hz	

ABSOLUTE MAXIMUM RATINGS

Stresses at or above those listed in Table 11 may cause permanent damage to the product. This is a stress rating only. The functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 11. Absolute Maximum Ratings

Parameter	Rating	Unit
SUPPLY		
VBAT_ANA1	−0.3 to +3.6	V
VBAT_ANA2		
VBAT_ADC		
VBAT_DIG1		
VBAT_DIG2		
VREF_ADC		
ANALOG		
VDCDC_CAP1N	−0.3 to +3.6	V
VDCDC_AP1P		
VDCDC_OUT		
VDCDC_CAP2N		
VDCDC_CAP2P		
VLDO_OUT	−0.3 to +1.32	V
SYS_HFXTAL_IN		
SYS_HFXTAL_OUT		
SYS_LFXTAL_IN		
SYS_LFXTAL_OUT		
DIGITAL INPUT/OUTPUT		
P0.X	−0.3 to +3.6	V
P1.X		
P2.X		
$\overline{\text{SYS\_HWRST}}$		

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE INFORMATION

Figure 4 and Table 12 provide details about package branding. For a complete listing of product availability, see the Ordering Guide section.

Figure 4. Product Information on Package[1]

[1] Exact brand may differ, depending on package type.

Table 12. Package Brand Information

Brand Key	Field Description
ADuCM3027/ADuCM3029	Product model
t	Temperature range
pp	Package type
Z	RoHS compliant designation
ccc	See the Ordering Guide section
vvvvvv.x	Assembly lot code
n.n	Silicon revision
yyww	Date code

Serial Ports

To determine whether communication is possible between two devices at a particular clock speed, confirm the following specifications:

- Frame sync delay and frame sync setup and hold
- Data delay and data setup and hold
- Serial clock (SPT_CLK) width

In Figure 6, use the rising edge or the falling edge of SPT_CLK (external or internal) as the active sampling edge.

When externally generated, the SPORT clock is called $f_{SPTCLKEXT}$.

$$t_{SPTCLKEXT} = \frac{1}{f_{SPTCLKEXT}}$$

When internally generated, the programmed SPORT clock ($f_{SPTCLKPROG}$) frequency is set by the following equation:

$$f_{SPTCLKPROG} = \frac{f_{PCLK}}{2 \times (CLKDIV + 1)}$$

where CLKDIV is a field in the SPORT_DIV register that can be set from 0 to 65535.

Table 15. Serial Ports—External Clock

Parameter		Min	Max	Unit
TIMING REQUIREMENTS				
t_{SFSE}	Frame Sync Setup Before SPT_CLK (Externally Generated Frame Sync in Transmit or Receive Mode)[1]	5		ns
t_{HFSE}	Frame Sync Hold After SPT_CLK (Externally Generated Frame Sync in Transmit or Receive Mode)[1]	5		ns
t_{SDRE}	Receive Data Setup Before Receive SPT_CLK[1]	5		ns
t_{HDRE}	Receive Data Hold After SPT_CLK[1]	8		ns
t_{SCLKW}	SPT_CLK Width[2]	38.5		ns
t_{SPTCLK}	SPT_CLK Period[2]	77		ns
SWITCHING CHARACTERISTICS				
t_{DFSE}	Frame Sync Delay After SPT_CLK (Internally Generated Frame Sync in Transmit or Receive Mode)[3]		20	ns
t_{HOFSE}	Frame Sync Hold After SPT_CLK (Internally Generated Frame Sync in Transmit or Receive Mode)[3]	2		ns
t_{DDTE}	Transmit Data Delay After Transmit SPT_CLK[3]		20	ns
t_{HDTE}	Transmit Data Hold After Transmit SPT_CLK[3]	1		ns

[1] This specification is referenced to the sample edge.
[2] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external SPT_CLK.
[3] This specification is referenced to the drive edge.

Table 16. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
TIMING REQUIREMENTS				
t_{SDRI}	Receive Data Setup Before SPT_CLK[1]	25		ns
t_{HDRI}	Receive Data Hold After SPT_CLK[1]	0		ns
SWITCHING CHARACTERISTICS				
t_{DFSI}	Frame Sync Delay After SPT_CLK (Internally Generated Frame Sync in Transmit or Receive Mode)[2]		20	ns
t_{HOFSI}	Frame Sync Hold After SPT_CLK (Internally Generated Frame Sync in Transmit or Receive Mode)[2]	–8		ns
t_{DDTI}	Transmit Data Delay After SPT_CLK[2]		20	ns
t_{HDTI}	Transmit Data Hold After SPT_CLK[2]	–7		ns
t_{SCLKIW}	SPT_CLK Width	t_{PCLK} – 1.5		ns
t_{SPTCLK}	SPT_CLK Period	2 × t_{PCLK} – 1		ns

[1] This specification is referenced to the sample edge.
[2] This specification is referenced to the drive edge.

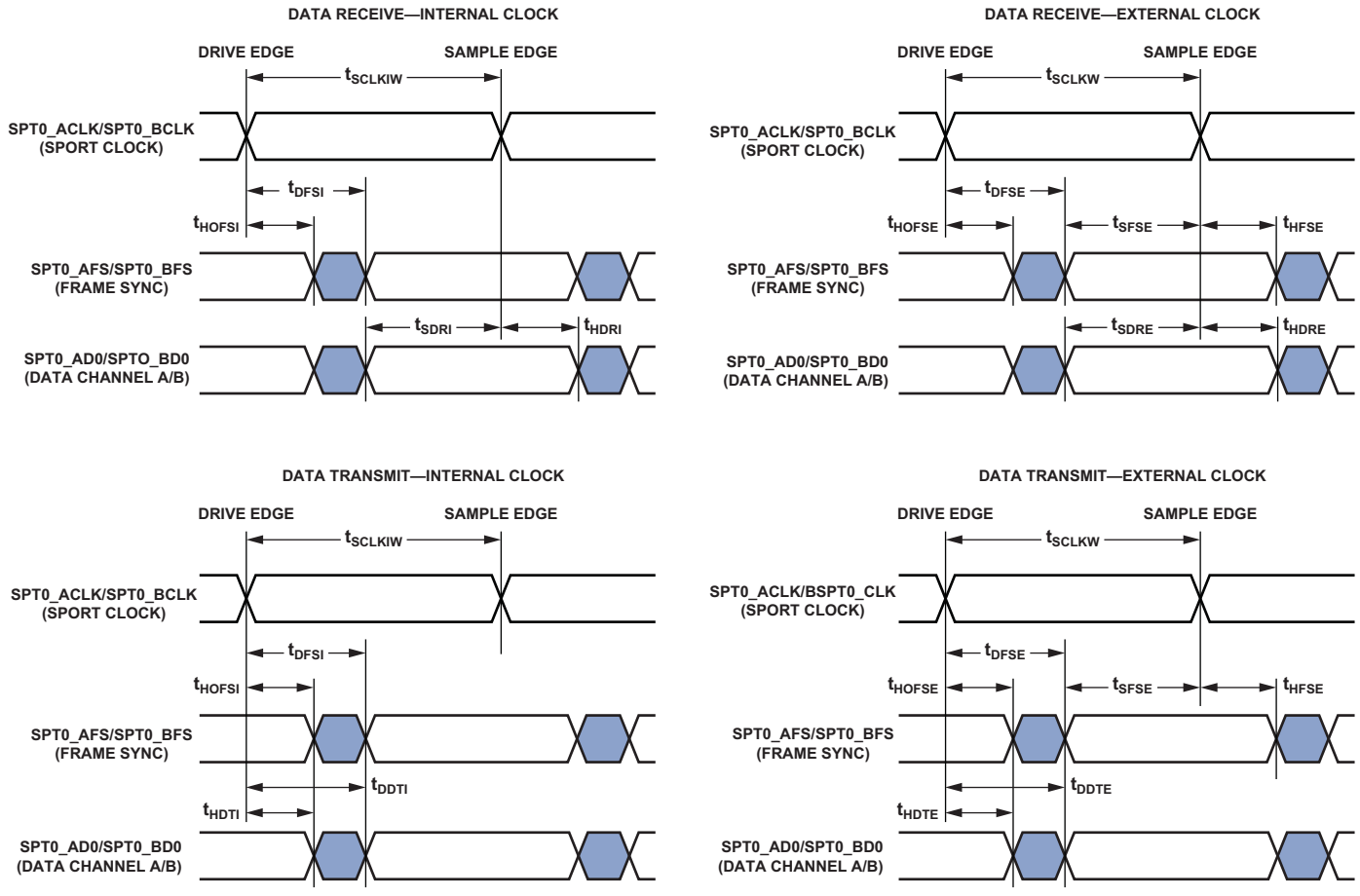


Figure 6. Serial Ports

SPI Timing

Table 18, Figure 8, and Figure 9 (for master mode) and Table 19, Figure 10, and Figure 11 (for slave mode) describe SPI timing specifications. High speed SPI (SPIH) can be used for high data rate peripherals.

Table 18. SPI Master Mode Timing[1]

Parameter		Min	Max	Unit
TIMING REQUIREMENTS				
t_{CS}	$\overline{CS}$ to SCLK Edge	$0.5 \times t_{PCLK} - 3$		ns
t_{SL}	SCLK Low Pulse Width	$t_{PCLK} - 3.5$		ns
t_{SH}	SCLK High Pulse Width	$t_{PCLK} - 3.5$		ns
t_{DSU}	Data Input Setup Time Before SCLK Edge	5		ns
t_{DHD}	Data Input Hold Time After SCLK Edge	20		ns
SWITCHING CHARACTERISTICS				
t_{DAV}	Data Output Valid After SCLK Edge		25	ns
t_{DOSU}	Data Output Setup Before SCLK Edge	$t_{PCLK} - 2.2$		ns
t_{SFS}	$\overline{CS}$ High After SCLK Edge	$0.5 \times t_{PCLK} - 3$		ns

[1] This specification is characterized with respect to double drive strength.

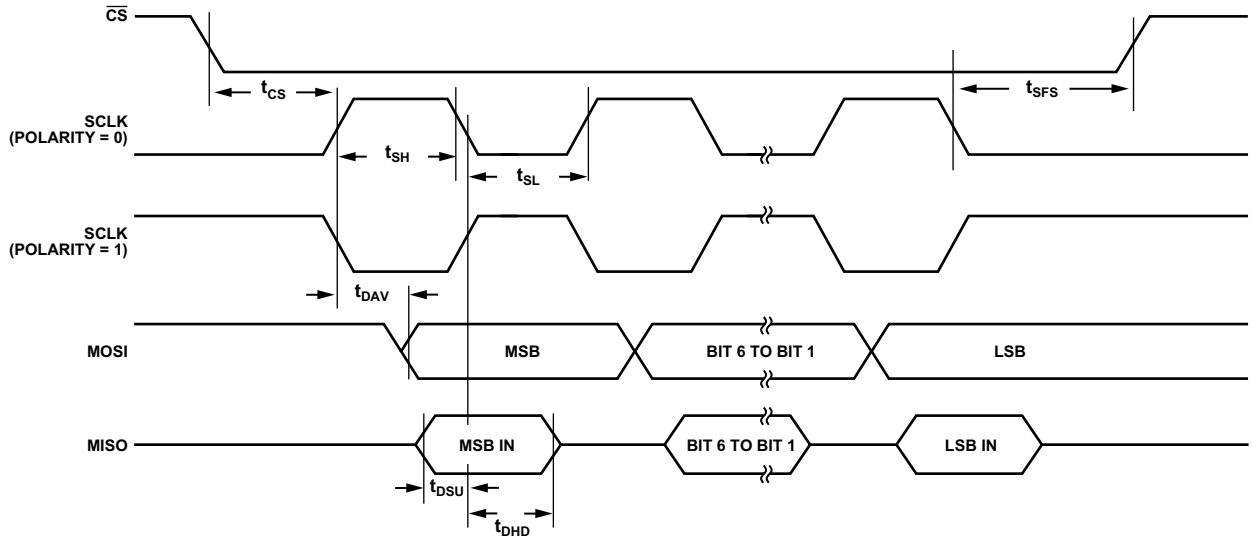


Figure 8. SPI Master Mode Timing (Phase Mode = 1)

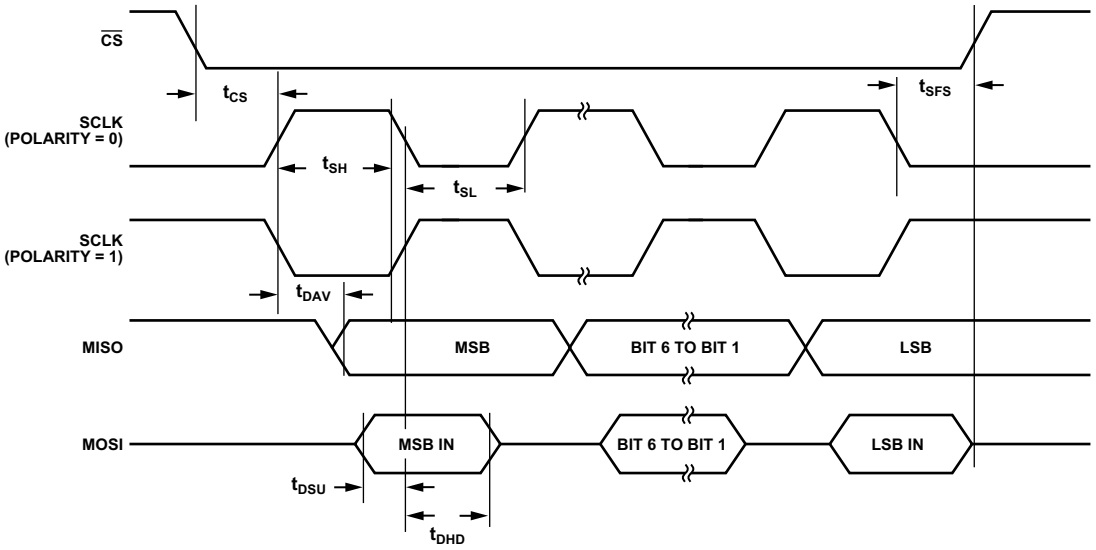


Figure 10. SPI Slave Mode Timing (Phase Mode = 1)

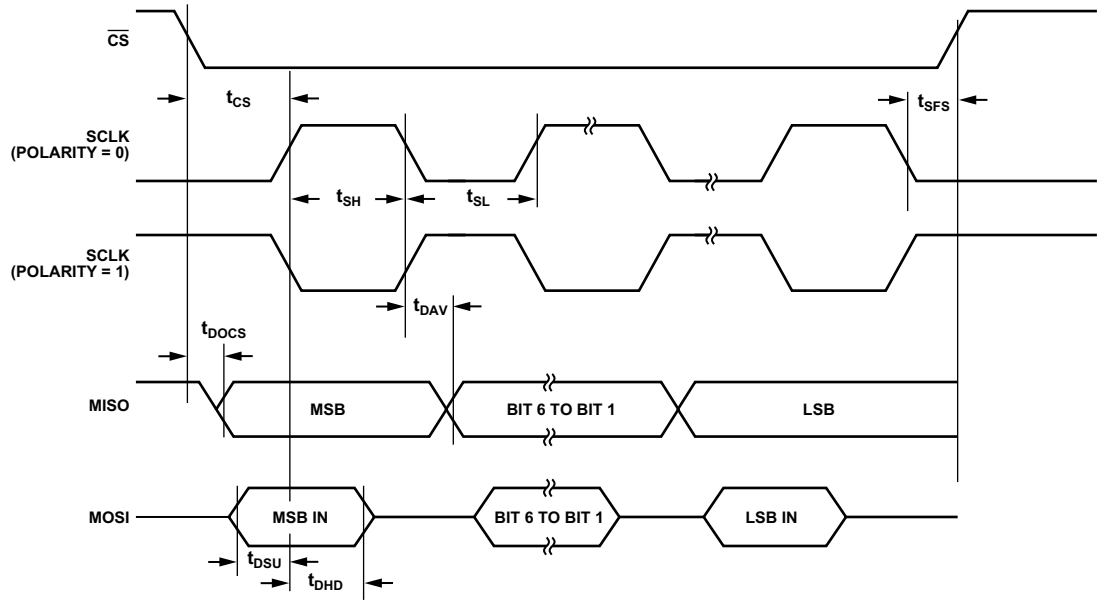


Figure 11. SPI Slave Mode Timing (Phase Mode = 0)

MCU TEST CONDITIONS

The ac signal specifications (timing parameters) that appear in this data sheet include output disable time, output enable time, and others. Timing is measured on signals when they cross the V_{MEAS} level as described in Figure 14. All delays (in ns or µs) are measured between the point that the first signal reaches V_{MEAS} and the point that the second signal reaches V_{MEAS}. The value of V_{MEAS} is set to $V_{BAT}/2$.

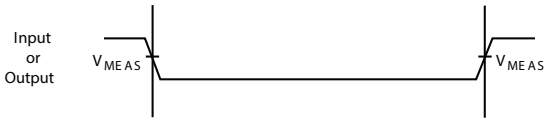
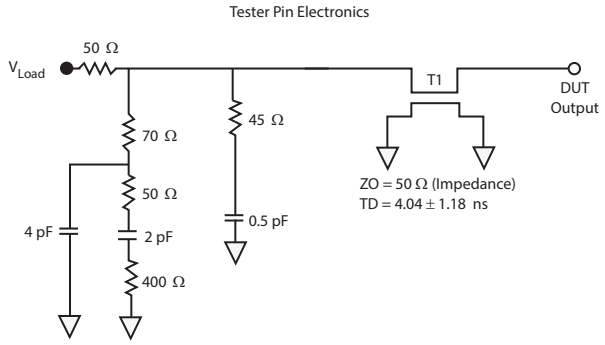


Figure 14. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFELECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD) IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 15. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

DRIVER TYPES

Table 22 shows driver types.

Table 22. Driver Types

Driver Type[1, 2, 3]	Associated Pins
Type A	P0_00, P0_01, P0_02, P0_03, P0_07, P0_10, P0_11, P0_12, P0_13, P0_15, P1_00, P1_01, P1_02, P1_03, P1_04, P1_05, P1_06, P1_07, P1_08, P1_09, P1_10, P1_15, P2_00, P2_01, P2_04, P2_05, P2_06, P2_07, P2_08, P2_09, P2_10, P2_11, $\overline{\text{SYS\_HWRST}}$
Type B	P0_08, P0_09, P0_14, P1_11, P1_12, P1_13, P1_14, P2_02
Type C	P0_04, P0_05
Type D	P0_06

[1] In single drive mode, the maximum source/sink capacity is 2 mA.
[2] In double drive mode, the maximum source/sink capacity is 4 mA.
[3] At maximum drive capacity, only 16 GPIOs are allowed to switch at any given point of time.

Figure 16 through Figure 21 show the typical current voltage characteristics for the output drivers of the MCU.

The curves represent the current drive capability of the output drivers as a function of output voltage.

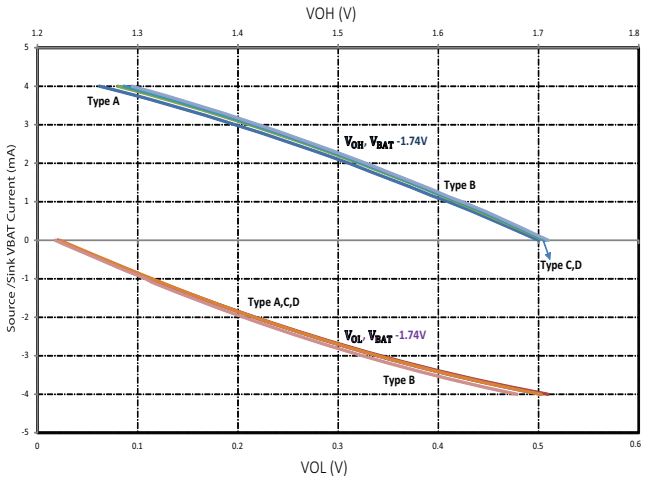


Figure 16. Output Double Drive Strength Characteristics (VBAT = 1.74 V)

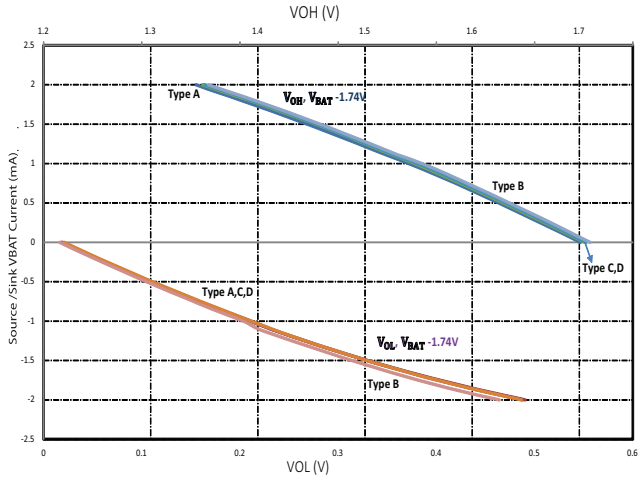


Figure 17. Output Single Drive Strength Characteristics (VBAT = 1.74 V)

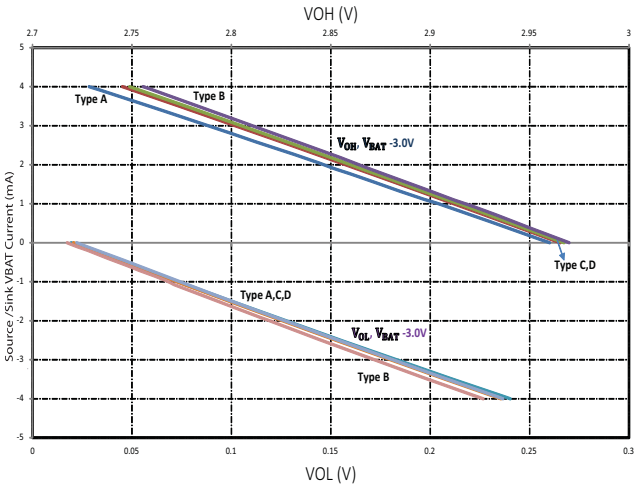


Figure 18. Output Double Drive Strength Characteristics (VBAT = 3.0 V)

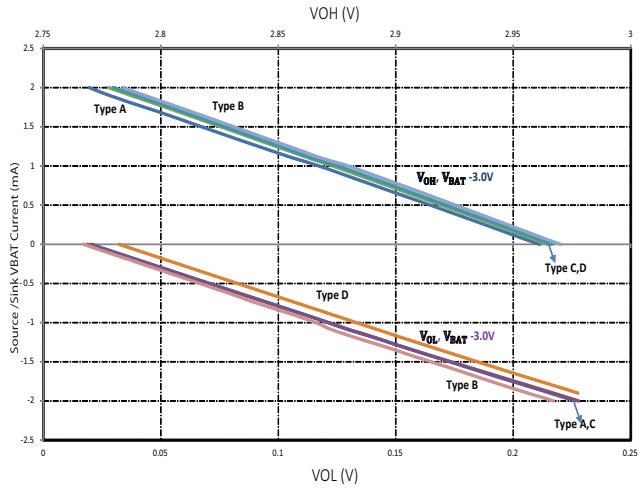


Figure 19. Output Single Drive Strength Characteristics (VBAT = 3.0 V)

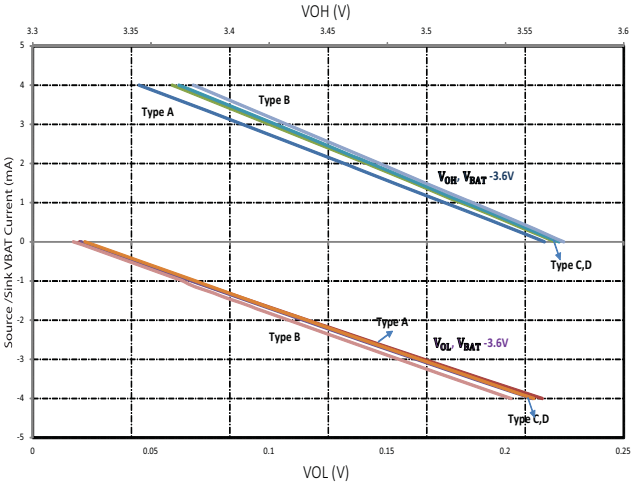


Figure 20. Output Double Drive Strength Characteristics (VBAT = 3.6 V)

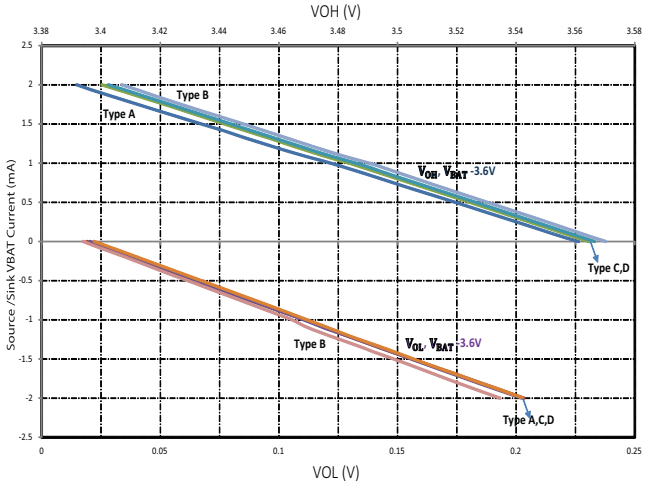


Figure 21. Output Single Drive Strength Characteristics (VBAT = 3.6 V)

PIN CONFIGURATION AND FUNCTION DESCRIPTION

Figure 22 shows an overview of signal placement on the 64-Lead LFCSP_WQ.

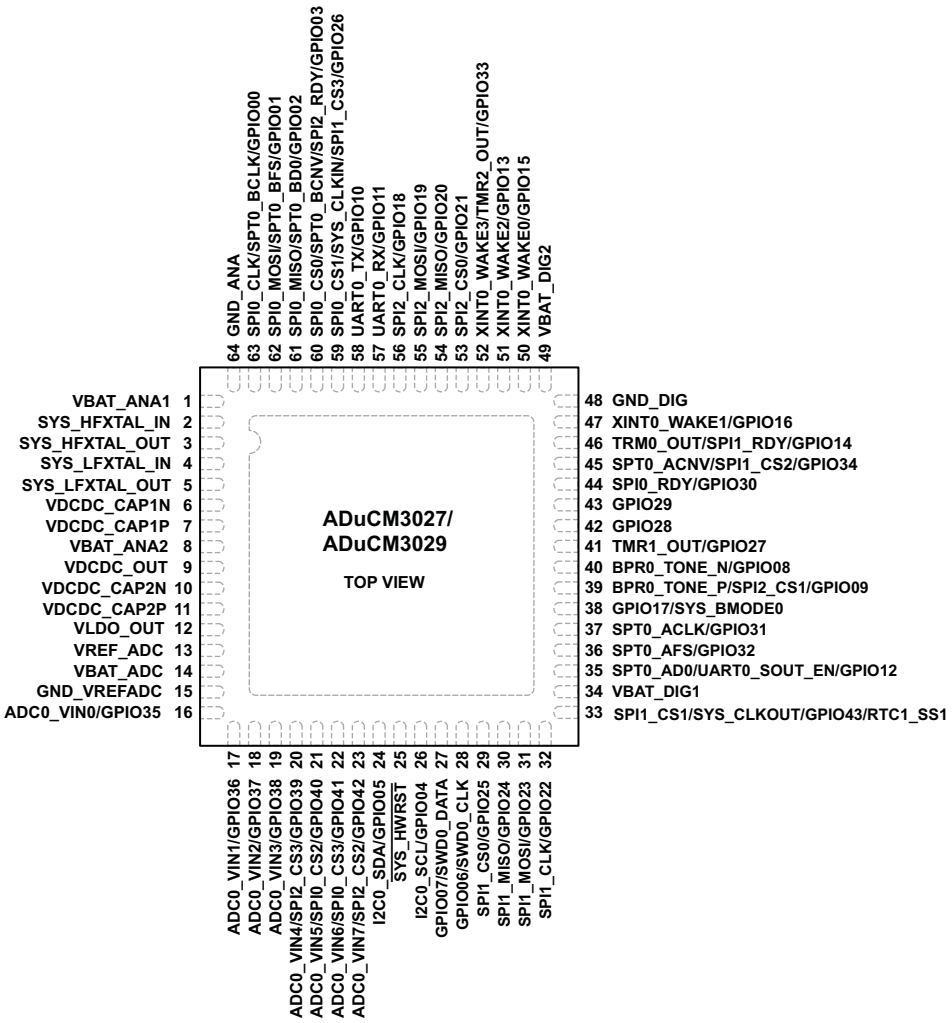


Figure 22. 64-Lead LFCSP Configuration

Figure 23 shows an overview of signal placement on the 54-Ball WLCSP.

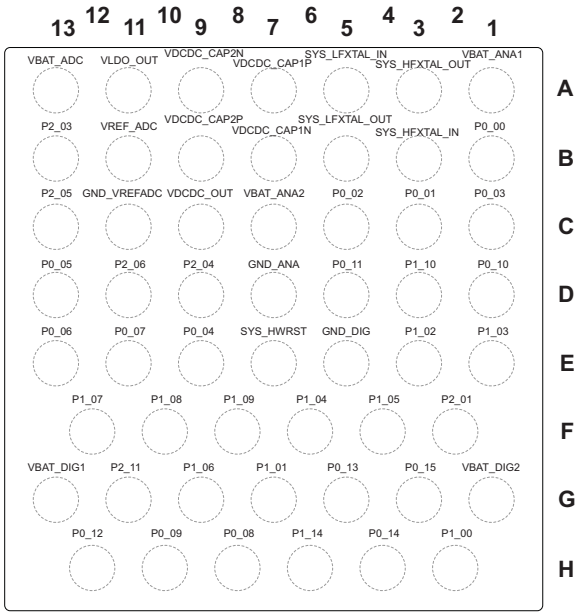


Figure 23. 54-Ball WLCSP Configuration

Table 24 lists the signal descriptions of the ADuCM3027/ADuCM3029 MCUs.

Table 24. Signal Functional Descriptions

GPIO Signal Name	Description
SPIn_CLK	SPI Clock. n = 0, 1, 2.
SPIn_MOSI	SPI Master Out Slave In. n = 0, 1, 2.
SPIn_MISO	SPI Master In Slave Out. n = 0, 1, 2.
SPIn_RDY	SPI Ready Signal. n = 0, 1, 2.
SPIn_CSm	SPI Chip Select Signal. n = 0, 1, 2 and m = 0, 1, 2, 3.
SPT0_ACLK	SPORT A Clock Signal.
SPT0_AFS	SPORT A Frame Sync.
SPT0_AD0	SPORT A Data Pin 0.
SPT0_ACNV	SPORT A Converter Signal for Interface with ADC.
SPT0_BCLK	SPORT B Clock Signal.
SPT0_BFS	SPORT B Frame Sync.
SPT0_BD0	SPORT B Data Pin 0.
SPT0_BCNV	SPORT B Converter Signal for Interface with ADC.
I2C0_SCL	I^2C Clock.
I2C0_SDA	I^2C Data.
SWD0_CLK	Serial Wire Debug Clock.
SWD0_DATA	Serial Wire Debug Data.
BPR0_TONE_N	Beeper Tone Negative Pin.
BPR0_TONE_P	Beeper Tone Positive Pin.
UART0_TX	UART Transmit Pin.
UART0_RX	UART Receive Pin.
UART0_SOUT_EN	UART Serial Data Out Pin.
XINT0_WAKEn	System Wake-Up Pin. Wake Up from Flexi/Hibernate/Shutdown Modes[1]. n = 0, 1, 2, 3.
TMRn_OUT	Timer Output Pin. n = 0, 1, 2.
SYS_BMODE0	Boot Mode Pin.
SYS_CLKIN	External Clock In Pin.
SYS_CLKOUT	External Clock Out Pin.
RTC1_SS1	RTC1 SensorStrobe Pin.
ADC0_VINn	ADC Voltage Input Pin. n = 0, 1, 2, 3, 4, 5, 6, 7.

[1] For shutdown, XINT0_WAKE3 is not capable of waking the device from shutdown mode.

Table 26. Pin Function Descriptions, 54-Ball WLCSP (Continued)

Ball No.	GPIO	Pin Label	Description	GPIO Pull
G05	P0_13	XINT0_WAKE2/GPIO13		PU
G07	P1_01	GPIO17/SYS_BMODE0		PU
G09	P1_06	SPI1_CLK/GPIO22		PU
G11	P2_11	SPI1_CS1/SYS_CLKOUT/GPIO43/RTC1_SS1		PU
G13		VBAT_DIG1	Digital 3 V Supply.	
H02	P1_00	XINT0_WAKE1/GPIO16		PU
H04	P0_14	TMR0_OUT/SPI1_RDY/GPIO14		PU
H06	P1_14	SPI0_RDY/GPIO30		PU
H08	P0_08	BPR0_TONE_N/GPIO08		PU
H10	P0_09	BPR0_TONE_P/SPI2_CS1/GPIO09		PU
H12	P0_12	SPT0_AD0/GPIO12/UART0_SOUT_EN		PU

ORDERING GUIDE

Model[1]	Description	Temperature[2, 3]	Package Description	Package Option
ADUCM3027BCBZ-RL	ULP ARM Cortex-M3 with 128 KB Embedded Flash	−40°C to +85°C	54-Ball WLCSP, 13″ Reel	CB-54-1
ADUCM3027BCBZ-R7	ULP ARM Cortex-M3 with 128 KB Embedded Flash	−40°C to +85°C	54-Ball WLCSP, 7″ Reel	CB-54-1
ADUCM3027BCPZ	ULP ARM Cortex-M3 with 128 KB Embedded Flash	−40°C to +85°C	64-Lead LFCSP	CP-64-16
ADUCM3027BCPZ-RL	ULP ARM Cortex-M3 with 128 KB Embedded Flash	−40°C to +85°C	64-Lead LFCSP, 13″ Reel	CP-64-16
ADUCM3027BCPZ-R7	ULP ARM Cortex-M3 with 128 KB Embedded Flash	−40°C to +85°C	64-Lead LFCSP, 7″ Reel	CP-64-16
ADUCM3029BCBZ-RL	ULP ARM Cortex-M3 with 256 KB Embedded Flash	−40°C to +85°C	54-Ball WLCSP, 13″ Reel	CB-54-1
ADUCM3029BCBZ-R7	ULP ARM Cortex-M3 with 256 KB Embedded Flash	−40°C to +85°C	54-Ball WLCSP, 7″ Reel	CB-54-1
ADUCM3029BCPZ	ULP ARM Cortex-M3 with 256 KB Embedded Flash	−40°C to +85°C	64-Lead LFCSP	CP-64-16
ADUCM3029BCPZ-RL	ULP ARM Cortex-M3 with 256 KB Embedded Flash	−40°C to +85°C	64-Lead LFCSP, 13″ Reel	CP-64-16
ADUCM3029BCPZ-R7	ULP ARM Cortex-M3 with 256 KB Embedded Flash	−40°C to +85°C	64-Lead LFCSP, 7″ Reel	CP-64-16
ADZS-UCM3029EZLITE	ADuCM3029 Evaluation Kit	−40°C to +85°C	64-Lead LFCSP	CP-64-16

[1] Z = RoHS Compliant Part.
[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. See the Absolute Maximum Ratings section for T_J (junction temperature) specification which is the only temperature specification.
[3] These are preproduction devices. See ENG-Grade agreement for details.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

D14168-0-3/17(0)