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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	-
Core Size	-
Speed	-
Connectivity	-
Peripherals	-
Number of I/O	-
Program Memory Size	-
Program Memory Type	-
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	-
Data Converters	-
Oscillator Type	-
Operating Temperature	-
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aducm3029bcpz-r7

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REVISION HISTORY

3/2017—Revision 0: Initial Version

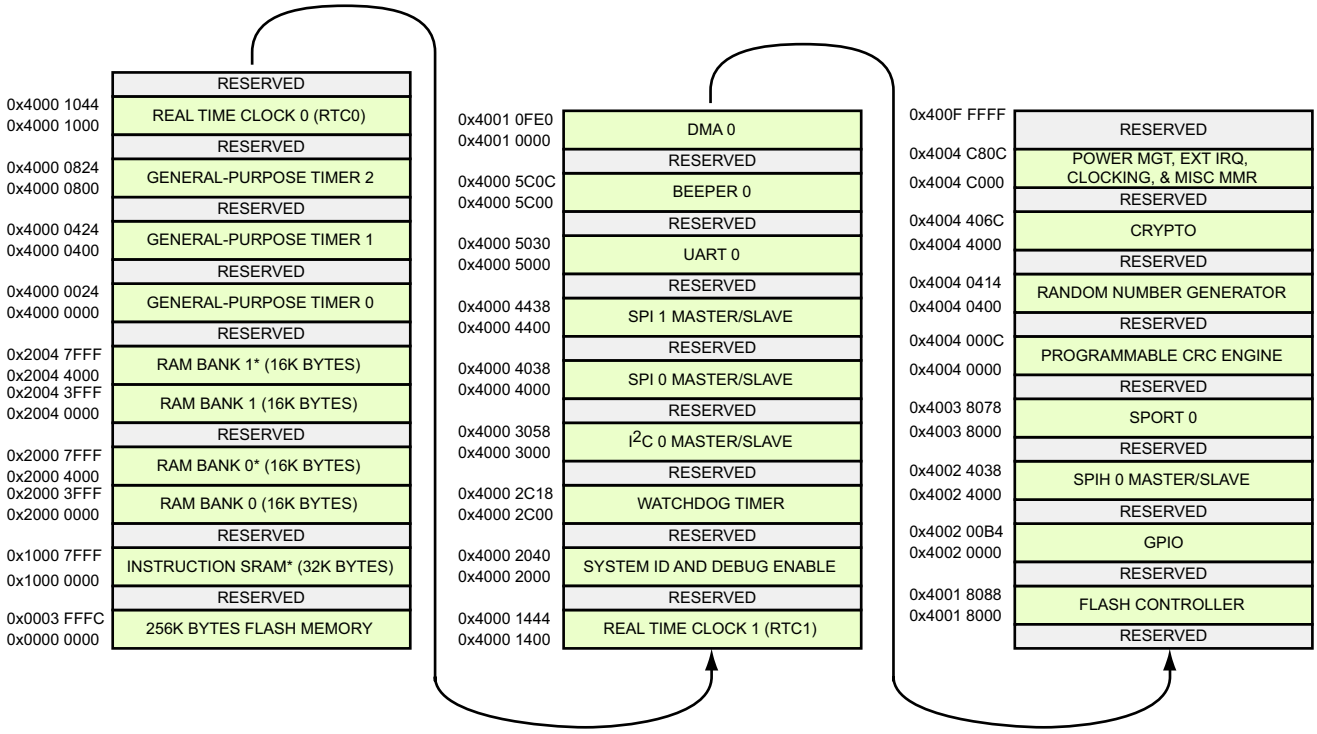


Figure 2. ADuCM3027/ADuCM3029 Memory Map

Cache Controller

The ADuCM3027/ADuCM3029 MCUs have an optional 4 KB instruction cache. In certain applications, enabling the cache and executing the code can result in lower power consumption than operating directly from flash. When the cache controller is enabled, 4 KB of instruction SRAM is reserved as cache memory. In hibernate mode, the cache memory is not retained.

SYSTEM AND INTEGRATION FEATURES

The ADuCM3027/ADuCM3029 MCUs provide several features that ease system integration.

Reset

There are four types of resets: external, power-on, watchdog timeout, and software system reset. The software system reset is provided as part of the Cortex-M3 core.

The $\overline{\text{SYS\_HWRST}}$ pin is toggled to perform a hardware reset.

Booting

The ADuCM3027/ADuCM3029 MCUs support two boot modes: booting from internal flash and upgrading software through UART download. If the SYS_BMODE0 pin (GPIO17) is pulled low during power-up or a hard reset, the MCU enters into serial download mode.

In this mode, an on-chip loader routine initiates in the kernel, which configures the UART port and communicates with the host to manage the firmware upgrade via a specific serial download protocol.

Table 2. Boot Modes

Boot Mode	Description
0	UART download mode.
1	Flash boot. Boot from integrated flash memory.

Power Management

The ADuCM3027/ADuCM3029 MCUs have an integrated power management system that optimizes performance and extends battery life of the devices.

The power management system consists of the following:

- Integrated 1.2 V low dropout regulator (LDO) and optional capacitive buck regulator
- Integrated power switches for low standby current in hibernate and shutdown modes

The main features of the ADC subsystem include the following:

- 12-bit resolution.
- Programmable ADC update rate from 10 KSPS to 1.8 MSPS.
- Integrated input multiplexer that supports up to eight channels.
- Temperature sensing support.
- Battery monitoring support.
- Software selectable on-chip reference voltage generation—1.25 V and 2.5 V.
- Software selectable internal or external reference.
- Autocycle mode—ability to automatically select a sequence of input channels for conversion.
- Averaging function—converted data on single or multiple channels can be averaged up to 256 samples.
- Alert function—internal digital comparator for ADC0_VIN0, ADC0_VIN1, ADC0_VIN2, and ADC0_VIN3 channels. An interrupt is generated if the digital comparator detects an ADC result above or below a user defined threshold.
- Dedicated DMA channel support.
- Each channel, including temperature sensor and battery monitoring, has a data register for conversion result.

Clocking

The ADuCM3027/ADuCM3029 MCUs have the following clocking options:

- 26 MHz
  - Internal oscillator—HFOSC (26 MHz)
  - External crystal oscillator—HFXTAL (26 MHz or 16 MHz)
  - GPIO clock in—SYS_CLKIN
- 32 kHz
  - Internal oscillator—LFOSC
  - External crystal oscillator—LFXTAL

The clock options have software configurability with the following exceptions:

- HFOSC cannot be disabled when using an internal buck regulator.
- LFOSC cannot be disabled even if using LFXTAL.

Real-Time Clock (RTC)

The ADuCM3027/ADuCM3029 MCUs have two real-time clock blocks—RTC0 and RTC1 (FLEX_RTC). The clock blocks share a low power crystal oscillation circuit that operates in conjunction with a 32,768 Hz external crystal.

The RTC has an alarm that interrupts the core when the programmed alarm value matches the RTC count. The software enables and configures the RTC.

The RTC also has a digital trim capability to allow a positive or negative adjustment to the RTC count at fixed intervals.

The FLEX_RTC supports SensorStrobe mechanism. Using this mechanism, the ADuCM3027/ADuCM3029 MCUs can be used as a programmable clock generator in some power modes, including hibernate mode. In this way, the external sensors can have their timing domains mastered by the ADuCM3027/ADuCM3029 MCUs, as SensorStrobe can output a programmable divider from the FLEX_RTC, which can operate up to a resolution of 30.7 µs. The sensors and MCU are in sync, which removes the need for additional resampling of data to time align it.

In the absence of this mechanism,

- The external sensor uses an RC oscillator (~±30% typical variation). The MCU must sample the data and resample it on the time domain of the MCU before using it.

Or

- The MCU remains in a higher power state and drives each data conversion on the sensor side.

This mechanism allows the ADuCM3027/ADuCM3029 MCUs to be in a lower power state for a long duration and avoids unnecessary data processing which extends the battery life of the end product.

SPECIFICATIONS

For information about product specifications, contact your Analog Devices, Inc. representative.

OPERATING CONDITIONS

Parameter		Conditions	Min	Typ	Max	Unit
V_{BAT}[1, 2]	External Battery Supply Voltage		1.74	3.0	3.6	V
V_{IH}	High Level Input Voltage	V_{BAT} = 3.6 V	2.5			V
V_{IL}	Low Level Input Voltage	V_{BAT} = 1.74 V			0.45	V
V_{BAT_ADC}	ADC Supply Voltage		1.74	3.0	3.6	V
T_J	Junction Temperature	$T_{AMBIENT}$ = −40°C to +85°C	−40		+85	°C

[1] The voltage must remain powered even if the associated function is not used.
[2] Value applies to the VBAT_ANA1,VBAT_ANA2,VBAT_DIG1, and VBAT_DIG2 pins.

ELECTRICAL CHARACTERISTICS

Parameter		Conditions	Min	Typ	Max	Unit
V_{OH}[1]	High Level Output Voltage	V_{BAT} = minimum V, I_{OH} = −1.0 mA	1.4			V
V_{OL}[1]	Low Level Output Voltage	V_{BAT} = minimum V, I_{OL} = 1.0 mA			0.4	V
I_{IHPU}[2]	High Level Input Current Pull-Up	V_{BAT} = maximum V, V_{IN} = maximum V_{BAT}		0.01	1	µA
I_{ILPU}[2]	Low Level Input Current Pull-Up	V_{BAT} = maximum V, V_{IN} = 0 V			100	µA
I_{OZH}[3]	Three-State Leakage Current	V_{BAT} = maximum V, V_{IN} = maximum V_{BAT}		0.01	1	µA
I_{OZL}[3]	Three-State Leakage Current	V_{BAT} = maximum V, V_{IN} = 0 V		0.01	1	µA
I_{OZLPU}[4]	Three-State Leakage Current Pull-Up	V_{BAT} = maximum V, V_{IN} = 0 V			100	µA
I_{OZHPU}[4]	Three-State Leakage Current Pull-Up	V_{BAT} = maximum V, V_{IN} = maximum V_{BAT}			1	µA
I_{OZLPD}[5]	Three-State Leakage Current Pull-Down	V_{BAT} = maximum V, V_{IN} = 0 V			1	µA
I_{OZHPD}[5]	Three-State Leakage Current Pull-Down	V_{BAT} = maximum V, V_{IN} = maximum V_{BAT}			100	µA
C_{IN}	Input Capacitance	T_J = 25°C		10		pF

[1] Applies to the output and bidirectional pins: P1_10, P0_10, P0_11, P1_02, P1_03, P1_04, P1_05, P2_01, P0_13, P0_15, P1_00, P1_01, P1_15, P2_00, P0_12, P2_11, P1_06, P1_07, P1_08, P1_09, P0_00, P0_01, P0_02, P0_03, P0_06, P0_07, P2_03, P2_04, P2_05, P2_06, P2_07, P2_08, P2_09, P2_10, P0_04, P0_05, P0_14, P2_02, P1_14, P1_13, P1_12, P1_11, P0_08, and P0_09.
[2] Applies to the input pin with pull-up: $\overline{\text{SYS\_HWRST}}$.
[3] Applies to the three-statable pins: P1_10, P0_10, P0_11, P1_02, P1_03, P1_04, P1_05, P2_01, P0_13, P0_15, P1_00, P1_15, P2_00, P0_12, P2_11, P1_06, P1_07, P1_08, P1_09, P0_00, P0_01, P0_02, P0_03, P2_03, P2_04, P2_05, P2_06, P2_07, P2_08, P2_09, P2_10, P0_04, P0_05, P0_14, P2_02, P1_14, P1_13, P1_12, P1_11, P0_08, and P0_09.
[4] Applies to the three-statable pins with pull-ups: P1_10, P0_10, P0_11, P1_02, P1_03, P1_04, P1_05, P2_01, P0_13, P0_15, P1_00, P1_15, P2_00, P0_12, P2_11, P1_06, P1_07, P1_08, P1_09, P0_00, P0_01, P0_02, P0_03, P2_03, P2_04, P2_05, P2_06, P2_07, P2_08, P2_09, P2_10, P0_04, P0_05, P0_14, P2_02, P1_14, P1_13, P1_12, P1_11, P0_08, P0_09, P0_07, and P1_01.
[5] Applies to the three-statable pin with pull-down: P0_06.

SYSTEM CLOCKS/TIMERS

Table 7 and Table 8 show the system clock specifications for the ADuCM3027/ADuCM3029 MCUs.

Platform External Crystal Oscillator

Table 7. Platform External Crystal Oscillator Specifications

Parameter	Min	Typ	Max	Unit	Conditions
LOW FREQUENCY EXTERNAL CRYSTAL OSCILLATOR (LFXTAL)					
$C_{EXT1} = C_{EXT2}$	6		10	pF	External capacitor, $C_{EXT1} = C_{EXT2}$ (symmetrical load), for $C_L \leq 5$ pF (maximum) and ESR = 30 kΩ (maximum). C_{EXT1}, C_{EXT2} must be selected considering the printed circuit board (PCB) trace capacitance due to routing.
Frequency		32,768		Hz	
HIGH FREQUENCY EXTERNAL CRYSTAL OSCILLATOR (HFXTAL)					
$C_{EXT1} = C_{EXT2}$			20	pF	External capacitor, $C_{EXT1} = C_{EXT2}$ (symmetrical load), for C_L = 10 pF (maximum) and ESR = 50 Ω (maximum). C_{EXT1}, C_{EXT2} must be selected considering the PCB trace capacitance due to routing.
Frequency		26		MHz	

On-Chip RC Oscillator

Table 8. On-Chip RC Oscillator Specifications

Parameter	Min	Typ	Max	Unit	Conditions
HIGH FREQUENCY RC OSCILLATOR (HFOSC)					
Frequency	25.09	26	26.728	MHz	
LOW FREQUENCY RC OSCILLATOR (LFOSC)					
Frequency	30,800	32,768	34,407	Hz	

TIMING SPECIFICATIONS

Specifications are subject to change without notice.

Reset Timing

Table 13 and Figure 5 describe reset timing.

Table 13. Reset Timing

Parameter		Min	Max	Unit
TIMING REQUIREMENTS				
t_{WRST}	$\overline{SYS\_HWRST}$ Asserted Pulse Width Low[1]	4		µs

[1] Applies after power-up sequence is complete.

Figure 5. Reset Timing

System Clock and PLL

Table 14 describes system clock and phase-locked loop (PLL) specifications.

Table 14. System Clock and PLL

Parameter		Min	Max	Unit
TIMING REQUIREMENTS				
t_{CK}	PLL Input CLKIN Period[1]	38.5	62.5	ns
f_{PLL}	PLL Output Frequency [2, 3]	16	60	MHz
t_{PCLK}	System Peripheral Clock Period	38.5	154	ns
t_{HCLK}	Advanced High Performance Bus (AHB) Subsystem Clock Period	38.5	154	ns

[1] The input to the PLL can come either from the high frequency external crystal or from the high frequency internal RC oscillator. Refer to the ADuCM302x Ultra Low Power ARM Cortex-M3 MCU with Integrated Power Management Hardware Reference.

[2] For the minimum value, the recommended settings are PLL_MSEL = 13, PLL_NSEL = 16, and PLL_DIV2 = 1 for PLL input clock = 26 MHz; and PLL_MSEL = 13, PLL_NSEL = 26, and PLL_DIV2 = 1 for PLL input clock = 16 MHz.

[3] For the maximum value, the recommended settings are PLL_MSEL = 13, PLL_NSEL = 30, and PLL_DIV2 = 0 for PLL input clock = 26 MHz; and PLL_MSEL = 8, PLL_NSEL = 30, and PLL_DIV2 = 0 for PLL input clock= 16 MHz.

Serial Ports

To determine whether communication is possible between two devices at a particular clock speed, confirm the following specifications:

- Frame sync delay and frame sync setup and hold
- Data delay and data setup and hold
- Serial clock (SPT_CLK) width

In Figure 6, use the rising edge or the falling edge of SPT_CLK (external or internal) as the active sampling edge.

When externally generated, the SPORT clock is called $f_{SPTCLKEXT}$.

$$t_{SPTCLKEXT} = \frac{1}{f_{SPTCLKEXT}}$$

When internally generated, the programmed SPORT clock ($f_{SPTCLKPROG}$) frequency is set by the following equation:

$$f_{SPTCLKPROG} = \frac{f_{PCLK}}{2 \times (CLKDIV + 1)}$$

where CLKDIV is a field in the SPORT_DIV register that can be set from 0 to 65535.

Table 15. Serial Ports—External Clock

Parameter		Min	Max	Unit
TIMING REQUIREMENTS				
t_{SFSE}	Frame Sync Setup Before SPT_CLK (Externally Generated Frame Sync in Transmit or Receive Mode)[1]	5		ns
t_{HFSE}	Frame Sync Hold After SPT_CLK (Externally Generated Frame Sync in Transmit or Receive Mode)[1]	5		ns
t_{SDRE}	Receive Data Setup Before Receive SPT_CLK[1]	5		ns
t_{HDRE}	Receive Data Hold After SPT_CLK[1]	8		ns
t_{SCLKW}	SPT_CLK Width[2]	38.5		ns
t_{SPTCLK}	SPT_CLK Period[2]	77		ns
SWITCHING CHARACTERISTICS				
t_{DFSE}	Frame Sync Delay After SPT_CLK (Internally Generated Frame Sync in Transmit or Receive Mode)[3]		20	ns
t_{HOFSE}	Frame Sync Hold After SPT_CLK (Internally Generated Frame Sync in Transmit or Receive Mode)[3]	2		ns
t_{DDTE}	Transmit Data Delay After Transmit SPT_CLK[3]		20	ns
t_{HDTE}	Transmit Data Hold After Transmit SPT_CLK[3]	1		ns

[1] This specification is referenced to the sample edge.
[2] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external SPT_CLK.
[3] This specification is referenced to the drive edge.

SPI Timing

Table 18, Figure 8, and Figure 9 (for master mode) and Table 19, Figure 10, and Figure 11 (for slave mode) describe SPI timing specifications. High speed SPI (SPIH) can be used for high data rate peripherals.

Table 18. SPI Master Mode Timing[1]

Parameter		Min	Max	Unit
TIMING REQUIREMENTS				
t_{CS}	$\overline{CS}$ to SCLK Edge	$0.5 \times t_{PCLK} - 3$		ns
t_{SL}	SCLK Low Pulse Width	$t_{PCLK} - 3.5$		ns
t_{SH}	SCLK High Pulse Width	$t_{PCLK} - 3.5$		ns
t_{DSU}	Data Input Setup Time Before SCLK Edge	5		ns
t_{DHD}	Data Input Hold Time After SCLK Edge	20		ns
SWITCHING CHARACTERISTICS				
t_{DAV}	Data Output Valid After SCLK Edge		25	ns
t_{DOSU}	Data Output Setup Before SCLK Edge	$t_{PCLK} - 2.2$		ns
t_{SFS}	$\overline{CS}$ High After SCLK Edge	$0.5 \times t_{PCLK} - 3$		ns

[1] This specification is characterized with respect to double drive strength.

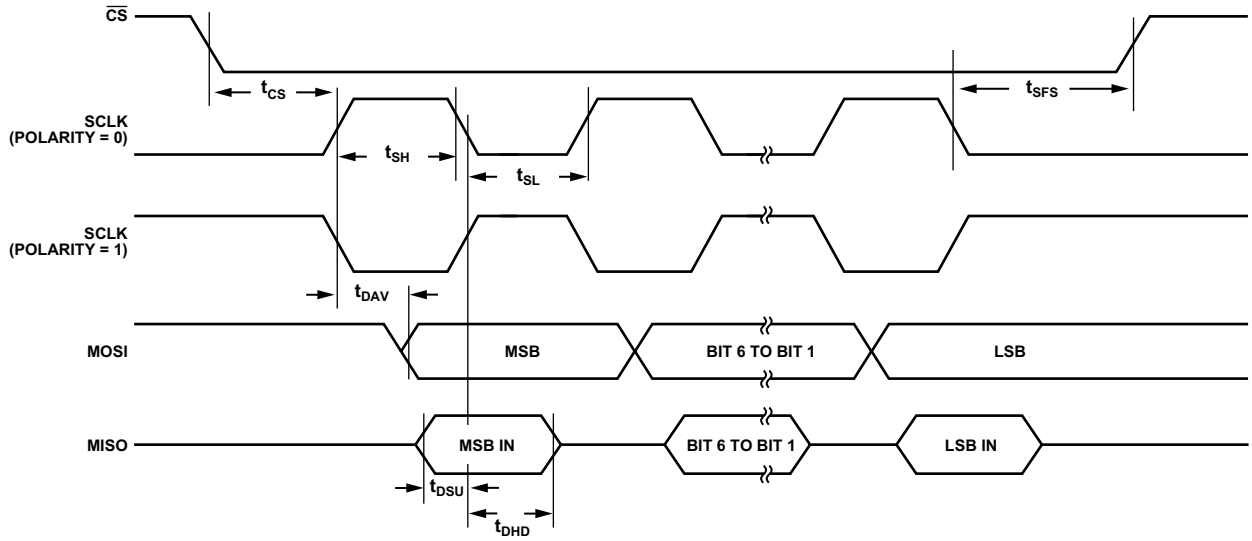


Figure 8. SPI Master Mode Timing (Phase Mode = 1)

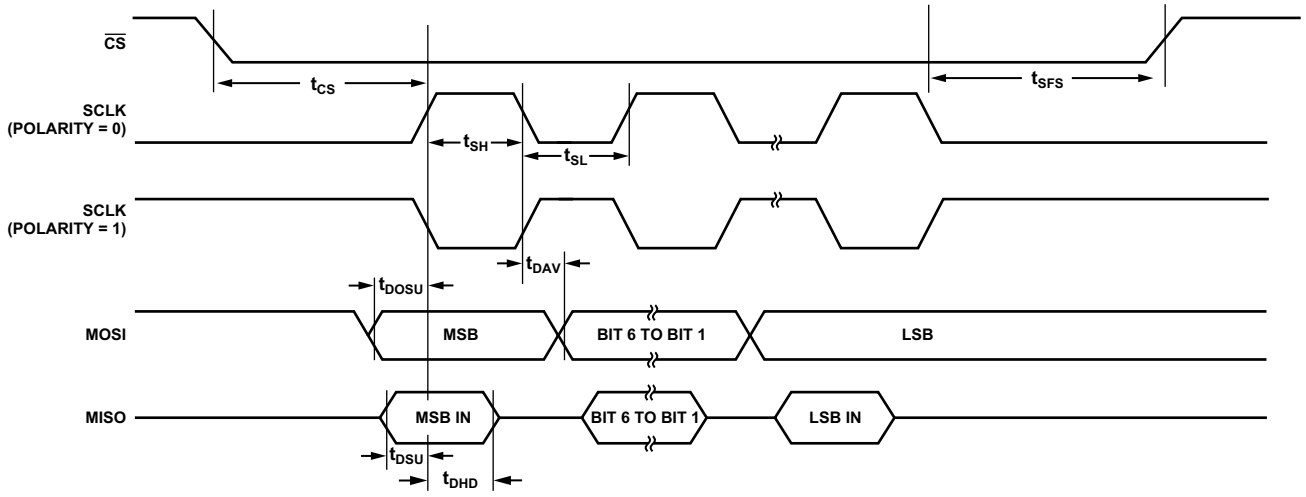


Figure 9. SPI Master Mode Timing (Phase Mode = 0)

Table 19. SPI Slave Mode Timing

Parameter		Min	Max	Unit
TIMING REQUIREMENTS				
t_{CS}	$\overline{CS}$ to SCLK Edge	38.5		ns
t_{SL}	SCLK Low Pulse Width	38.5		ns
t_{SH}	SCLK High Pulse Width	38.5		ns
t_{DSU}	Data Input Setup Time Before SCLK Edge	6		ns
t_{DHD}	Data Input Hold Time After SCLK Edge	8		ns
SWITCHING CHARACTERISTICS				
t_{DAV}	Data Output Valid After SCLK Edge	25		ns
t_{DOCS}	Data Output Valid After $\overline{CS}$ Edge		20	ns
t_{SFS}	$\overline{CS}$ High After SCLK Edge	38.5		ns

General-Purpose Port Timing

Table 20 and Figure 12 describe general-purpose port timing.

Table 20. General-Purpose Port Timing

Parameter		Min	Max	Unit
TIMING REQUIREMENTS				
t_{WFI}	General-Purpose Port Pin Input Pulse Width	$4 \times t_{PCLK}$		ns

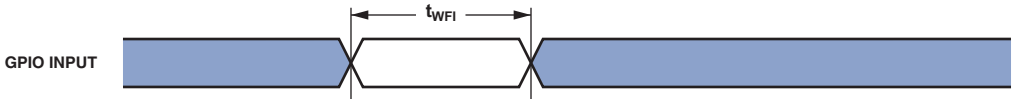


Figure 12. General-Purpose Port Timing

Timer PWM_OUT Cycle Timing

Table 21 and Figure 13 describe timer PWM_OUT cycle timing.

Table 21. Timer PWM_OUT Cycle Timing

Parameter		Min	Max	Unit
SWITCHING CHARACTERISTICS				
t_{PWMO}	Timer Pulse Width Output	$4 \times t_{PCLK} - 6$	$256 \times (2^{16} - 1)$	ns

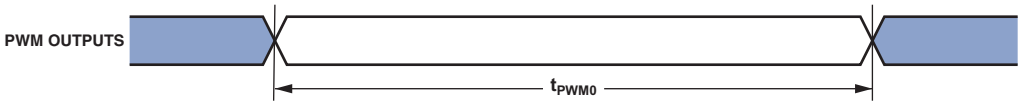


Figure 13. Timer PWM_OUT Cycle Timing

MCU TEST CONDITIONS

The ac signal specifications (timing parameters) that appear in this data sheet include output disable time, output enable time, and others. Timing is measured on signals when they cross the V_{MEAS} level as described in Figure 14. All delays (in ns or µs) are measured between the point that the first signal reaches V_{MEAS} and the point that the second signal reaches V_{MEAS}. The value of V_{MEAS} is set to $V_{BAT}/2$.

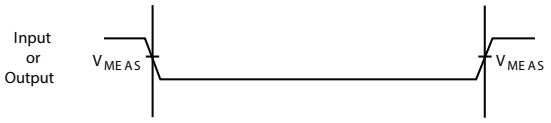
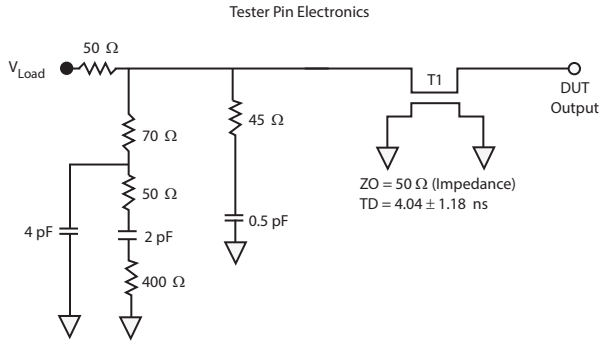


Figure 14. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFELECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD) IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 15. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

DRIVER TYPES

Table 22 shows driver types.

Table 22. Driver Types

Driver Type[1, 2, 3]	Associated Pins
Type A	P0_00, P0_01, P0_02, P0_03, P0_07, P0_10, P0_11, P0_12, P0_13, P0_15, P1_00, P1_01, P1_02, P1_03, P1_04, P1_05, P1_06, P1_07, P1_08, P1_09, P1_10, P1_15, P2_00, P2_01, P2_04, P2_05, P2_06, P2_07, P2_08, P2_09, P2_10, P2_11, $\overline{\text{SYS\_HWRST}}$
Type B	P0_08, P0_09, P0_14, P1_11, P1_12, P1_13, P1_14, P2_02
Type C	P0_04, P0_05
Type D	P0_06

[1] In single drive mode, the maximum source/sink capacity is 2 mA.
[2] In double drive mode, the maximum source/sink capacity is 4 mA.
[3] At maximum drive capacity, only 16 GPIOs are allowed to switch at any given point of time.

Figure 16 through Figure 21 show the typical current voltage characteristics for the output drivers of the MCU.

The curves represent the current drive capability of the output drivers as a function of output voltage.

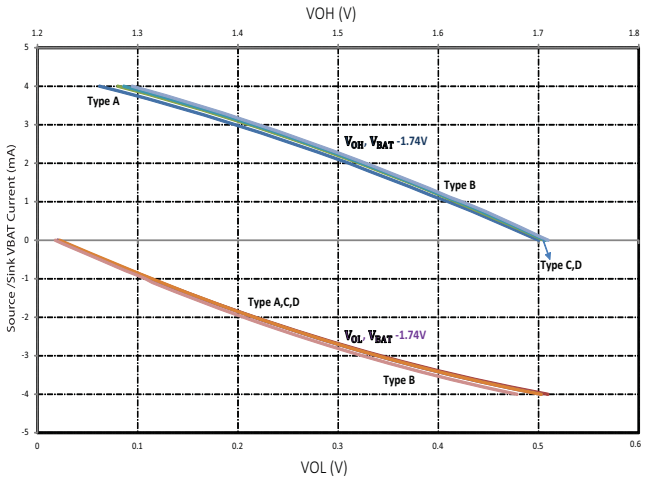


Figure 16. Output Double Drive Strength Characteristics (VBAT = 1.74 V)

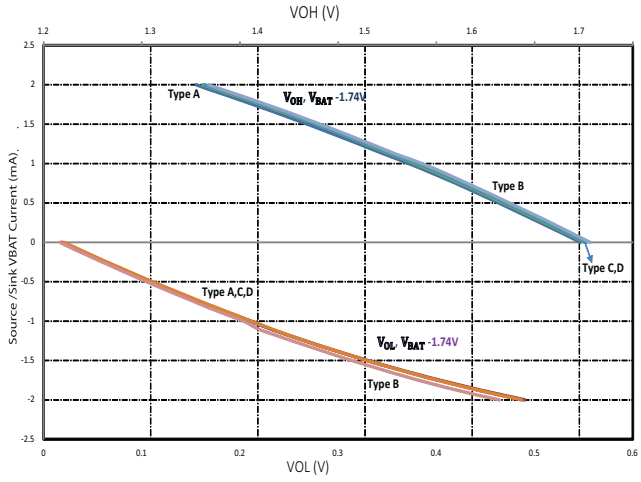


Figure 17. Output Single Drive Strength Characteristics (VBAT = 1.74 V)

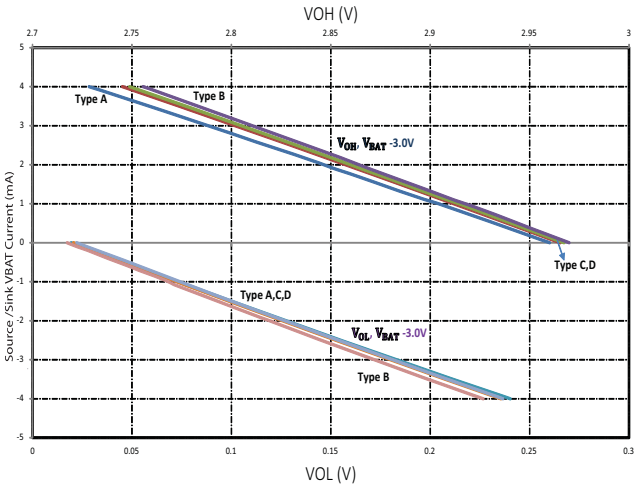


Figure 18. Output Double Drive Strength Characteristics (VBAT = 3.0 V)

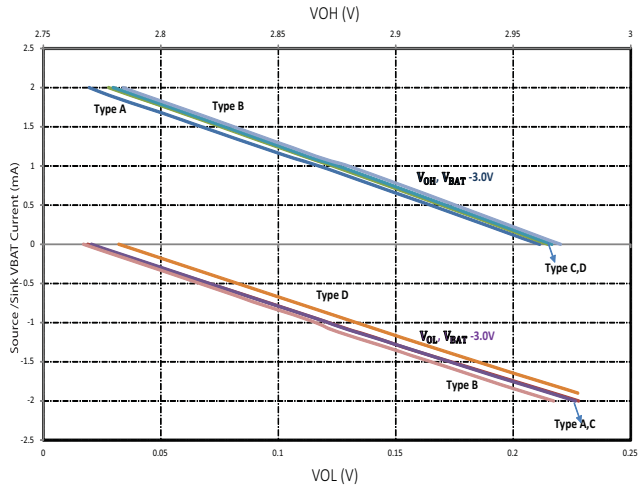


Figure 19. Output Single Drive Strength Characteristics (VBAT = 3.0 V)

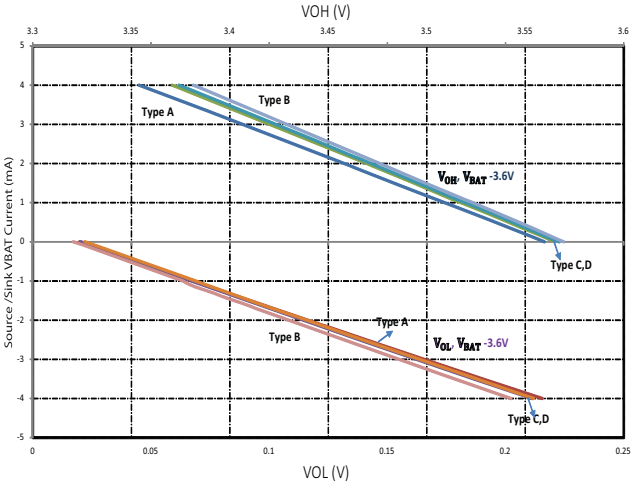


Figure 20. Output Double Drive Strength Characteristics (VBAT = 3.6 V)

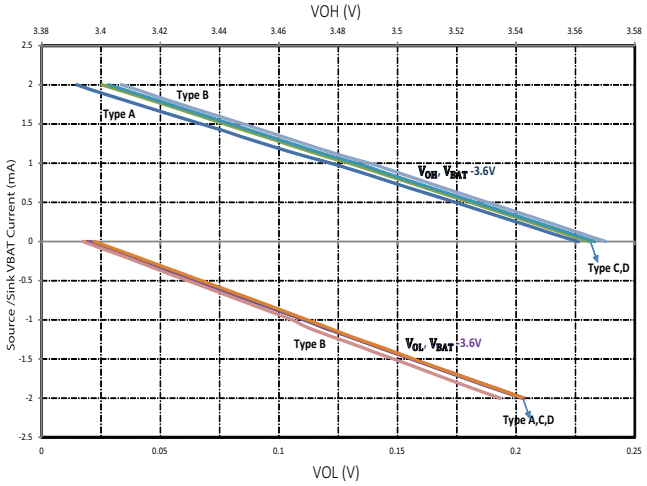


Figure 21. Output Single Drive Strength Characteristics (VBAT = 3.6 V)

ENVIRONMENTAL CONDITIONS

Table 23. Thermal Characteristics (64-Lead LFCSP)

Parameter	Typ	Unit
θ_{JA}	28.2	°C/W
θ_{JC}	5.4	°C/W

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first-order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:
T_A is ambient temperature (°C).
T_J is junction temperature (°C).
P_D is power dissipation (To calculate P_D, see the Power Supply Current section).

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heat sink is required.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

Figure 22 shows an overview of signal placement on the 64-Lead LFCSP_WQ.

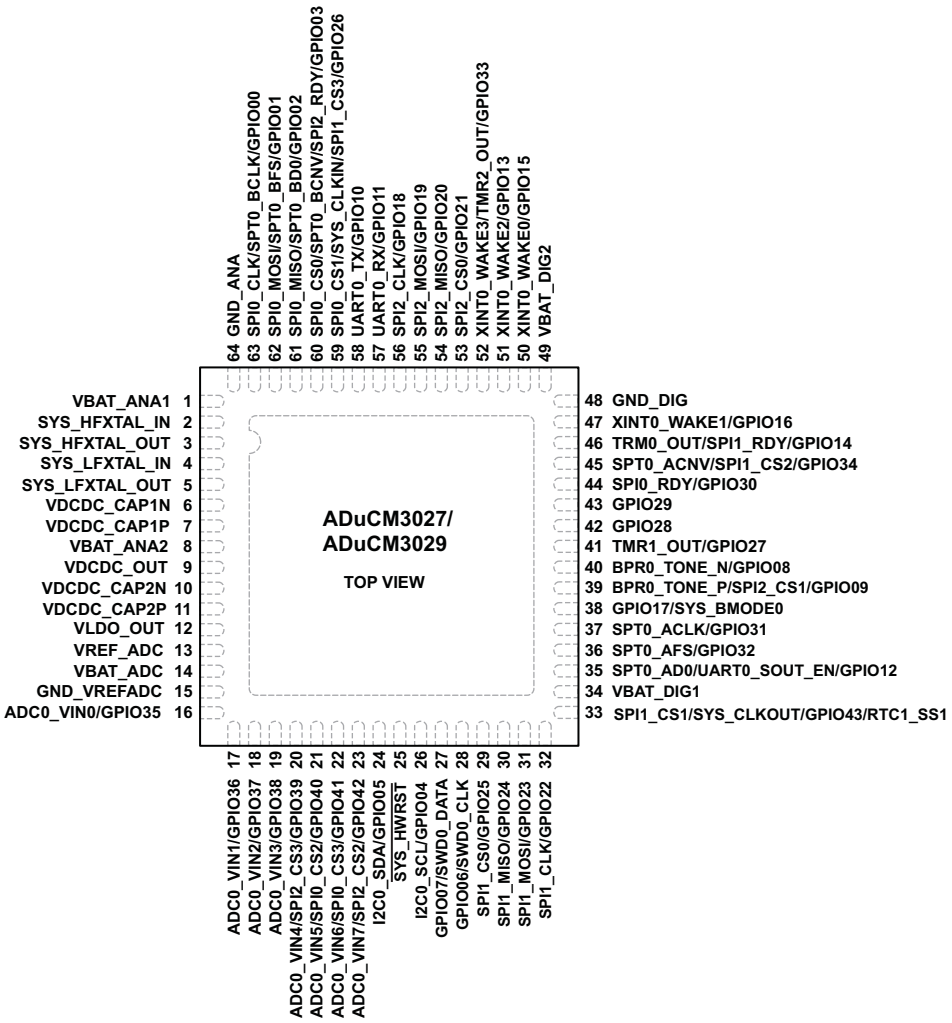


Figure 22. 64-Lead LFCSP Configuration

Figure 23 shows an overview of signal placement on the 54-Ball WLCSP.

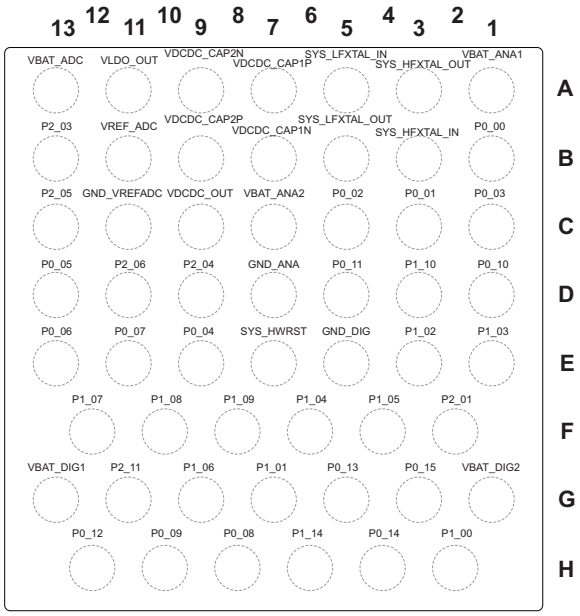


Figure 23. 54-Ball WLCSP Configuration

Table 24 lists the signal descriptions of the ADuCM3027/ADuCM3029 MCUs.

Table 24. Signal Functional Descriptions

GPIO Signal Name	Description
SPIn_CLK	SPI Clock. n = 0, 1, 2.
SPIn_MOSI	SPI Master Out Slave In. n = 0, 1, 2.
SPIn_MISO	SPI Master In Slave Out. n = 0, 1, 2.
SPIn_RDY	SPI Ready Signal. n = 0, 1, 2.
SPIn_CSm	SPI Chip Select Signal. n = 0, 1, 2 and m = 0, 1, 2, 3.
SPT0_ACLK	SPORT A Clock Signal.
SPT0_AFS	SPORT A Frame Sync.
SPT0_AD0	SPORT A Data Pin 0.
SPT0_ACNV	SPORT A Converter Signal for Interface with ADC.
SPT0_BCLK	SPORT B Clock Signal.
SPT0_BFS	SPORT B Frame Sync.
SPT0_BD0	SPORT B Data Pin 0.
SPT0_BCNV	SPORT B Converter Signal for Interface with ADC.
I2C0_SCL	I^2C Clock.
I2C0_SDA	I^2C Data.
SWD0_CLK	Serial Wire Debug Clock.
SWD0_DATA	Serial Wire Debug Data.
BPR0_TONE_N	Beeper Tone Negative Pin.
BPR0_TONE_P	Beeper Tone Positive Pin.
UART0_TX	UART Transmit Pin.
UART0_RX	UART Receive Pin.
UART0_SOUT_EN	UART Serial Data Out Pin.
XINT0_WAKEn	System Wake-Up Pin. Wake Up from Flexi/Hibernate/Shutdown Modes[1]. n = 0, 1, 2, 3.
TMRn_OUT	Timer Output Pin. n = 0, 1, 2.
SYS_BMODE0	Boot Mode Pin.
SYS_CLKIN	External Clock In Pin.
SYS_CLKOUT	External Clock Out Pin.
RTC1_SS1	RTC1 SensorStrobe Pin.
ADC0_VINn	ADC Voltage Input Pin. n = 0, 1, 2, 3, 4, 5, 6, 7.

[1] For shutdown, XINT0_WAKE3 is not capable of waking the device from shutdown mode.

Table 25. Pin Function Descriptions, 64-Lead LFCSP_WQ (Continued)

Pin No.	GPIO	Signal Name	Description	GPIO Pull
46	P0_14	TMR0_OUT/SPI1_RDY/GPIO14		PU
47	P1_00	XINT0_WAKE1/GPIO16		PU
48		GND_DIG	Digital Ground.	
49		VBAT_DIG2	Digital 3 V Supply.	
50	P0_15	XINT0_WAKE0/GPIO15		PU
51	P0_13	XINT0_WAKE2/GPIO13		PU
52	P2_01	XINT0_WAKE3/TMR2_OUT/GPIO33		PU
53	P1_05	SPI2_CS0/GPIO21		PU
54	P1_04	SPI2_MISO/GPIO20		PU
55	P1_03	SPI2_MOSI/GPIO19		PU
56	P1_02	SPI2_CLK/GPIO18		PU
57	P0_11	UART0_RX/GPIO11		PU
58	P0_10	UART0_TX/GPIO10		PU
59	P1_10	SPI0_CS1/SYS_CLKIN/SPI1_CS3/GPIO26		PU
60	P0_03	SPI0_CS0/SPT0_BCNV/SPI2_RDY/GPIO03		PU
61	P0_02	SPI0_MISO/SPT0_BD0/GPIO02		PU
62	P0_01	SPI0_MOSI/SPT0_BFS/GPIO01		PU
63	P0_00	SPI0_CLK/SPT0_BCLK/GPIO00		PU
64		GND_ANA	Analog Ground.	
Exposed Pad		GND	Ground.	

Table 26 lists the 54-Ball WLCSP package by ball number for the ADuCM3027/ADuCM3029 MCUs.

Table 26. Pin Function Descriptions, 54-Ball WLCSP

Ball No.	GPIO	Pin Label	Description	GPIO Pull
A01		VBAT_ANA1	Analog 3 V Supply.	
A03		SYS_HFXTAL_OUT	26 MHz High Frequency Crystal.	
A05		SYS_LFXTAL_IN	32 kHz Low Frequency Crystal.	
A07		VDCDC_CAP1P	Buck Fly Capacitor.	
A09		VDCDC_CAP2N	Buck Fly Capacitor.	
A11		VLDO_OUT	LDO Output Capacitor	
A13		VBAT_ADC	Analog 3 V Supply for ADC.	
B01	P0_00	SPI0_CLK/SPT0_BCLK/GPIO00		PU
B03		SYS_HFXTAL_IN	26 MHz High Frequency Crystal.	
B05		SYS_LFXTAL_OUT	32 kHz Low Frequency Crystal.	
B07		VDCDC_CAP1N	Buck Fly Capacitor.	
B09		VDCDC_CAP2P	Buck Fly Capacitor.	
B11		VREF_ADC	Analog Reference Voltage for ADC.	
B13	P2_03	ADC0_VIN0/GPIO35		PU
C01	P0_03	SPI0_CS0/SPT0_BCNV/SPI2_RDY/GPIO03		PU
C03	P0_01	SPI0_MOSI/SPT0_BFS/GPIO01		PU
C05	P0_02	SPI0_MISO/SPT0_BD0/GPIO02		PU
C07		VBAT_ANA2	Analog 3 V Supply.	
C09		VDCDC_OUT	Buck Output Capacitor.	
C11		GND_VREFADC	Reference Ground for ADC.	
C13	P2_05	ADC0_VIN2/GPIO37		PU
D01	P0_10	UART0_TX/GPIO10		PU
D03	P1_10	SPI0_CS1/SYS_CLKIN/SPI1_CS3/GPIO26		PU
D05	P0_11	UART0_RX/GPIO11		PU
D07		GND_ANA	Analog Ground.	
D09	P2_04	ADC0_VIN1/GPIO36		PU
D11	P2_06	ADC0_VIN3/GPIO38		PU
D13	P0_05	I2C0_SDA/GPIO05		PU
E01	P1_03	SPI2_MOSI/GPIO19		PU
E03	P1_02	SPI2_CLK/GPIO18		PU
E05		GND_DIG	Digital Ground.	
E07		$\overline{\text{SYS\_HWRST}}$	System Hardware Reset.	
E09	P0_04	I2C0_SCL/GPIO04		PU
E11	P0_07	GPIO07/SWD0_DATA		PU
E13	P0_06	GPIO06/SWD0_CLK		PD
F02	P2_01	XINT0_WAKE3/TMR2_OUT/GPIO33		PU
F04	P1_05	SPI2_CS0/GPIO21		PU
F06	P1_04	SPI2_MISO/GPIO20		PU
F08	P1_09	SPI1_CS0/GPIO25		PU
F10	P1_08	SPI1_MISO/GPIO24		PU
F12	P1_07	SPI1_MOSI/GPIO23		PU
G01		VBAT_DIG2	Digital 3 V Supply.	
G03	P0_15	XINT0_WAKE0/GPIO15		PU

OUTLINE DIMENSIONS

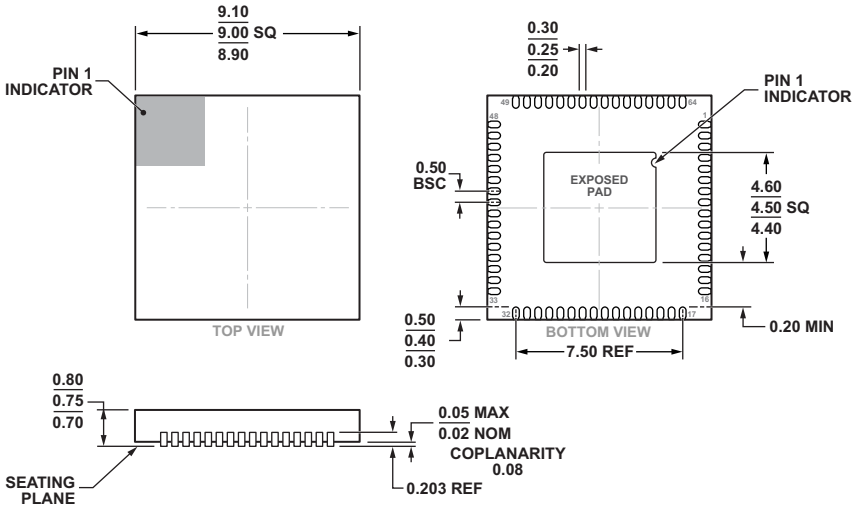


Figure 24. 64-Lead Frame Chip Scale Package [LFCSP]
9 mm x 9 mm Body and 0.75 mm Package Height
(CP-64-16)
Dimensions shown in mm
Note: Exposed pad must be grounded

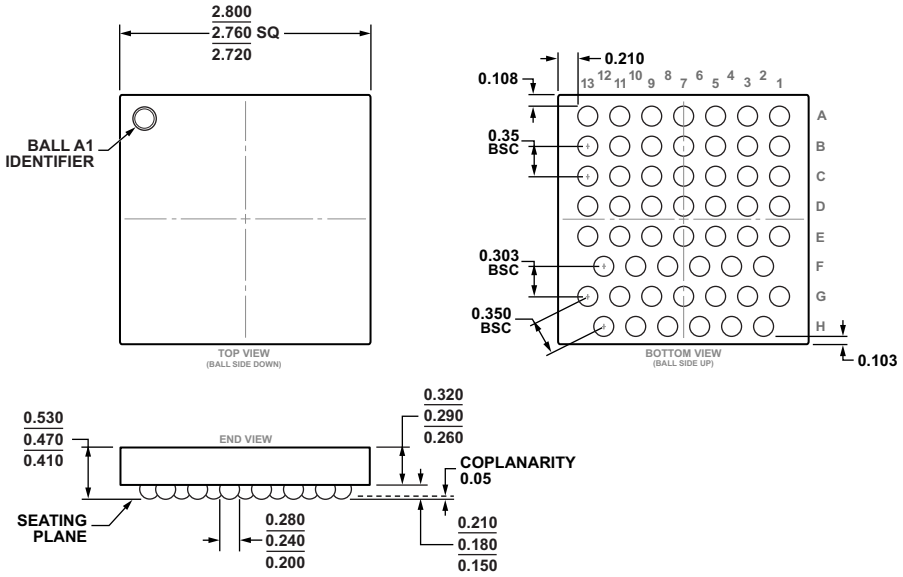


Figure 25. 54-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-54-1)
Dimensions shown in mm