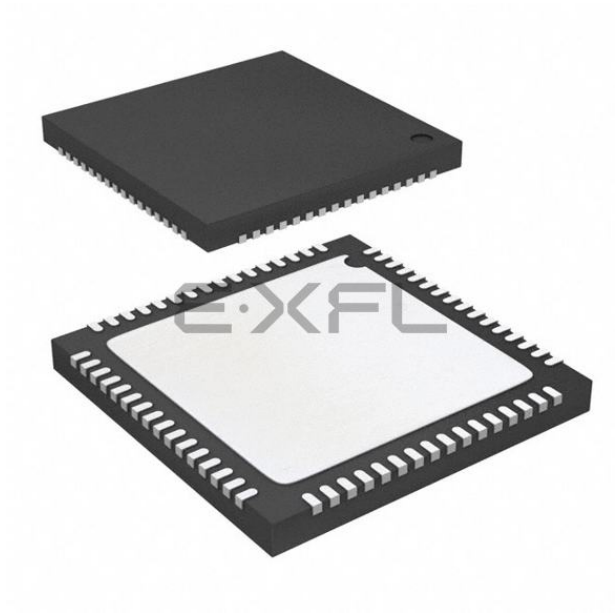

**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 26MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | DMA, POR, PWM, WDT |
| Number of I/O | 44 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 96K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.74V ~ 3.6V |
| Data Converters | A/D 8x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-WFQFN Exposed Pad, CSP |
| Supplier Device Package | 64-LFCSP-WQ (9x9) |
| Purchase URL | https://www.e-xfl.com/product-detail/analog-devices/aducm3029bcpz-rl |

# TABLE OF CONTENTS



## REVISION HISTORY

**3/2017—Revision 0: Initial Version**

- Configurable for ultralow power operation
  - Deep sleep mode, dynamic power management
  - Programmable clock generator unit

### *ARM Cortex-M3 Memory Subsystem*

The memory map of the ADuCM3027/ADuCM3029 is based on the Cortex-M3 model from ARM. By retaining the standardized memory mapping, it is easier to port applications across M3 platforms.

The ADuCM3027/ADuCM3029 application development is based on memory blocks across code/SRAM regions. Internal memory is available via internal SRAM and internal flash.

**Code Region**

Accesses in this region (0x0000 0000 to 0x0001 FC00 for the ADuCM3027 and 0x0000 0000 to 0x0003 FFFF for the ADuCM3029) are performed by the core and target the memory and cache resources.

**SRAM Region**

Accesses in this region (0x2000 0000 to 0x2004 7FFF) are performed by the ARM Cortex-M3 core. The SRAM region of the core can otherwise act as a data region for an application.

- **Internal SRAM Data Region.** This space can contain read/write data. Internal SRAM can be partitioned between code and data (SRAM region in M3 space) in 32 KB blocks. Access to this region occurs at core clock speed with no wait states.
  It also supports read/write access by the Cortex-M3 core and read/write DMA access by system devices. It supports exclusive memory accesses via the global exclusive access monitor within the Cortex-M3 platform.
- **System MMRs**. Various system memory mapped registers (MMRs) reside in this region.

**System Region**

Accesses in this region (0xE000 0000 to 0xF7FF FFFF) are performed by the ARM Cortex-M3 core and are handled within the Cortex-M3 platform.

- **CoreSight™ ROM.** The read only memory (ROM) table entries point to the debug components of the processor.
- **ARM APB Peripheral.** This space is defined by ARM and occupies the bottom 256 KB/128 KB of the system (SYS) region (0xE000 0000 to 0xE004 0000) depending on the device used. The space supports read/write access by the M3 core to the internal peripherals of the ARM core (NVIC, system control space (SCS), wake-up interrupt controller (WIC)) and CoreSight ROM. It is not accessible by system DMA.

## MEMORY ARCHITECTURE

The internal memory of the ADuCM3027/ADuCM3029 is shown in Figure 2. It incorporates up to 256 KB of embedded flash memory for program code and nonvolatile data storage, 32 KB of data SRAM, and 32 KB of SRAM (configured as instruction space or data space).

### *SRAM Region*

This memory space contains the application instructions and literal (constant) data that must be accessed in real-time. It supports read/write access by the ARM Cortex-M3 core and read/write DMA access by system peripherals. Byte, half-word, and word accesses are supported.

SRAM is divided into 32 KB data SRAM and 32 KB instruction SRAM. If instruction SRAM is not enabled, then the associated 32 KB can be mapped as data SRAM, resulting in 64 KB of data SRAM.

Parity bit error detection (optional) is available on all SRAM memories. Two parity bits are associated with each 32-bit word.

When the cache controller is enabled, 4 KB of the instruction SRAM is reserved as cache memory.

Users can select the SRAM configuration modes depending on the instruction SRAM and cache needed.

In hibernate mode, 8 KB to 32 KB of the SRAM can be retained in increments of 8 KB. 8 KB of data SRAM is always retained. Users can additionally retain

- 16 KB out of 32 KB of instruction SRAM
- 8 KB out of 32 KB of data SRAM

### *MMRs (Peripheral Control and Status)*

For the address space containing MMRs, refer to Figure 2. These registers provide control and status for on-chip peripherals of the ADuCM3027/ADuCM3029. For more information about the MMRs, refer to the ADuCM302x Ultra Low Power ARM Cortex-M3 MCU with Integrated Power Management Hardware Reference.

### *Flash Memory*

The ADuCM3027/ADuCM3029 MCUs include 128 KB to 256 KB of embedded flash memory, which is accessed using a flash controller. For memory available on each product, see Table 1. The flash controller is coupled with a cache controller. A prefetch mechanism is implemented in the flash controller to optimize code performance.

Flash writes are supported by a key hole mechanism via advanced peripheral bus (APB) writes to MMRs. The flash controller provides support for DMA-based key hole writes.

With respect to flash integrity, the devices support the following:

- A fixed user key required for running protected commands, including mass erase and page erase.
- An optional and user definable user failure analysis key (FAA key). Analog Devices personnel need this key while performing failure analysis.
- An optional and user definable write protection for user accessible memory.
- An optional 8-bit ECC. It is enabled by default. It is recommended not to disable ECC.

The key differences between RTC0 and RTC1 (FLEX_RTC) are shown in Table 3.

**Table 3. RTC Features**

| Features | RTC0 | RTC1 (FLEX_RTC) |
|---|---|---|
| Resolution of Time Base (Prescaling) | Counts time at 1 Hz in units of seconds. Operationally, always prescales to 1 Hz (for example, divide by 32,768) and always counts real time in units of seconds. | Can prescale the clock by any power of two from 0 to 15. It can count time in units of any of these 16 possible prescale settings. For example, the clock can be prescaled by 1, 2, 4, 8, …, 16384, or 32768. |
| Source Clock | LFXTAL. | Depending on the low frequency multiplexer (LFMUX) configuration, the RTC is clocked by the LFXTAL or the LFOSC. |
| Wake-Up Timer | Wake-up time is specified in units of seconds. | Supports alarm times down to a resolution of 30.7 µs, that is, where the time is specified down to a specific 32 kHz clock cycle. |
| Number of Alarms | One alarm only. Uses an absolute, nonrepeating alarm time, specified in units of 1 sec. | Two alarms. One absolute alarm time and one periodic alarm, repeating every 60 prescaled time units. |
| SensorStrobe Mechanism | Not available. | SensorStrobe is an alarm mechanism in the RTC that causes an output pulse to be sent via GPIOs to an external device to instruct the device to take a measurement or perform some action at a specific time. SensorStrobe events are scheduled at a specific target time relative to the real-time count of the RTC. SensorStrobe can be enabled in active, Flexi, and hibernate modes. |
| Input Capture | Not available. | Input capture takes a snapshot of the RTC when an external device signals an event via a transition on one of the GPIO inputs to the ADuCM3027/ ADuCM3029. Typically, an input-capture event is triggered by an autonomous measurement or action on such a device, which then signals to the ADuCM3027/ ADuCM3029 that the RTC must take a snapshot of time corresponding to the event. Taking the snapshot can wake up the ADuCM3027/ ADuCM3029 and cause an interrupt to the CPU. The CPU can subsequently obtain information from the RTC on the exact 32 kHz cycle on which the input capture event occurred. |

### *Hardware*

The ADuCM3029 EZ-KIT® is available to prototype sensor configurations with the ADuCM3027/ADuCM3029 MCUs.

### *Software*

The ADuCM3029 EZ-KIT includes a complete development and debug environment for the ADuCM3027/ADuCM3029 MCUs. The board support package (BSP) for the ADuCM3027/ADuCM3029 is provided for the IAR Embedded Workbench for ARM, Keil™, and CrossCore® embedded studio (CCES) environments.

The BSP also includes operating system (OS) aware drivers and example code for all the peripherals on the devices.

## ADDITIONAL INFORMATION

The following publications that describe the ADuCM3027/ADuCM3029 MCUs can be ordered from any Analog Devices sales office or accessed electronically on the Analog Devices website:

- ADuCM302x Ultra Low Power ARM Cortex-M3 MCU with Integrated Power Management Hardware Reference.
- ADuCM3027/ADuCM3029 Anomaly List

This data sheet describes the ARM Cortex-M3 core and memory architecture used on the ADuCM3027/ADuCM3029 MCUs, but does not provide detailed programming information for the ARM processor. For more information about programming the ARM processor, visit the ARM Infocenter web page.

The applicable documentation for programming the ARM Cortex-M3 processor include the following:

- *ARM Cortex-M3 Devices Generic User Guide*
- *ARM Cortex-M3 Technical Reference Manual*

## REFERENCE DESIGNS

The Circuits from the Lab® page provides the following:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

## SECURITY FEATURES DISCLAIMER

To our knowledge, the Security Features, when used in accordance with the data sheet and hardware reference manual specifications, provide a secure method of implementing code and data safeguards. However, Analog Devices does not guarantee that this technology provides absolute security. ACCORDINGLY, ANALOG DEVICES HEREBY DISCLAIMS ANY AND ALL EXPRESS AND IMPLIED WARRANTIES THAT THE SECURITY FEATURES CANNOT BE BREACHED, COMPROMISED, OR OTHERWISE CIRCUMVENTED AND IN NO EVENT SHALL ANALOG DEVICES BE LIABLE FOR ANY LOSS, DAMAGE, DESTRUCTION, OR RELEASE OF DATA, INFORMATION, PHYSICAL PROPERTY, OR INTELLECTUAL PROPERTY.

### *Power Supply Current*

Table 4, Table 5, and Table 6 describe power supply current for $V_{BAT}$.

**Table 4. Active Mode—Current Consumption When $V_{BAT}$ = 3.0 V**

| Conditions | Buck | Typ[1] | Max[2] | Unit |
|---|---|---|---|---|
| Code[3] executing from flash, cache enabled, peripheral clocks off, HCLK = 6.5 MHz | Enabled | 0.40 | | mA |
| Code[3] executing from flash, cache enabled, peripheral clocks off, HCLK = 26 MHz | Enabled | 0.98 | 1.29 | mA |
| | Disabled | 1.75 | 2.38 | mA |
| Code[3] executing from flash, cache disabled, peripheral clocks off, HCLK = 26 MHz | Enabled | 1.28 | 1.64 | mA |
| | Disabled | 2.34 | 3.0 | mA |
| Code[3] executing from SRAM, peripheral clocks off, HCLK = 26 MHz | Enabled | 0.95 | 1.36 | mA |
| | Disabled | 1.78 | 2.48 | mA |
| Code[3] executing from flash, cache enabled, peripheral clocks on, HCLK = 26 MHz, PCLK = 26 MHz | Enabled | 1.08 | 1.43 | mA |
| | Disabled | 1.99 | 2.67 | mA |
| Code[3] executing from flash, cache disabled, peripheral clocks on, HCLK = 26 MHz, PCLK = 26 MHz | Enabled | 1.37 | 1.78 | mA |
| | Disabled | 2.55 | 3.29 | mA |
| Code[3] executing from SRAM, peripheral clocks on, HCLK = 26 MHz, PCLK = 26 MHz | Enabled | 1.08 | 1.49 | mA |
| | Disabled | 2.03 | 2.74 | mA |

[1] $T_J$ = 25°C.
[2] $T_J$ = 85°C.
[3] The code being executed is a prime number generation in a continuous loop, with HFOSC as the system clock source.

**Table 5. Flexi™ Mode—Current Consumption When $V_{BAT}$ = 3.0 V**

| Conditions | Buck | Typ[1] | Max[2] | Unit |
|---|---|---|---|---|
| Peripheral clocks off | Enabled | 0.3 | 0.67 | mA |
| | Disabled | 0.52 | 1.11 | mA |
| Peripheral clocks on, PCLK = 26 MHz | Enabled | 0.39 | 0.80 | mA |
| | Disabled | 0.7 | 1.38 | mA |

[1] $T_J$ = 25°C.
[2] $T_J$ = 85°C.

**Table 6. Deep Sleep Modes[1]—Current Consumption When $V_{BAT}$ = 3.0 V**

| Mode | Conditions | −40°C Typ | +25°C Typ | +85°C Typ | +85°C Max | Unit |
|---|---|---|---|---|---|---|
| Hibernate | RTC1 and RTC0 disabled, 8 KB SRAM retained, LFXTAL off | 0.66 | 0.75 | 2.0 | 6.05 | µA |
| | RTC1 and RTC0 disabled, 16 KB SRAM retained, LFXTAL off | 0.67 | 0.77 | 2.4 | 6.4 | µA |
| | RTC1 and RTC0 disabled, 24 KB SRAM retained, LFXTAL off | 0.68 | 0.79 | 2.6 | 6.75 | µA |
| | RTC1 and RTC0 disabled, 32 KB SRAM retained, LFXTAL off | 0.69 | 0.81 | 3.0 | 7.1 | µA |
| | RTC1 enabled, 8 KB SRAM retained, LFOSC as source for RTC1 | 0.69 | 0.78 | 2.05 | 6.1 | µA |
| | RTC1 enabled, 8 KB SRAM retained, LFXTAL as source for RTC1 | 0.74 | 0.83 | 2.1 | 6.15 | µA |
| | RTC1 and RTC0 enabled, 8 KB SRAM retained, LFXTAL as source for RTC1 and RTC0 | 0.83 | 0.93 | 2.25 | 6.3 | µA |
| Shutdown | RTC0 enabled, LFXTAL as source for RTC0 | 290 | 310 | 490 | 1180 | nA |
| | RTC0 disabled | 40 | 56 | 260 | 950 | nA |

[1] Buck enable/disable selection does not affect power consumption.

## SYSTEM CLOCKS/TIMERS

Table 7 and Table 8 show the system clock specifications for the ADuCM3027/ADuCM3029 MCUs.

### *Platform External Crystal Oscillator*

**Table 7. Platform External Crystal Oscillator Specifications**

| Parameter | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|
| LOW FREQUENCY EXTERNAL CRYSTAL OSCILLATOR (LFXTAL) | | | | | |
| $C_{EXT1} = C_{EXT2}$ | 6 | | 10 | pF | External capacitor, $C_{EXT1} = C_{EXT2}$ (symmetrical load), for $C_L \leq 5$ pF (maximum) and ESR = 30 kΩ (maximum). $C_{EXT1}$, $C_{EXT2}$ must be selected considering the printed circuit board (PCB) trace capacitance due to routing. |
| Frequency | | 32,768 | | Hz | |
| HIGH FREQUENCY EXTERNAL CRYSTAL OSCILLATOR (HFXTAL) | | | | | |
| $C_{EXT1} = C_{EXT2}$ | | | 20 | pF | External capacitor, $C_{EXT1} = C_{EXT2}$ (symmetrical load), for $C_L$ = 10 pF (maximum) and ESR = 50 Ω (maximum). $C_{EXT1}$, $C_{EXT2}$ must be selected considering the PCB trace capacitance due to routing. |
| Frequency | | 26 | | MHz | |

### *On-Chip RC Oscillator*

**Table 8. On-Chip RC Oscillator Specifications**

| Parameter | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|
| HIGH FREQUENCY RC OSCILLATOR (HFOSC) | | | | | |
| Frequency | 25.09 | 26 | 26.728 | MHz | |
| LOW FREQUENCY RC OSCILLATOR (LFOSC) | | | | | |
| Frequency | 30,800 | 32,768 | 34,407 | Hz | |

## ABSOLUTE MAXIMUM RATINGS

Stresses at or above those listed in Table 11 may cause permanent damage to the product. This is a stress rating only. The functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

**Table 11. Absolute Maximum Ratings**

| Parameter | Rating | Unit |
|---|---|---|
| SUPPLY | | |
| VBAT_ANA1 | −0.3 to +3.6 | V |
| VBAT_ANA2 | | |
| VBAT_ADC | | |
| VBAT_DIG1 | | |
| VBAT_DIG2 | | |
| VREF_ADC | | |
| ANALOG | | |
| VDCDC_CAP1N | −0.3 to +3.6 | V |
| VDCDC_AP1P | | |
| VDCDC_OUT | | |
| VDCDC_CAP2N | | |
| VDCDC_CAP2P | | |
| VLDO_OUT | −0.3 to +1.32 | V |
| SYS_HFXTAL_IN | | |
| SYS_HFXTAL_OUT | | |
| SYS_LFXTAL_IN | | |
| SYS_LFXTAL_OUT | | |
| DIGITAL INPUT/OUTPUT | | |
| P0.X | −0.3 to +3.6 | V |
| P1.X | | |
| P2.X | | |
| $\overline{\text{SYS\_HWRST}}$ | | |

## ESD SENSITIVITY

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PACKAGE INFORMATION

Figure 4 and Table 12 provide details about package branding. For a complete listing of product availability, see the Ordering Guide section.


*Figure 4. Product Information on Package*[1]

[1] Exact brand may differ, depending on package type.

**Table 12. Package Brand Information**

| Brand Key | Field Description |
|---|---|
| ADuCM3027/ADuCM3029 | Product model |
| t | Temperature range |
| pp | Package type |
| Z | RoHS compliant designation |
| ccc | See the Ordering Guide section |
| vvvvvv.x | Assembly lot code |
| n.n | Silicon revision |
| yyww | Date code |

**Table 16. Serial Ports—Internal Clock**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| TIMING REQUIREMENTS | | | | |
| $t_{SDRI}$ | Receive Data Setup Before SPT_CLK[1] | 25 | | ns |
| $t_{HDRI}$ | Receive Data Hold After SPT_CLK[1] | 0 | | ns |
| SWITCHING CHARACTERISTICS | | | | |
| $t_{DFSI}$ | Frame Sync Delay After SPT_CLK (Internally Generated Frame Sync in Transmit or Receive Mode)[2] | | 20 | ns |
| $t_{HOFSI}$ | Frame Sync Hold After SPT_CLK (Internally Generated Frame Sync in Transmit or Receive Mode)[2] | –8 | | ns |
| $t_{DDTI}$ | Transmit Data Delay After SPT_CLK[2] | | 20 | ns |
| $t_{HDTI}$ | Transmit Data Hold After SPT_CLK[2] | –7 | | ns |
| $t_{SCLKIW}$ | SPT_CLK Width | $t_{PCLK}$ – 1.5 | | ns |
| $t_{SPTCLK}$ | SPT_CLK Period | 2 × $t_{PCLK}$ – 1 | | ns |

[1] This specification is referenced to the sample edge.
[2] This specification is referenced to the drive edge.

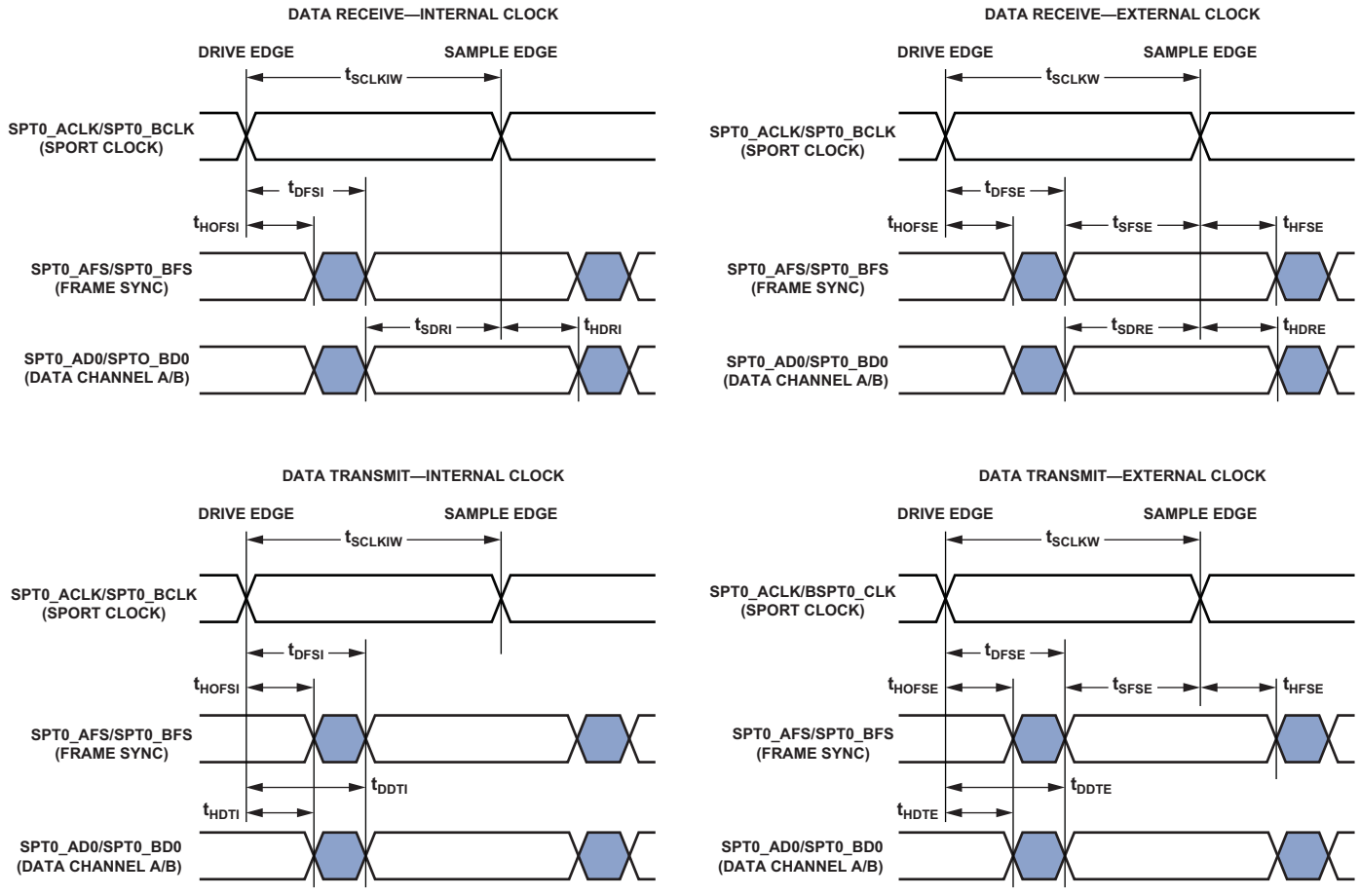


*Figure 6. Serial Ports*

**Table 17. Serial Ports—Enable and Three-State**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| SWITCHING CHARACTERISTICS | | | | |
| $t_{DDTIN}$ | Data Enable From Internal Transmit SPT_CLK[1] | 5 | | ns |
| $t_{DDTTI}$ | Data Disable From Internal Transmit SPT_CLK[1] | | 160 | ns |

[1] This specification is referenced to the drive edge.

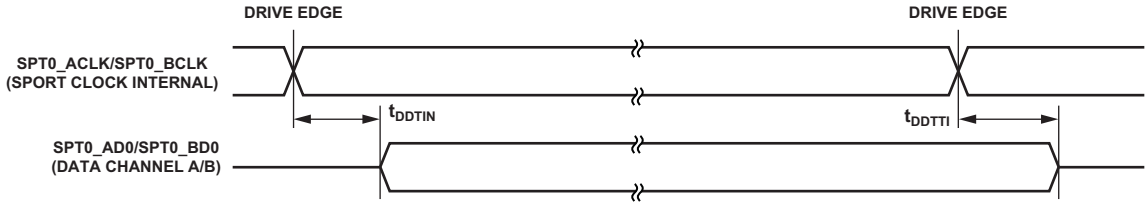


*Figure 7. Serial Ports—Enable and Three-State*

### *SPI Timing*

Table 18, Figure 8, and Figure 9 (for master mode) and Table 19, Figure 10, and Figure 11 (for slave mode) describe SPI timing specifications. High speed SPI (SPIH) can be used for high data rate peripherals.

**Table 18. SPI Master Mode Timing[1]**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| TIMING REQUIREMENTS | | | | |
| $t_{CS}$ | $\overline{CS}$ to SCLK Edge | $0.5 \times t_{PCLK} - 3$ | | ns |
| $t_{SL}$ | SCLK Low Pulse Width | $t_{PCLK} - 3.5$ | | ns |
| $t_{SH}$ | SCLK High Pulse Width | $t_{PCLK} - 3.5$ | | ns |
| $t_{DSU}$ | Data Input Setup Time Before SCLK Edge | 5 | | ns |
| $t_{DHD}$ | Data Input Hold Time After SCLK Edge | 20 | | ns |
| SWITCHING CHARACTERISTICS | | | | |
| $t_{DAV}$ | Data Output Valid After SCLK Edge | | 25 | ns |
| $t_{DOSU}$ | Data Output Setup Before SCLK Edge | $t_{PCLK} - 2.2$ | | ns |
| $t_{SFS}$ | $\overline{CS}$ High After SCLK Edge | $0.5 \times t_{PCLK} - 3$ | | ns |

[1] This specification is characterized with respect to double drive strength.

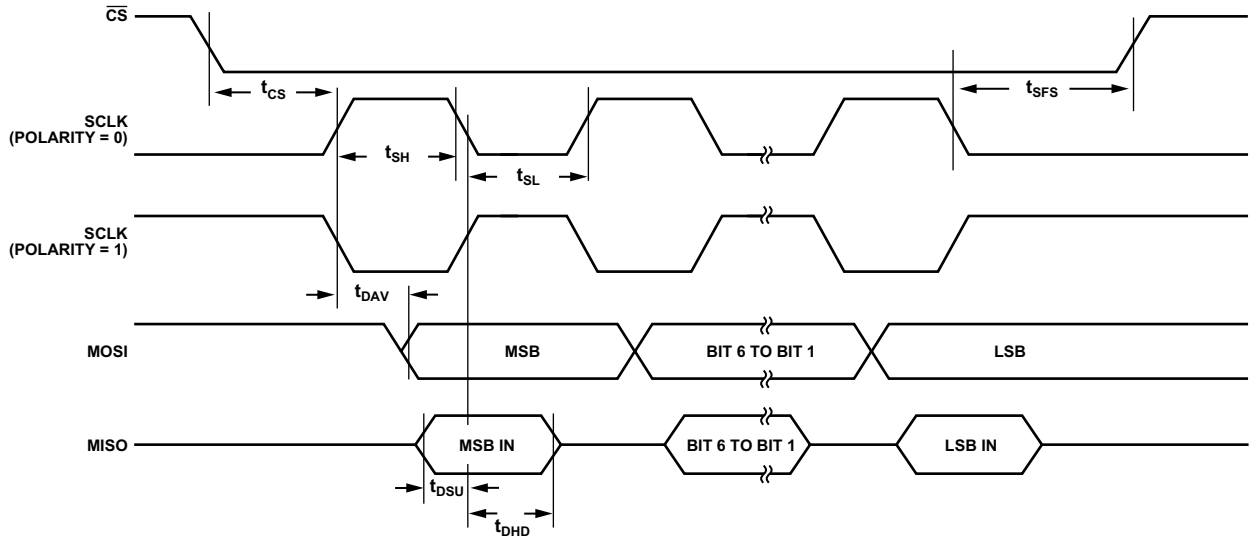


*Figure 8. SPI Master Mode Timing (Phase Mode = 1)*

### General-Purpose Port Timing

Table 20 and Figure 12 describe general-purpose port timing.

**Table 20. General-Purpose Port Timing**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| TIMING REQUIREMENTS | | | | |
| $t_{WFI}$ | General-Purpose Port Pin Input Pulse Width | $4 \times t_{PCLK}$ | | ns |

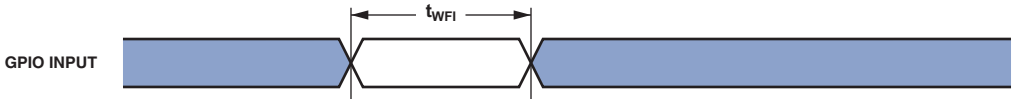


*Figure 12. General-Purpose Port Timing*

### Timer PWM_OUT Cycle Timing

Table 21 and Figure 13 describe timer PWM_OUT cycle timing.

**Table 21. Timer PWM_OUT Cycle Timing**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| SWITCHING CHARACTERISTICS | | | | |
| $t_{PWMO}$ | Timer Pulse Width Output | $4 \times t_{PCLK} - 6$ | $256 \times (2^{16} - 1)$ | ns |

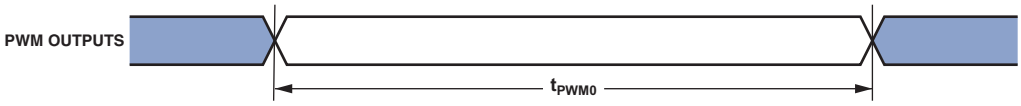


*Figure 13. Timer PWM_OUT Cycle Timing*

Figure 16 through Figure 21 show the typical current voltage characteristics for the output drivers of the MCU.

The curves represent the current drive capability of the output drivers as a function of output voltage.

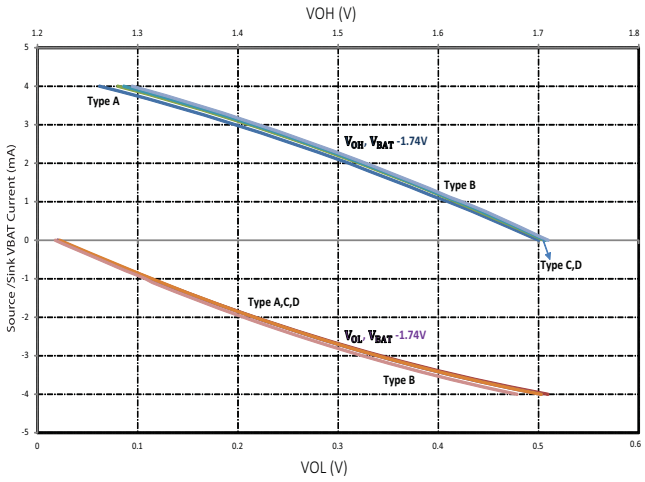


*Figure 16. Output Double Drive Strength Characteristics (VBAT = 1.74 V)*

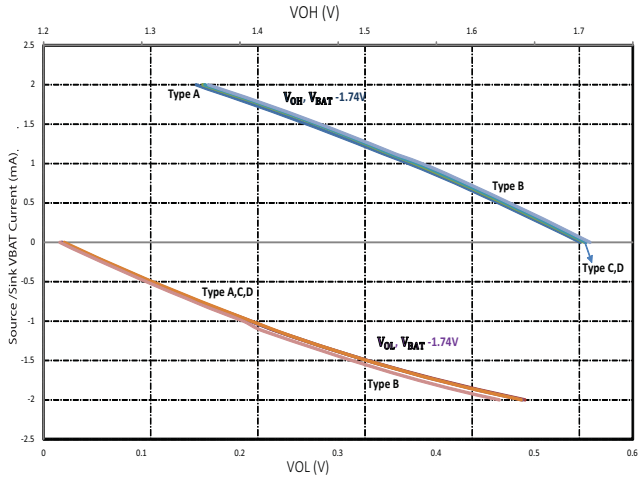


*Figure 17. Output Single Drive Strength Characteristics (VBAT = 1.74 V)*

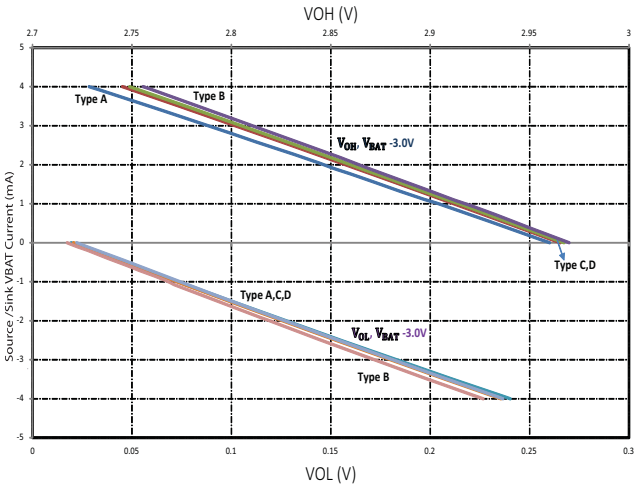


*Figure 18. Output Double Drive Strength Characteristics (VBAT = 3.0 V)*

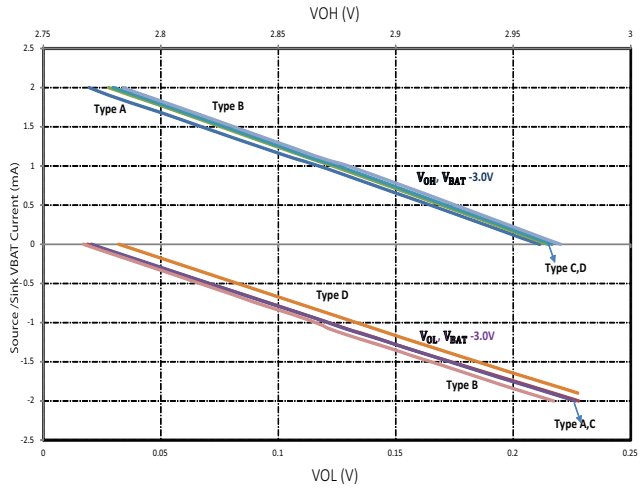


*Figure 19. Output Single Drive Strength Characteristics (VBAT = 3.0 V)*

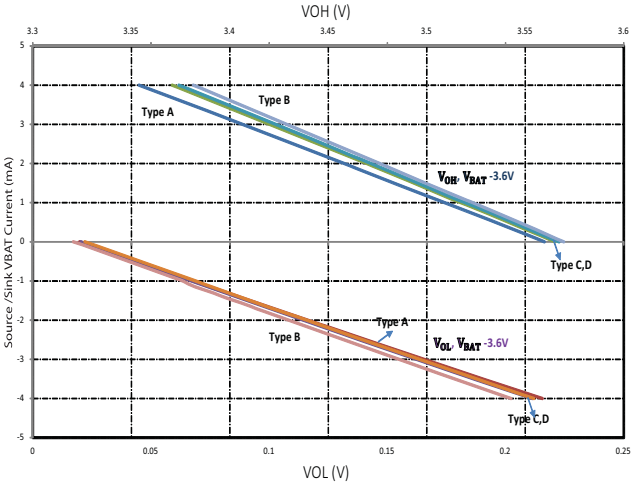


*Figure 20. Output Double Drive Strength Characteristics (VBAT = 3.6 V)*

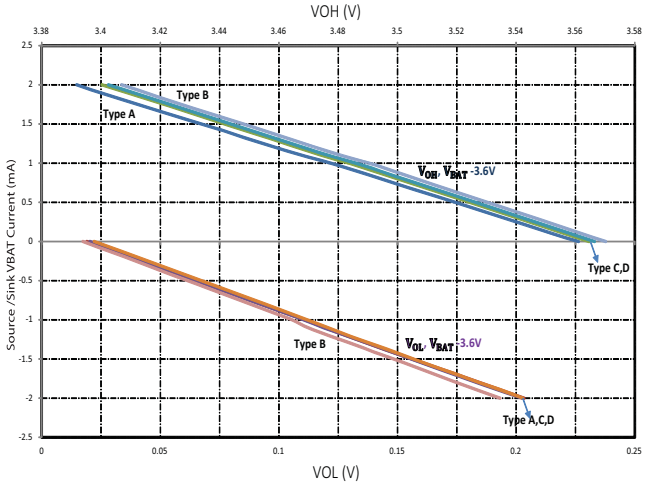


*Figure 21. Output Single Drive Strength Characteristics (VBAT = 3.6 V)*

## ENVIRONMENTAL CONDITIONS

**Table 23. Thermal Characteristics (64-Lead LFCSP)**

| Parameter | Typ | Unit |
|---|---|---|
| $\theta_{JA}$ | 28.2 | °C/W |
| $\theta_{JC}$ | 5.4 | °C/W |

Values of $\theta_{JA}$ are provided for package comparison and PCB design considerations. $\theta_{JA}$ can be used for a first-order approximation of $T_J$ by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:
$T_A$ is ambient temperature (°C).
$T_J$ is junction temperature (°C).
$P_D$ is power dissipation (To calculate $P_D$, see the Power Supply Current section).

Values of $\theta_{JC}$ are provided for package comparison and PCB design considerations when an external heat sink is required.

# PIN CONFIGURATION AND FUNCTION DESCRIPTION

Figure 22 shows an overview of signal placement on the 64-Lead LFCSP_WQ.

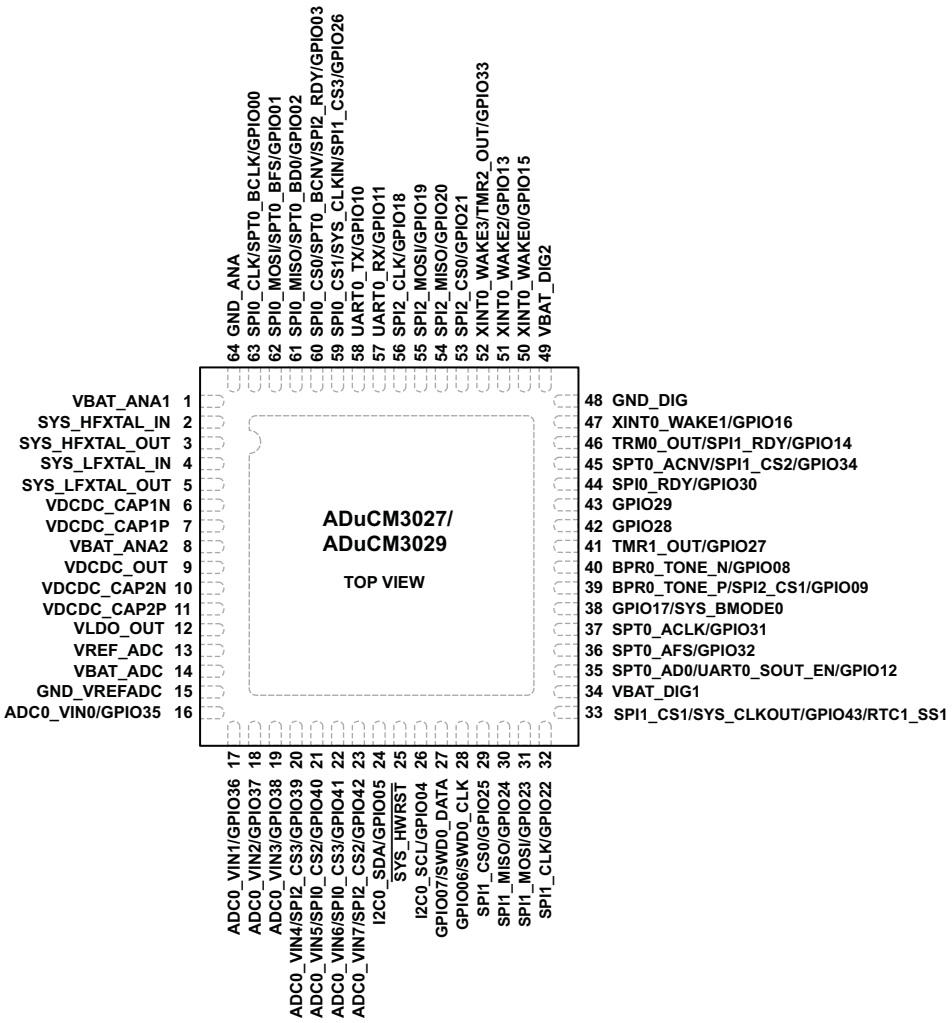


*Figure 22. 64-Lead LFCSP Configuration*

Table 24 lists the signal descriptions of the ADuCM3027/ADuCM3029 MCUs.

**Table 24. Signal Functional Descriptions**

| GPIO Signal Name | Description |
|---|---|
| SPIn_CLK | SPI Clock. n = 0, 1, 2. |
| SPIn_MOSI | SPI Master Out Slave In. n = 0, 1, 2. |
| SPIn_MISO | SPI Master In Slave Out. n = 0, 1, 2. |
| SPIn_RDY | SPI Ready Signal. n = 0, 1, 2. |
| SPIn_CSm | SPI Chip Select Signal. n = 0, 1, 2 and m = 0, 1, 2, 3. |
| SPT0_ACLK | SPORT A Clock Signal. |
| SPT0_AFS | SPORT A Frame Sync. |
| SPT0_AD0 | SPORT A Data Pin 0. |
| SPT0_ACNV | SPORT A Converter Signal for Interface with ADC. |
| SPT0_BCLK | SPORT B Clock Signal. |
| SPT0_BFS | SPORT B Frame Sync. |
| SPT0_BD0 | SPORT B Data Pin 0. |
| SPT0_BCNV | SPORT B Converter Signal for Interface with ADC. |
| I2C0_SCL | $I^2C$ Clock. |
| I2C0_SDA | $I^2C$ Data. |
| SWD0_CLK | Serial Wire Debug Clock. |
| SWD0_DATA | Serial Wire Debug Data. |
| BPR0_TONE_N | Beeper Tone Negative Pin. |
| BPR0_TONE_P | Beeper Tone Positive Pin. |
| UART0_TX | UART Transmit Pin. |
| UART0_RX | UART Receive Pin. |
| UART0_SOUT_EN | UART Serial Data Out Pin. |
| XINT0_WAKEn | System Wake-Up Pin. Wake Up from Flexi/Hibernate/Shutdown Modes[1]. n = 0, 1, 2, 3. |
| TMRn_OUT | Timer Output Pin. n = 0, 1, 2. |
| SYS_BMODE0 | Boot Mode Pin. |
| SYS_CLKIN | External Clock In Pin. |
| SYS_CLKOUT | External Clock Out Pin. |
| RTC1_SS1 | RTC1 SensorStrobe Pin. |
| ADC0_VINn | ADC Voltage Input Pin. n = 0, 1, 2, 3, 4, 5, 6, 7. |

[1] For shutdown, XINT0_WAKE3 is not capable of waking the device from shutdown mode.

Table 25 lists the 64-Lead LFCSP_WQ package by pin number for the ADuCM3027/ADuCM3029 MCUs.

**Table 25. Pin Function Descriptions, 64-Lead LFCSP_WQ**

| Pin No. | GPIO | Signal Name | Description | GPIO Pull |
|---|---|---|---|---|
| 1 | | VBAT_ANA1 | Analog 3 V Supply. | |
| 2 | | SYS_HFXTAL_IN | 26 MHz High Frequency Crystal. | |
| 3 | | SYS_HFXTAL_OUT | 26 MHz High Frequency Crystal. | |
| 4 | | SYS_LFXTAL_IN | 32 kHz Low Frequency Crystal. | |
| 5 | | SYS_LFXTAL_OUT | 32 kHz Low Frequency Crystal. | |
| 6 | | VDCDC_CAP1N | Buck Fly Capacitor. | |
| 7 | | VDCDC_CAP1P | Buck Fly Capacitor. | |
| 8 | | VBAT_ANA2 | Analog 3 V Supply. | |
| 9 | | VDCDC_OUT | Buck Output Capacitor. | |
| 10 | | VDCDC_CAP2N | Buck Fly Capacitor. | |
| 11 | | VDCDC_CAP2P | Buck Fly Capacitor. | |
| 12 | | VLDO_OUT | LDO Output Capacitor. | |
| 13 | | VREF_ADC | Analog Reference Voltage for ADC. | |
| 14 | | VBAT_ADC | Analog 3 V Supply for ADC. | |
| 15 | | GND_VREFADC | Reference Ground for ADC. | |
| 16 | P2_03 | ADC0_VIN0/GPIO35 | | PU |
| 17 | P2_04 | ADC0_VIN1/GPIO36 | | PU |
| 18 | P2_05 | ADC0_VIN2/GPIO37 | | PU |
| 19 | P2_06 | ADC0_VIN3/GPIO38 | | PU |
| 20 | P2_07 | ADC0_VIN4/SPI2_CS3/GPIO39 | | PU |
| 21 | P2_08 | ADC0_VIN5/SPI0_CS2/GPIO40 | | PU |
| 22 | P2_09 | ADC0_VIN6/SPI0_CS3/GPIO41 | | PU |
| 23 | P2_10 | ADC0_VIN7/SPI2_CS2/GPIO42 | | PU |
| 24 | P0_05 | I2C0_SDA/GPIO05 | | PU |
| 25 | | $\overline{\text{SYS\_HWRST}}$ | System Hardware Reset. | |
| 26 | P0_04 | I2C0_SCL/GPIO04 | | PU |
| 27 | P0_07 | GPIO07/SWD0_DATA | | PU |
| 28 | P0_06 | GPIO06/SWD0_CLK | | PD |
| 29 | P1_09 | SPI1_CS0/GPIO25 | | PU |
| 30 | P1_08 | SPI1_MISO/GPIO24 | | PU |
| 31 | P1_07 | SPI1_MOSI/GPIO23 | | PU |
| 32 | P1_06 | SPI1_CLK/GPIO22 | | PU |
| 33 | P2_11 | SPI1_CS1/SYS_CLKOUT/GPIO43/RTC1_SS1 | | PU |
| 34 | | VBAT_DIG1 | Digital 3 V Supply. | |
| 35 | P0_12 | SPT0_AD0/GPIO12 | | PU |
| 36 | P2_00 | SPT0_AFS/GPIO32 | | PU |
| 37 | P1_15 | SPT0_ACLK/GPIO31 | | PU |
| 38 | P1_01 | GPIO17/SYS_BMODE0 | | PU |
| 39 | P0_09 | BPR0_TONE_P/SPI2_CS1/GPIO09 | | PU |
| 40 | P0_08 | BPR0_TONE_N/GPIO08 | | PU |
| 41 | P1_11 | TMR1_OUT/GPIO27 | | PU |
| 42 | P1_12 | GPIO28 | | PU |
| 43 | P1_13 | GPIO29 | | PU |
| 44 | P1_14 | SPI0_RDY/GPIO30 | | PU |
| 45 | P2_02 | SPT0_ACNV/SPI1_CS2/GPIO34 | | PU |

**Table 26. Pin Function Descriptions, 54-Ball WLCSP (Continued)**

| Ball No. | GPIO | Pin Label | Description | GPIO Pull |
|---|---|---|---|---|
| G05 | P0_13 | XINT0_WAKE2/GPIO13 | | PU |
| G07 | P1_01 | GPIO17/SYS_BMODE0 | | PU |
| G09 | P1_06 | SPI1_CLK/GPIO22 | | PU |
| G11 | P2_11 | SPI1_CS1/SYS_CLKOUT/GPIO43/RTC1_SS1 | | PU |
| G13 | | VBAT_DIG1 | Digital 3 V Supply. | |
| H02 | P1_00 | XINT0_WAKE1/GPIO16 | | PU |
| H04 | P0_14 | TMR0_OUT/SPI1_RDY/GPIO14 | | PU |
| H06 | P1_14 | SPI0_RDY/GPIO30 | | PU |
| H08 | P0_08 | BPR0_TONE_N/GPIO08 | | PU |
| H10 | P0_09 | BPR0_TONE_P/SPI2_CS1/GPIO09 | | PU |
| H12 | P0_12 | SPT0_AD0/GPIO12/UART0_SOUT_EN | | PU |

# OUTLINE DIMENSIONS

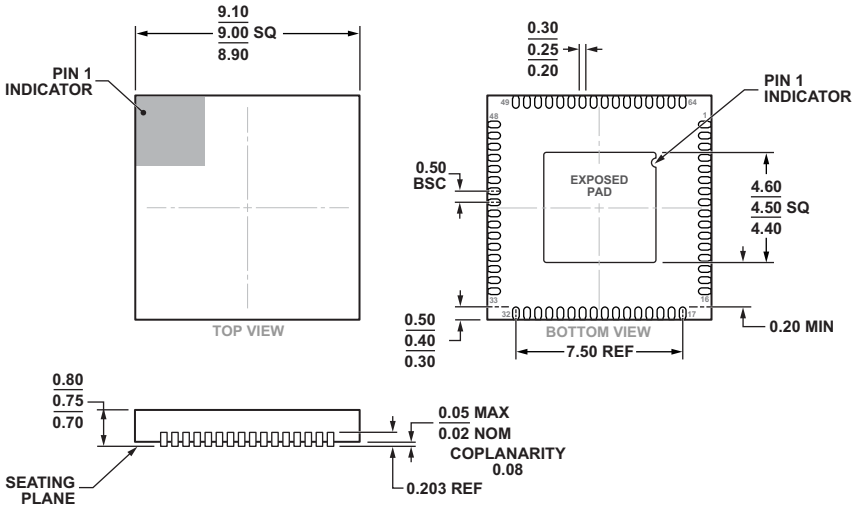


*Figure 24. 64-Lead Frame Chip Scale Package [LFCSP]*
*9 mm x 9 mm Body and 0.75 mm Package Height*
*(CP-64-16)*
*Dimensions shown in mm*
*Note: Exposed pad must be grounded*

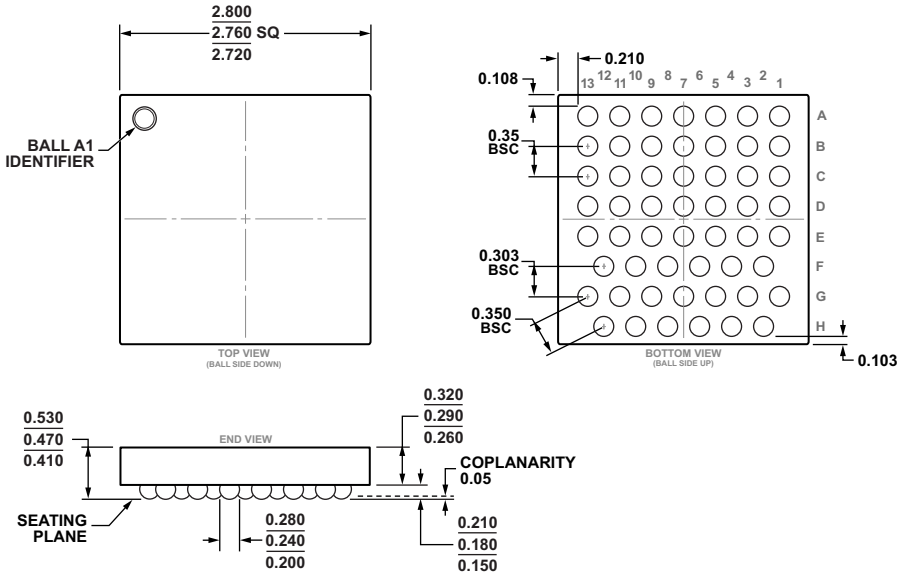


*Figure 25. 54-Ball Wafer Level Chip Scale Package [WLCSP]*
*(CB-54-1)*
*Dimensions shown in mm*

## ORDERING GUIDE

| Model[1] | Description | Temperature[2, 3] | Package Description | Package Option |
|---|---|---|---|---|
| ADUCM3027BCBZ-RL | ULP ARM Cortex-M3 with 128 KB Embedded Flash | −40°C to +85°C | 54-Ball WLCSP, 13″ Reel | CB-54-1 |
| ADUCM3027BCBZ-R7 | ULP ARM Cortex-M3 with 128 KB Embedded Flash | −40°C to +85°C | 54-Ball WLCSP, 7″ Reel | CB-54-1 |
| ADUCM3027BCPZ | ULP ARM Cortex-M3 with 128 KB Embedded Flash | −40°C to +85°C | 64-Lead LFCSP | CP-64-16 |
| ADUCM3027BCPZ-RL | ULP ARM Cortex-M3 with 128 KB Embedded Flash | −40°C to +85°C | 64-Lead LFCSP, 13″ Reel | CP-64-16 |
| ADUCM3027BCPZ-R7 | ULP ARM Cortex-M3 with 128 KB Embedded Flash | −40°C to +85°C | 64-Lead LFCSP, 7″ Reel | CP-64-16 |
| ADUCM3029BCBZ-RL | ULP ARM Cortex-M3 with 256 KB Embedded Flash | −40°C to +85°C | 54-Ball WLCSP, 13″ Reel | CB-54-1 |
| ADUCM3029BCBZ-R7 | ULP ARM Cortex-M3 with 256 KB Embedded Flash | −40°C to +85°C | 54-Ball WLCSP, 7″ Reel | CB-54-1 |
| ADUCM3029BCPZ | ULP ARM Cortex-M3 with 256 KB Embedded Flash | −40°C to +85°C | 64-Lead LFCSP | CP-64-16 |
| ADUCM3029BCPZ-RL | ULP ARM Cortex-M3 with 256 KB Embedded Flash | −40°C to +85°C | 64-Lead LFCSP, 13″ Reel | CP-64-16 |
| ADUCM3029BCPZ-R7 | ULP ARM Cortex-M3 with 256 KB Embedded Flash | −40°C to +85°C | 64-Lead LFCSP, 7″ Reel | CP-64-16 |
| ADZS-UCM3029EZLITE | ADuCM3029 Evaluation Kit | −40°C to +85°C | 64-Lead LFCSP | CP-64-16 |

[1] Z = RoHS Compliant Part.
[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. See the Absolute Maximum Ratings section for $T_J$ (junction temperature) specification which is the only temperature specification.
[3] These are preproduction devices. See ENG-Grade agreement for details.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).


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