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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | - |
| Core Size | - |
| Speed | - |
| Connectivity | - |
| Peripherals | - |
| Number of I/O | - |
| Program Memory Size | - |
| Program Memory Type | - |
| EEPROM Size | - |
| RAM Size | - |
| Voltage - Supply (Vcc/Vdd) | - |
| Data Converters | - |
| Oscillator Type | - |
| Operating Temperature | - |
| Mounting Type | - |
| Package / Case | - |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/analog-devices/aducm3029bcpz |

# GENERAL DESCRIPTION

The ADuCM3027/ADuCM3029 microcontroller units (MCUs) are ultra low power microcontroller systems with integrated power management for processing, control, and connectivity. The MCU system is based on the ARM Cortex-M3 processor, a collection of digital peripherals, embedded SRAM and flash memory, and an analog subsystem which provides clocking, reset, and power management capability in addition to an analog-to-digital converter (ADC) subsystem. For a feature comparison across the ADuCM3027/ADuCM3029 product offerings, see Table 1.

**Table 1. Product Flash Memory Options**

| Device | Embedded Flash Memory Size |
|---|---|
| ADuCM3029 | 256 KB |
| ADuCM3027 | 128 KB |

System features that are common across the ADuCM3027/ADuCM3029 MCUs include the following:

- Up to 26 MHz ARM Cortex-M3 processor
- Up to 256 KB of embedded flash memory with error correction code (ECC)
- Optional 4 KB cache for lower active power
- 64 KB system SRAM with parity
- Power management unit (PMU)
- Multilayer advanced microcontroller bus architecture (AMBA) bus matrix
- Central direct memory access (DMA) controller
- Beeper interface
- Serial port (SPORT), serial peripheral interface (SPI), inter-integrated circuit ($I^2C$), and universal asynchronous receiver/transmitter (UART) peripheral interfaces
- Cryptographic hardware support with advanced encryption standard (AES) and secure hash algorithm (SHA) -256
- Real-time clock (RTC)
- General-purpose and watchdog timers
- Programmable general-purpose input/output (GPIO) pins
- Hardware cyclic redundancy check (CRC) calculator with programmable generator polynomial
- Power-on reset (POR) and power supply monitor (PSM)
- 12-bit successive approximation register (SAR) ADC
- True random number generator (TRNG)

To support low dynamic and hibernate power management, the ADuCM3027/ADuCM3029 MCUs provide a collection of power modes and features, such as dynamic and software controlled clock gating and power gating.

For full details on the ADuCM3027/ADuCM3029 MCUs, refer to the ADuCM302x Ultra Low Power ARM Cortex-M3 MCU with Integrated Power Management Hardware Reference.

## HIGHLIGHTS

The following are the key features of the ADuCM3027/ADuCM3029 MCUs**:**

- Industry leading ultralow power consumption.
- Robust operation.
  - Full voltage monitoring in deep sleep modes.
  - ECC support on flash.
  - Parity error detection on SRAM memory.
- Leading edge security.
  - Fast encryption provides read protection to customer algorithms.
  - Write protection prevents device reprogramming by unauthorized code.
- Failure detection of 32 kHz LFXTAL via interrupt.
- SensorStrobe for precise time synchronized sampling of external sensors.
  - Works in hibernate mode, resulting in drastic current reduction in system solutions. Current consumption reduces by 10 times when using, for example, the ADXL363 accelerometer.
  - Software intervention is not required after setup.
  - No pulse drift due to software execution.

## ARM CORTEX-M3 PROCESSOR

The ARM Cortex-M3 core is a 32-bit reduced instruction set computer (RISC). The length of the data can be 8 bits, 16 bits, or 32 bits. The length of the instruction word is 16 bits or 32 bits.

The processor has the following features:

- Cortex-M3 architecture
  - Thumb-2 instruction set architecture (ISA) technology
  - Three-stage pipeline with branch speculation
  - Low latency interrupt processing with tail chaining
  - Single-cycle multiply
  - Hardware divide instructions
  - Nested vectored interrupt controller (NVIC) (64 interrupts and 8 priorities)
  - Two hardware breakpoints and one watchpoint (unlimited software breakpoints using Segger JLink)
- Memory protection unit (MPU)
  - Eight-region MPU with subregions and background region
  - Programmable clock generator unit

### Cryptographic Accelerator

The cryptographic accelerator is a 32-bit APB DMA capable peripheral. There are two 32-bit buffers provided for data input/output operations. These buffers read in or read out 128 bits in four data accesses. Big endian and little endian data formats are supported, as are the following modes:

- Electronic code book (ECB) mode—AES mode
- Counter (CTR) mode
- Cipher block chaining (CBC) mode
- Message authentication code (MAC) mode
- Cipher block chaining-message authentication code (CCM/CCM*) mode
- SHA-256 modes

### True Random Number Generator (TRNG)

The TRNG is used during operations where nondeterministic values are required. This can include generating challenges for secure communication or keys for an encrypted communication channel. The generator can run multiple times to generate a sufficient number of bits for the strength of the intended operation. The TRNG can seed a deterministic random bit generator.

### Reliability and Robustness Features

The ADuCM3027/ADuCM3029 MCUs provide a number of features that can enhance or help achieve certain levels of system safety and reliability. While the level of safety is mainly dominated by system considerations, the following features are provided to enhance robustness:

- ECC enabled flash memory. The entire flash array can be protected to either correct single-bit errors or detect two-bit errors per 64-bit flash data (enabled by default).
- Multiparity bit protected SRAM. Each word of the SRAM and cache memory is protected by multiple parity bits to allow detection of random soft errors.
- Software watchdog. The on-chip watchdog timer can provide software-based supervision of the ADuCM3027/ADuCM3029.

### Cyclic Redundancy Check (CRC) Accelerator

The CRC accelerator computes the CRC for a block of memory locations. The exact memory location can be in the SRAM, flash, or any combination of MMRs. The CRC accelerator generates a checksum that can be compared with an expected signature.

The main features of the CRC include the following:

- Generates a CRC signature for a block of data.
- Supports programmable polynomial length of up to 32 bits.
- Operates on 32 bits of data at a time.
- Supports MSB first and LSB first CRC implementations.
- Various data mirroring capabilities.
- Initial seed to be programmed by user.
- DMA controller (memory to memory transfer) used for data transfer to offload the MCU.

### Programmable GPIOs

The ADuCM3027/ADuCM3029 MCUs have 44 and 36 GPIO pins in the LFCSP and WLCSP packages, respectively, with multiple, configurable functions defined by user code. They can be configured as an input/output and have programmable pull-up resistors. All GPIO pins are functional over the full supply range.

In deep sleep mode, GPIO pins retain their state. On reset, they tristate.

### Timers

The ADuCM3027/ADuCM3029 MCUs have three general-purpose timers and a watchdog timer.

#### General-Purpose Timers

The ADuCM3027/ADuCM3029 MCUs have three identical general-purpose timers, each with a 16-bit up and down counter. The up and down counter can be clocked from one of four user selectable clock sources. Any selected clock source can be scaled down using a prescaler of 1, 16, 64, or 256.

#### Watchdog Timer (WDT)

The WDT is a 16-bit count down timer with a programmable prescaler. The prescaler source is selectable and can be scaled by a factor of 1, 16, or 256. The watchdog timer is clocked by the 32 kHz on-chip oscillator (LFOSC) and recovers from an illegal software state. The WDT requires periodic servicing to prevent it from forcing a reset or interrupt to the MCU.

### Analog-to-Digital Converter (ADC) Subsystem

The ADuCM3027/ADuCM3029 MCUs integrate a 12-bit SAR ADC with up to eight external channels. Conversions can be performed in single or autocycle mode. In single mode, the ADC can be configured to convert on a particular channel by selecting one of the channels. Autocycle mode is provided to reduce MCU overhead of sampling and reading individual channel registers. The ADC can also be used for temperature sensing and measuring battery voltage using dedicated channels. Temperature sensing and battery monitoring cannot be included with external channels in autocycle mode.

A digital comparator triggers an interrupt if ADC input is above or below a programmable threshold. The ADC0_VIN0, ADC0_VIN1, ADC0_VIN2, and ADC0_VIN3 input channels can be used with the digital comparator.

Use the ADC in DMA mode to reduce MCU overhead by moving ADC results directly into SRAM with a single interrupt asserted when the required number of ADC conversions has been completely logged to memory.

The main features of the ADC subsystem include the following:

- 12-bit resolution.
- Programmable ADC update rate from 10 KSPS to 1.8 MSPS.
- Integrated input multiplexer that supports up to eight channels.
- Temperature sensing support.
- Battery monitoring support.
- Software selectable on-chip reference voltage generation—1.25 V and 2.5 V.
- Software selectable internal or external reference.
- Autocycle mode—ability to automatically select a sequence of input channels for conversion.
- Averaging function—converted data on single or multiple channels can be averaged up to 256 samples.
- Alert function—internal digital comparator for ADC0_VIN0, ADC0_VIN1, ADC0_VIN2, and ADC0_VIN3 channels. An interrupt is generated if the digital comparator detects an ADC result above or below a user defined threshold.
- Dedicated DMA channel support.
- Each channel, including temperature sensor and battery monitoring, has a data register for conversion result.

### *Clocking*

The ADuCM3027/ADuCM3029 MCUs have the following clocking options:

- 26 MHz
  - Internal oscillator—HFOSC (26 MHz)
  - External crystal oscillator—HFXTAL (26 MHz or 16 MHz)
  - GPIO clock in—SYS_CLKIN
- 32 kHz
  - Internal oscillator—LFOSC
  - External crystal oscillator—LFXTAL

The clock options have software configurability with the following exceptions:

- HFOSC cannot be disabled when using an internal buck regulator.
- LFOSC cannot be disabled even if using LFXTAL.

### *Real-Time Clock (RTC)*

The ADuCM3027/ADuCM3029 MCUs have two real-time clock blocks—RTC0 and RTC1 (FLEX_RTC). The clock blocks share a low power crystal oscillation circuit that operates in conjunction with a 32,768 Hz external crystal.

The RTC has an alarm that interrupts the core when the programmed alarm value matches the RTC count. The software enables and configures the RTC.

The RTC also has a digital trim capability to allow a positive or negative adjustment to the RTC count at fixed intervals.

The FLEX_RTC supports SensorStrobe mechanism. Using this mechanism, the ADuCM3027/ADuCM3029 MCUs can be used as a programmable clock generator in some power modes, including hibernate mode. In this way, the external sensors can have their timing domains mastered by the ADuCM3027/ADuCM3029 MCUs, as SensorStrobe can output a programmable divider from the FLEX_RTC, which can operate up to a resolution of 30.7 µs. The sensors and MCU are in sync, which removes the need for additional resampling of data to time align it.

In the absence of this mechanism,

- The external sensor uses an RC oscillator (~±30% typical variation). The MCU must sample the data and resample it on the time domain of the MCU before using it.

Or

- The MCU remains in a higher power state and drives each data conversion on the sensor side.

This mechanism allows the ADuCM3027/ADuCM3029 MCUs to be in a lower power state for a long duration and avoids unnecessary data processing which extends the battery life of the end product.

The key differences between RTC0 and RTC1 (FLEX_RTC) are shown in Table 3.

**Table 3. RTC Features**

| Features | RTC0 | RTC1 (FLEX_RTC) |
|---|---|---|
| Resolution of Time Base (Prescaling) | Counts time at 1 Hz in units of seconds. Operationally, always prescales to 1 Hz (for example, divide by 32,768) and always counts real time in units of seconds. | Can prescale the clock by any power of two from 0 to 15. It can count time in units of any of these 16 possible prescale settings. For example, the clock can be prescaled by 1, 2, 4, 8, …, 16384, or 32768. |
| Source Clock | LFXTAL. | Depending on the low frequency multiplexer (LFMUX) configuration, the RTC is clocked by the LFXTAL or the LFOSC. |
| Wake-Up Timer | Wake-up time is specified in units of seconds. | Supports alarm times down to a resolution of 30.7 µs, that is, where the time is specified down to a specific 32 kHz clock cycle. |
| Number of Alarms | One alarm only. Uses an absolute, nonrepeating alarm time, specified in units of 1 sec. | Two alarms. One absolute alarm time and one periodic alarm, repeating every 60 prescaled time units. |
| SensorStrobe Mechanism | Not available. | SensorStrobe is an alarm mechanism in the RTC that causes an output pulse to be sent via GPIOs to an external device to instruct the device to take a measurement or perform some action at a specific time. SensorStrobe events are scheduled at a specific target time relative to the real-time count of the RTC. SensorStrobe can be enabled in active, Flexi, and hibernate modes. |
| Input Capture | Not available. | Input capture takes a snapshot of the RTC when an external device signals an event via a transition on one of the GPIO inputs to the ADuCM3027/ ADuCM3029. Typically, an input-capture event is triggered by an autonomous measurement or action on such a device, which then signals to the ADuCM3027/ ADuCM3029 that the RTC must take a snapshot of time corresponding to the event. Taking the snapshot can wake up the ADuCM3027/ ADuCM3029 and cause an interrupt to the CPU. The CPU can subsequently obtain information from the RTC on the exact 32 kHz cycle on which the input capture event occurred. |

### *Hardware*

The ADuCM3029 EZ-KIT® is available to prototype sensor configurations with the ADuCM3027/ADuCM3029 MCUs.

### *Software*

The ADuCM3029 EZ-KIT includes a complete development and debug environment for the ADuCM3027/ADuCM3029 MCUs. The board support package (BSP) for the ADuCM3027/ADuCM3029 is provided for the IAR Embedded Workbench for ARM, Keil™, and CrossCore® embedded studio (CCES) environments.

The BSP also includes operating system (OS) aware drivers and example code for all the peripherals on the devices.

## ADDITIONAL INFORMATION

The following publications that describe the ADuCM3027/ADuCM3029 MCUs can be ordered from any Analog Devices sales office or accessed electronically on the Analog Devices website:

- ADuCM302x Ultra Low Power ARM Cortex-M3 MCU with Integrated Power Management Hardware Reference.
- ADuCM3027/ADuCM3029 Anomaly List

This data sheet describes the ARM Cortex-M3 core and memory architecture used on the ADuCM3027/ADuCM3029 MCUs, but does not provide detailed programming information for the ARM processor. For more information about programming the ARM processor, visit the ARM Infocenter web page.

The applicable documentation for programming the ARM Cortex-M3 processor include the following:

- *ARM Cortex-M3 Devices Generic User Guide*
- *ARM Cortex-M3 Technical Reference Manual*

## REFERENCE DESIGNS

The Circuits from the Lab® page provides the following:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

## SECURITY FEATURES DISCLAIMER

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# SPECIFICATIONS

For information about product specifications, contact your Analog Devices, Inc. representative.

## OPERATING CONDITIONS

| Parameter | | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{BAT}$[1, 2] | External Battery Supply Voltage | | 1.74 | 3.0 | 3.6 | V |
| $V_{IH}$ | High Level Input Voltage | $V_{BAT}$ = 3.6 V | 2.5 | | | V |
| $V_{IL}$ | Low Level Input Voltage | $V_{BAT}$ = 1.74 V | | | 0.45 | V |
| $V_{BAT\_ADC}$ | ADC Supply Voltage | | 1.74 | 3.0 | 3.6 | V |
| $T_J$ | Junction Temperature | $T_{AMBIENT}$ = −40°C to +85°C | −40 | | +85 | °C |

[1] The voltage must remain powered even if the associated function is not used.
[2] Value applies to the VBAT_ANA1,VBAT_ANA2,VBAT_DIG1, and VBAT_DIG2 pins.

## ELECTRICAL CHARACTERISTICS

| Parameter | | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$[1] | High Level Output Voltage | $V_{BAT}$ = minimum V, $I_{OH}$ = −1.0 mA | 1.4 | | | V |
| $V_{OL}$[1] | Low Level Output Voltage | $V_{BAT}$ = minimum V, $I_{OL}$ = 1.0 mA | | | 0.4 | V |
| $I_{IHPU}$[2] | High Level Input Current Pull-Up | $V_{BAT}$ = maximum V, $V_{IN}$ = maximum $V_{BAT}$ | | 0.01 | 1 | µA |
| $I_{ILPU}$[2] | Low Level Input Current Pull-Up | $V_{BAT}$ = maximum V, $V_{IN}$ = 0 V | | | 100 | µA |
| $I_{OZH}$[3] | Three-State Leakage Current | $V_{BAT}$ = maximum V, $V_{IN}$ = maximum $V_{BAT}$ | | 0.01 | 1 | µA |
| $I_{OZL}$[3] | Three-State Leakage Current | $V_{BAT}$ = maximum V, $V_{IN}$ = 0 V | | 0.01 | 1 | µA |
| $I_{OZLPU}$[4] | Three-State Leakage Current Pull-Up | $V_{BAT}$ = maximum V, $V_{IN}$ = 0 V | | | 100 | µA |
| $I_{OZHPU}$[4] | Three-State Leakage Current Pull-Up | $V_{BAT}$ = maximum V, $V_{IN}$ = maximum $V_{BAT}$ | | | 1 | µA |
| $I_{OZLPD}$[5] | Three-State Leakage Current Pull-Down | $V_{BAT}$ = maximum V, $V_{IN}$ = 0 V | | | 1 | µA |
| $I_{OZHPD}$[5] | Three-State Leakage Current Pull-Down | $V_{BAT}$ = maximum V, $V_{IN}$ = maximum $V_{BAT}$ | | | 100 | µA |
| $C_{IN}$ | Input Capacitance | $T_J$ = 25°C | | 10 | | pF |

[1] Applies to the output and bidirectional pins: P1_10, P0_10, P0_11, P1_02, P1_03, P1_04, P1_05, P2_01, P0_13, P0_15, P1_00, P1_01, P1_15, P2_00, P0_12, P2_11, P1_06, P1_07, P1_08, P1_09, P0_00, P0_01, P0_02, P0_03, P0_06, P0_07, P2_03, P2_04, P2_05, P2_06, P2_07, P2_08, P2_09, P2_10, P0_04, P0_05, P0_14, P2_02, P1_14, P1_13, P1_12, P1_11, P0_08, and P0_09.
[2] Applies to the input pin with pull-up: $\overline{\text{SYS\_HWRST}}$.
[3] Applies to the three-statable pins: P1_10, P0_10, P0_11, P1_02, P1_03, P1_04, P1_05, P2_01, P0_13, P0_15, P1_00, P1_15, P2_00, P0_12, P2_11, P1_06, P1_07, P1_08, P1_09, P0_00, P0_01, P0_02, P0_03, P2_03, P2_04, P2_05, P2_06, P2_07, P2_08, P2_09, P2_10, P0_04, P0_05, P0_14, P2_02, P1_14, P1_13, P1_12, P1_11, P0_08, and P0_09.
[4] Applies to the three-statable pins with pull-ups: P1_10, P0_10, P0_11, P1_02, P1_03, P1_04, P1_05, P2_01, P0_13, P0_15, P1_00, P1_15, P2_00, P0_12, P2_11, P1_06, P1_07, P1_08, P1_09, P0_00, P0_01, P0_02, P0_03, P2_03, P2_04, P2_05, P2_06, P2_07, P2_08, P2_09, P2_10, P0_04, P0_05, P0_14, P2_02, P1_14, P1_13, P1_12, P1_11, P0_08, P0_09, P0_07, and P1_01.
[5] Applies to the three-statable pin with pull-down: P0_06.

### *Power Supply Current*

Table 4, Table 5, and Table 6 describe power supply current for $V_{BAT}$.

**Table 4. Active Mode—Current Consumption When $V_{BAT}$ = 3.0 V**

| Conditions | Buck | Typ[1] | Max[2] | Unit |
|---|---|---|---|---|
| Code[3] executing from flash, cache enabled, peripheral clocks off, HCLK = 6.5 MHz | Enabled | 0.40 | | mA |
| Code[3] executing from flash, cache enabled, peripheral clocks off, HCLK = 26 MHz | Enabled | 0.98 | 1.29 | mA |
| | Disabled | 1.75 | 2.38 | mA |
| Code[3] executing from flash, cache disabled, peripheral clocks off, HCLK = 26 MHz | Enabled | 1.28 | 1.64 | mA |
| | Disabled | 2.34 | 3.0 | mA |
| Code[3] executing from SRAM, peripheral clocks off, HCLK = 26 MHz | Enabled | 0.95 | 1.36 | mA |
| | Disabled | 1.78 | 2.48 | mA |
| Code[3] executing from flash, cache enabled, peripheral clocks on, HCLK = 26 MHz, PCLK = 26 MHz | Enabled | 1.08 | 1.43 | mA |
| | Disabled | 1.99 | 2.67 | mA |
| Code[3] executing from flash, cache disabled, peripheral clocks on, HCLK = 26 MHz, PCLK = 26 MHz | Enabled | 1.37 | 1.78 | mA |
| | Disabled | 2.55 | 3.29 | mA |
| Code[3] executing from SRAM, peripheral clocks on, HCLK = 26 MHz, PCLK = 26 MHz | Enabled | 1.08 | 1.49 | mA |
| | Disabled | 2.03 | 2.74 | mA |

[1] $T_J$ = 25°C.
[2] $T_J$ = 85°C.
[3] The code being executed is a prime number generation in a continuous loop, with HFOSC as the system clock source.

**Table 5. Flexi™ Mode—Current Consumption When $V_{BAT}$ = 3.0 V**

| Conditions | Buck | Typ[1] | Max[2] | Unit |
|---|---|---|---|---|
| Peripheral clocks off | Enabled | 0.3 | 0.67 | mA |
| | Disabled | 0.52 | 1.11 | mA |
| Peripheral clocks on, PCLK = 26 MHz | Enabled | 0.39 | 0.80 | mA |
| | Disabled | 0.7 | 1.38 | mA |

[1] $T_J$ = 25°C.
[2] $T_J$ = 85°C.

**Table 6. Deep Sleep Modes[1]—Current Consumption When $V_{BAT}$ = 3.0 V**

| Mode | Conditions | −40°C Typ | +25°C Typ | +85°C Typ | +85°C Max | Unit |
|---|---|---|---|---|---|---|
| Hibernate | RTC1 and RTC0 disabled, 8 KB SRAM retained, LFXTAL off | 0.66 | 0.75 | 2.0 | 6.05 | µA |
| | RTC1 and RTC0 disabled, 16 KB SRAM retained, LFXTAL off | 0.67 | 0.77 | 2.4 | 6.4 | µA |
| | RTC1 and RTC0 disabled, 24 KB SRAM retained, LFXTAL off | 0.68 | 0.79 | 2.6 | 6.75 | µA |
| | RTC1 and RTC0 disabled, 32 KB SRAM retained, LFXTAL off | 0.69 | 0.81 | 3.0 | 7.1 | µA |
| | RTC1 enabled, 8 KB SRAM retained, LFOSC as source for RTC1 | 0.69 | 0.78 | 2.05 | 6.1 | µA |
| | RTC1 enabled, 8 KB SRAM retained, LFXTAL as source for RTC1 | 0.74 | 0.83 | 2.1 | 6.15 | µA |
| | RTC1 and RTC0 enabled, 8 KB SRAM retained, LFXTAL as source for RTC1 and RTC0 | 0.83 | 0.93 | 2.25 | 6.3 | µA |
| Shutdown | RTC0 enabled, LFXTAL as source for RTC0 | 290 | 310 | 490 | 1180 | nA |
| | RTC0 disabled | 40 | 56 | 260 | 950 | nA |

[1] Buck enable/disable selection does not affect power consumption.

## ADC SPECIFICATIONS

**Table 9. ADC Specifications**

| Parameter[1, 2] | VBAT/VREF (V) | Package | Typ | Unit | Conditions |
|---|---|---|---|---|---|
| NO MISSING CODE | 1.8/1.25 (internal/external) | 64-lead LFCSP | 12 | Bits | $F_{in}$ = 1068 Hz, $F_s$ = 100 KSPS, internal reference in low power mode, 400,000 samples end point method used |
| | 1.8/1.25 (internal/external) | 54-ball WLCSP | 12 | Bits | |
| | 3.0/2.5 (internal/external) | 64-lead LFCSP | 12 | Bits | |
| INTEGRAL NONLINEARITY ERROR | 1.8/1.25 (internal/external) | 64-lead LFCSP | ±1.6 | LSB | |
| | 1.8/1.25 (internal/external) | 54-ball WLCSP | ±1.8 | LSB | |
| | 3.0/2.5 (internal/external) | 64-lead LFCSP | ±1.4 | LSB | |
| DIFFERENTIAL NONLINEARITY ERROR | 1.8/1.25 (internal/external) | 64-lead LFCSP | −0.7, +1.15 | LSB | |
| | 1.8/1.25 (internal/external) | 54-ball WLCSP | −0.75, +1.2 | LSB | |
| | 3.0/2.5 (internal/external) | 64-lead LFCSP | −0.7, +1.1 | LSB | |
| OFFSET ERROR | 1.8/1.25 (external) | 64-lead LFCSP | ±0.5 | LSB | |
| | 1.8/1.25 (external) | 54-ball WLCSP | ±0.5 | LSB | |
| | 3.0/2.5 (external) | 64-lead LFCSP | ±0.5 | LSB | |
| GAIN ERROR | 1.8/1.25 (external) | 64-lead LFCSP | ±2.5 | LSB | |
| | 1.8/1.25 (external) | 54-ball WLCSP | ±3.0 | LSB | |
| | 3.0/2.5 (external) | 64-lead LFCSP | ±0.5 | LSB | |
| $I_{VBAT\_ADC}$[3] | 1.8/1.25 (internal) | 64-lead LFCSP | 104 | µA | $F_{in}$ = 1068 Hz, $F_s$ = 100 KSPS, internal reference in low power mode |
| | 1.8/1.25 (internal) | 54-ball WLCSP | 108 | µA | |
| | 3.0/2.5 (internal) | 64-lead LFCSP | 131 | µA | |

[1] The ADC is characterized in standalone mode without core activity and minimal or no switching on the adjacent ADC channels and digital inputs/outputs.
[2] The specifications are characterized after performing internal ADC offset calibration.
[3] Current consumption from VBAT_ADC supply when ADC is performing the conversion.

## FLASH SPECIFICATIONS

**Table 10. Flash Specifications**

| Parameter | Min | Typ | Max | Unit | Conditions |
|---|---|---|---|---|---|
| FLASH | | | | | |
| Endurance | 10,000 | | | Cycles | |
| Data Retention | | 10 | | Years | |

**Table 16. Serial Ports—Internal Clock**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| TIMING REQUIREMENTS | | | | |
| $t_{SDRI}$ | Receive Data Setup Before SPT_CLK[1] | 25 | | ns |
| $t_{HDRI}$ | Receive Data Hold After SPT_CLK[1] | 0 | | ns |
| SWITCHING CHARACTERISTICS | | | | |
| $t_{DFSI}$ | Frame Sync Delay After SPT_CLK (Internally Generated Frame Sync in Transmit or Receive Mode)[2] | | 20 | ns |
| $t_{HOFSI}$ | Frame Sync Hold After SPT_CLK (Internally Generated Frame Sync in Transmit or Receive Mode)[2] | –8 | | ns |
| $t_{DDTI}$ | Transmit Data Delay After SPT_CLK[2] | | 20 | ns |
| $t_{HDTI}$ | Transmit Data Hold After SPT_CLK[2] | –7 | | ns |
| $t_{SCLKIW}$ | SPT_CLK Width | $t_{PCLK}$ – 1.5 | | ns |
| $t_{SPTCLK}$ | SPT_CLK Period | 2 × $t_{PCLK}$ – 1 | | ns |

[1] This specification is referenced to the sample edge.
[2] This specification is referenced to the drive edge.

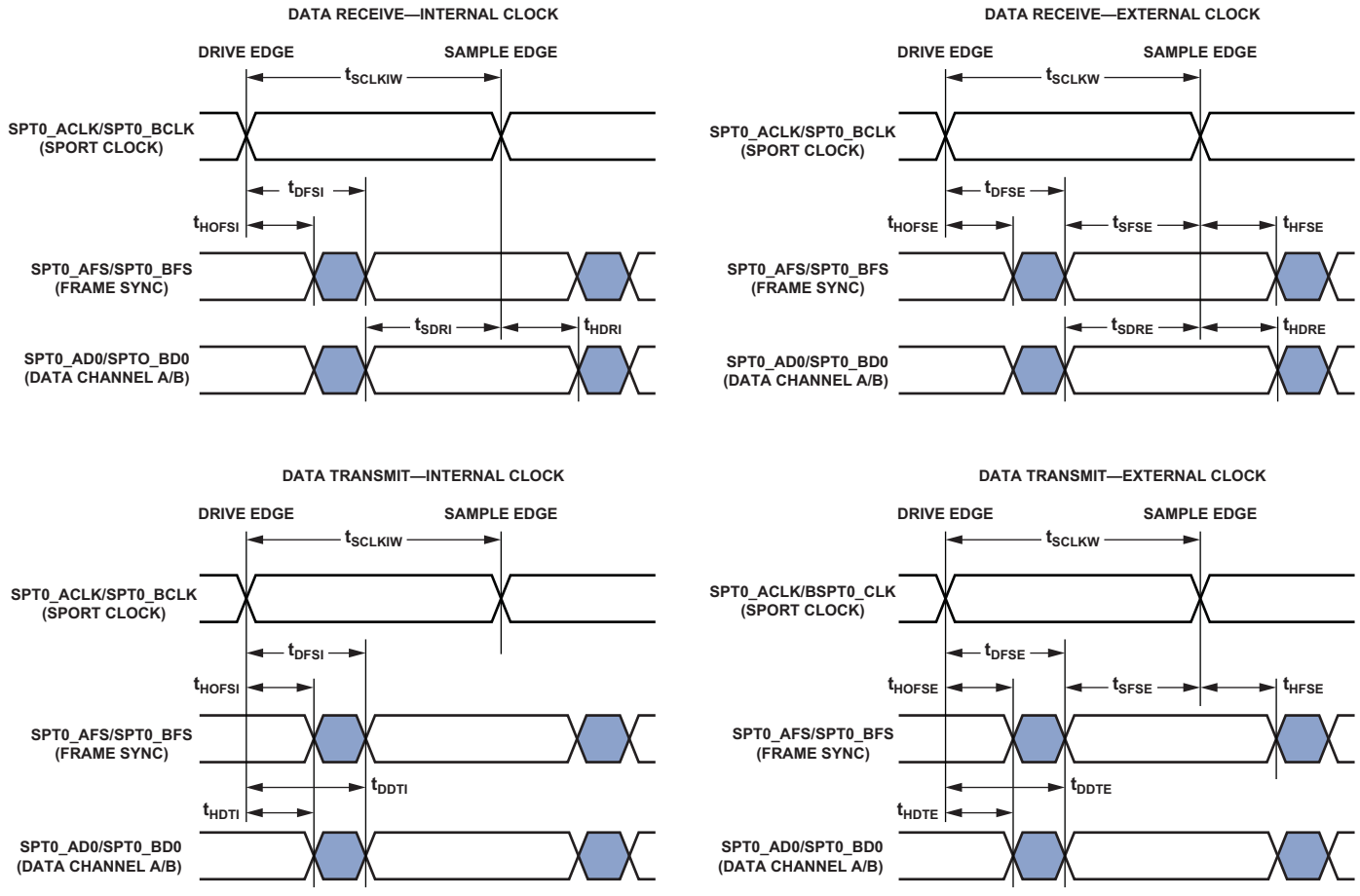


*Figure 6. Serial Ports*

**Table 17. Serial Ports—Enable and Three-State**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| SWITCHING CHARACTERISTICS | | | | |
| $t_{DDTIN}$ | Data Enable From Internal Transmit SPT_CLK[1] | 5 | | ns |
| $t_{DDTTI}$ | Data Disable From Internal Transmit SPT_CLK[1] | | 160 | ns |

[1] This specification is referenced to the drive edge.

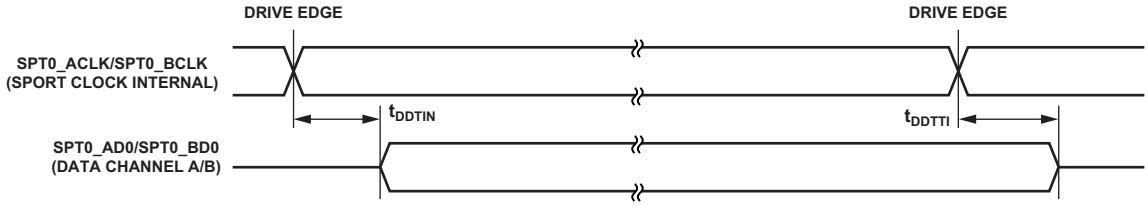


*Figure 7. Serial Ports—Enable and Three-State*

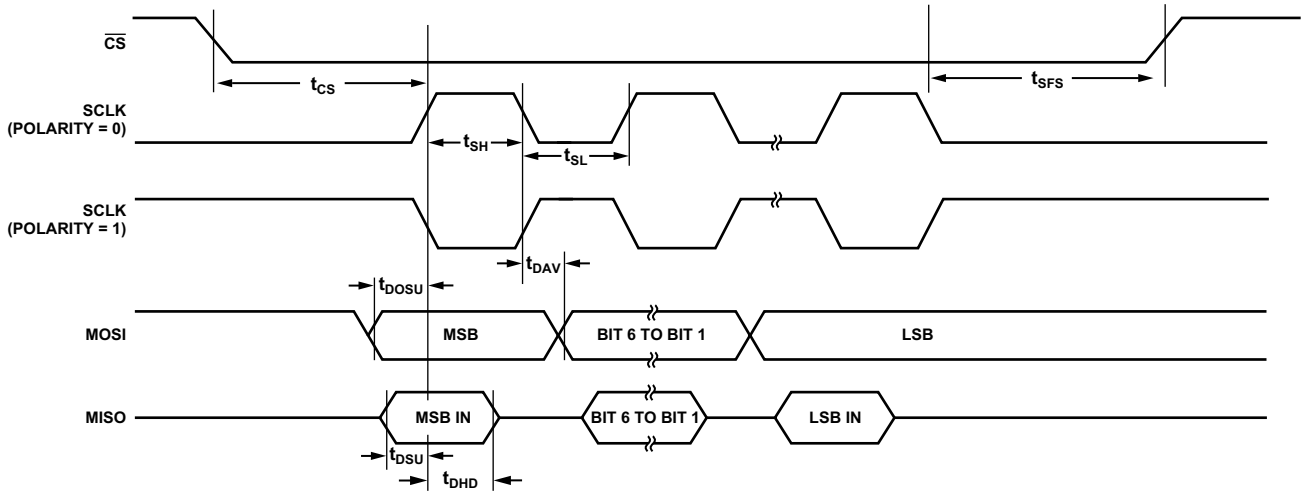


*Figure 9. SPI Master Mode Timing (Phase Mode = 0)*

**Table 19. SPI Slave Mode Timing**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| TIMING REQUIREMENTS | | | | |
| $t_{CS}$ | $\overline{CS}$ to SCLK Edge | 38.5 | | ns |
| $t_{SL}$ | SCLK Low Pulse Width | 38.5 | | ns |
| $t_{SH}$ | SCLK High Pulse Width | 38.5 | | ns |
| $t_{DSU}$ | Data Input Setup Time Before SCLK Edge | 6 | | ns |
| $t_{DHD}$ | Data Input Hold Time After SCLK Edge | 8 | | ns |
| SWITCHING CHARACTERISTICS | | | | |
| $t_{DAV}$ | Data Output Valid After SCLK Edge | 25 | | ns |
| $t_{DOCS}$ | Data Output Valid After $\overline{CS}$ Edge | | 20 | ns |
| $t_{SFS}$ | $\overline{CS}$ High After SCLK Edge | 38.5 | | ns |

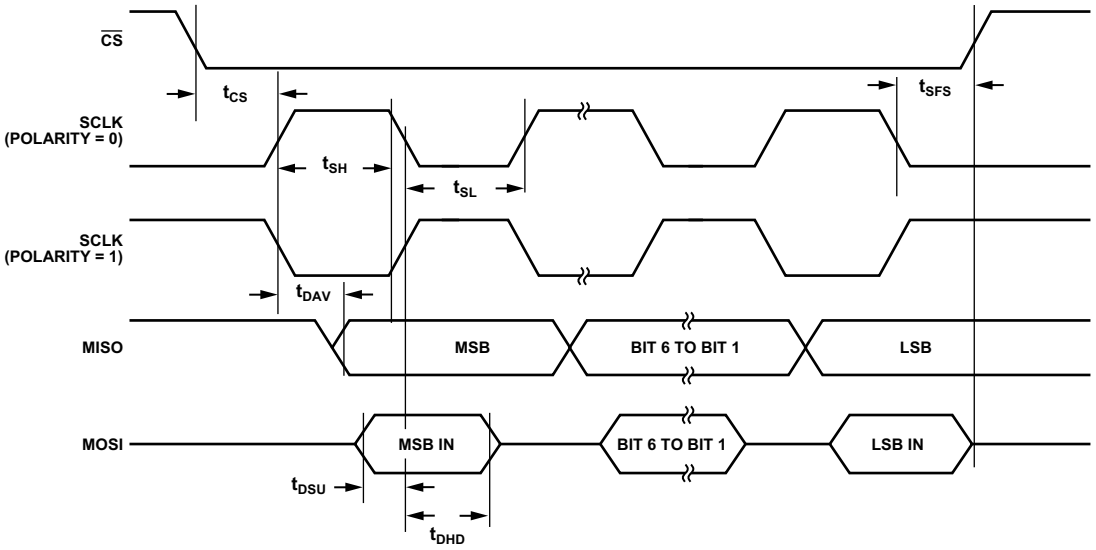


*Figure 10. SPI Slave Mode Timing (Phase Mode = 1)*

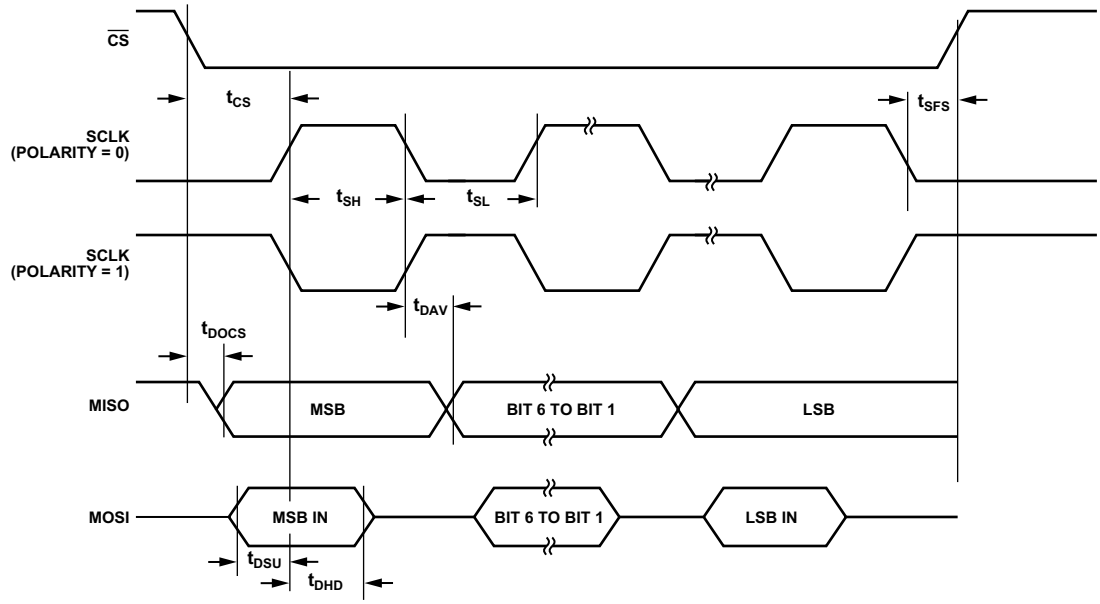


*Figure 11. SPI Slave Mode Timing (Phase Mode = 0)*

### General-Purpose Port Timing

Table 20 and Figure 12 describe general-purpose port timing.

**Table 20. General-Purpose Port Timing**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| TIMING REQUIREMENTS | | | | |
| $t_{WFI}$ | General-Purpose Port Pin Input Pulse Width | $4 \times t_{PCLK}$ | | ns |

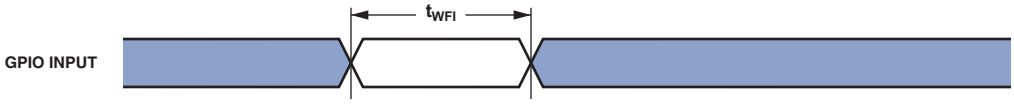


*Figure 12. General-Purpose Port Timing*

### Timer PWM_OUT Cycle Timing

Table 21 and Figure 13 describe timer PWM_OUT cycle timing.

**Table 21. Timer PWM_OUT Cycle Timing**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| SWITCHING CHARACTERISTICS | | | | |
| $t_{PWMO}$ | Timer Pulse Width Output | $4 \times t_{PCLK} - 6$ | $256 \times (2^{16} - 1)$ | ns |

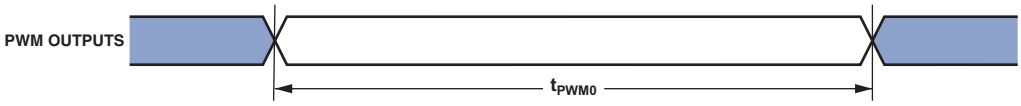


*Figure 13. Timer PWM_OUT Cycle Timing*

Figure 16 through Figure 21 show the typical current voltage characteristics for the output drivers of the MCU.

The curves represent the current drive capability of the output drivers as a function of output voltage.

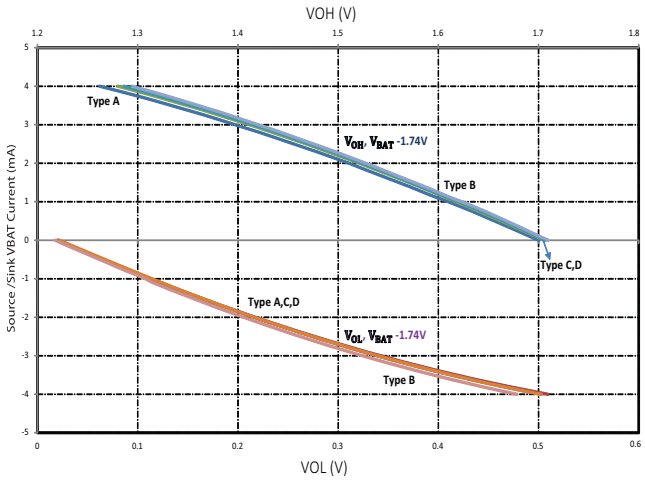


*Figure 16. Output Double Drive Strength Characteristics (VBAT = 1.74 V)*

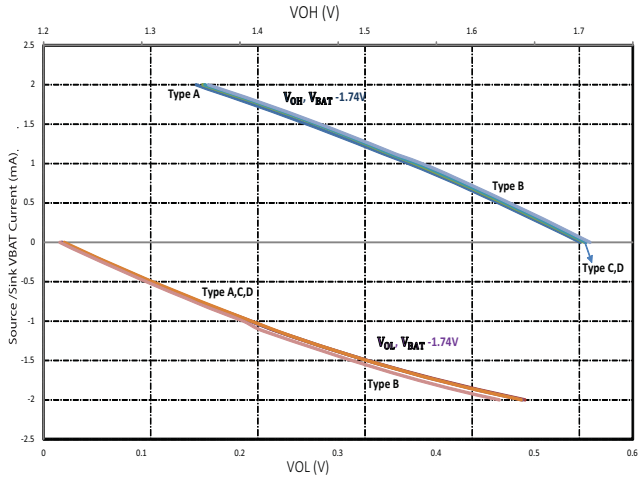


*Figure 17. Output Single Drive Strength Characteristics (VBAT = 1.74 V)*

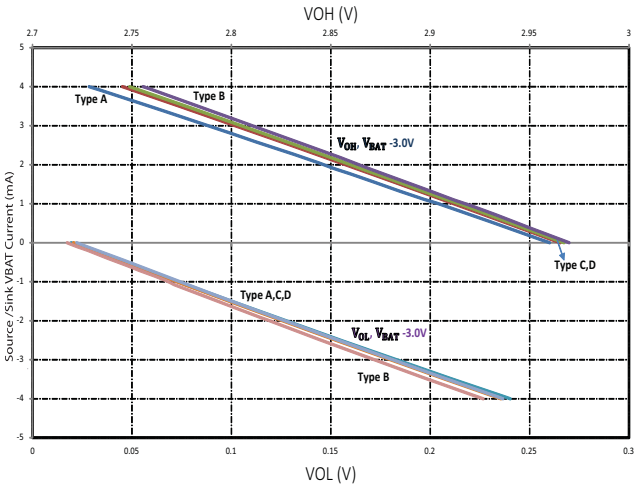


*Figure 18. Output Double Drive Strength Characteristics (VBAT = 3.0 V)*

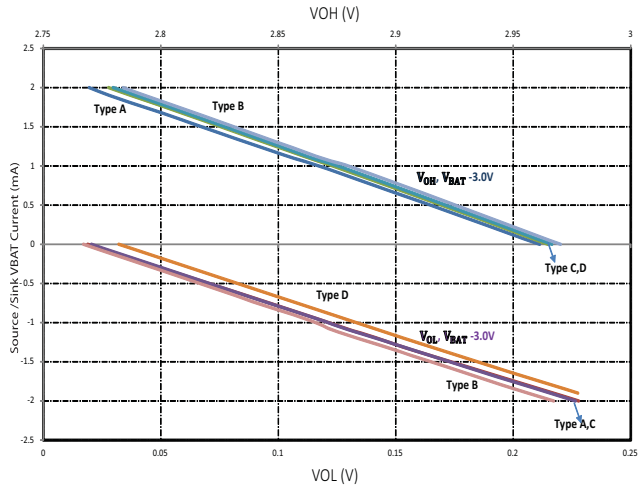


*Figure 19. Output Single Drive Strength Characteristics (VBAT = 3.0 V)*

## ENVIRONMENTAL CONDITIONS

**Table 23. Thermal Characteristics (64-Lead LFCSP)**

| Parameter | Typ | Unit |
|---|---|---|
| $\theta_{JA}$ | 28.2 | °C/W |
| $\theta_{JC}$ | 5.4 | °C/W |

Values of $\theta_{JA}$ are provided for package comparison and PCB design considerations. $\theta_{JA}$ can be used for a first-order approximation of $T_J$ by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:
$T_A$ is ambient temperature (°C).
$T_J$ is junction temperature (°C).
$P_D$ is power dissipation (To calculate $P_D$, see the Power Supply Current section).

Values of $\theta_{JC}$ are provided for package comparison and PCB design considerations when an external heat sink is required.

Table 24 lists the signal descriptions of the ADuCM3027/ADuCM3029 MCUs.

**Table 24. Signal Functional Descriptions**

| GPIO Signal Name | Description |
|---|---|
| SPIn_CLK | SPI Clock. n = 0, 1, 2. |
| SPIn_MOSI | SPI Master Out Slave In. n = 0, 1, 2. |
| SPIn_MISO | SPI Master In Slave Out. n = 0, 1, 2. |
| SPIn_RDY | SPI Ready Signal. n = 0, 1, 2. |
| SPIn_CSm | SPI Chip Select Signal. n = 0, 1, 2 and m = 0, 1, 2, 3. |
| SPT0_ACLK | SPORT A Clock Signal. |
| SPT0_AFS | SPORT A Frame Sync. |
| SPT0_AD0 | SPORT A Data Pin 0. |
| SPT0_ACNV | SPORT A Converter Signal for Interface with ADC. |
| SPT0_BCLK | SPORT B Clock Signal. |
| SPT0_BFS | SPORT B Frame Sync. |
| SPT0_BD0 | SPORT B Data Pin 0. |
| SPT0_BCNV | SPORT B Converter Signal for Interface with ADC. |
| I2C0_SCL | $I^2C$ Clock. |
| I2C0_SDA | $I^2C$ Data. |
| SWD0_CLK | Serial Wire Debug Clock. |
| SWD0_DATA | Serial Wire Debug Data. |
| BPR0_TONE_N | Beeper Tone Negative Pin. |
| BPR0_TONE_P | Beeper Tone Positive Pin. |
| UART0_TX | UART Transmit Pin. |
| UART0_RX | UART Receive Pin. |
| UART0_SOUT_EN | UART Serial Data Out Pin. |
| XINT0_WAKEn | System Wake-Up Pin. Wake Up from Flexi/Hibernate/Shutdown Modes[1]. n = 0, 1, 2, 3. |
| TMRn_OUT | Timer Output Pin. n = 0, 1, 2. |
| SYS_BMODE0 | Boot Mode Pin. |
| SYS_CLKIN | External Clock In Pin. |
| SYS_CLKOUT | External Clock Out Pin. |
| RTC1_SS1 | RTC1 SensorStrobe Pin. |
| ADC0_VINn | ADC Voltage Input Pin. n = 0, 1, 2, 3, 4, 5, 6, 7. |

[1] For shutdown, XINT0_WAKE3 is not capable of waking the device from shutdown mode.

Table 26 lists the 54-Ball WLCSP package by ball number for the ADuCM3027/ADuCM3029 MCUs.

**Table 26. Pin Function Descriptions, 54-Ball WLCSP**

| Ball No. | GPIO | Pin Label | Description | GPIO Pull |
|---|---|---|---|---|
| A01 | | VBAT_ANA1 | Analog 3 V Supply. | |
| A03 | | SYS_HFXTAL_OUT | 26 MHz High Frequency Crystal. | |
| A05 | | SYS_LFXTAL_IN | 32 kHz Low Frequency Crystal. | |
| A07 | | VDCDC_CAP1P | Buck Fly Capacitor. | |
| A09 | | VDCDC_CAP2N | Buck Fly Capacitor. | |
| A11 | | VLDO_OUT | LDO Output Capacitor | |
| A13 | | VBAT_ADC | Analog 3 V Supply for ADC. | |
| B01 | P0_00 | SPI0_CLK/SPT0_BCLK/GPIO00 | | PU |
| B03 | | SYS_HFXTAL_IN | 26 MHz High Frequency Crystal. | |
| B05 | | SYS_LFXTAL_OUT | 32 kHz Low Frequency Crystal. | |
| B07 | | VDCDC_CAP1N | Buck Fly Capacitor. | |
| B09 | | VDCDC_CAP2P | Buck Fly Capacitor. | |
| B11 | | VREF_ADC | Analog Reference Voltage for ADC. | |
| B13 | P2_03 | ADC0_VIN0/GPIO35 | | PU |
| C01 | P0_03 | SPI0_CS0/SPT0_BCNV/SPI2_RDY/GPIO03 | | PU |
| C03 | P0_01 | SPI0_MOSI/SPT0_BFS/GPIO01 | | PU |
| C05 | P0_02 | SPI0_MISO/SPT0_BD0/GPIO02 | | PU |
| C07 | | VBAT_ANA2 | Analog 3 V Supply. | |
| C09 | | VDCDC_OUT | Buck Output Capacitor. | |
| C11 | | GND_VREFADC | Reference Ground for ADC. | |
| C13 | P2_05 | ADC0_VIN2/GPIO37 | | PU |
| D01 | P0_10 | UART0_TX/GPIO10 | | PU |
| D03 | P1_10 | SPI0_CS1/SYS_CLKIN/SPI1_CS3/GPIO26 | | PU |
| D05 | P0_11 | UART0_RX/GPIO11 | | PU |
| D07 | | GND_ANA | Analog Ground. | |
| D09 | P2_04 | ADC0_VIN1/GPIO36 | | PU |
| D11 | P2_06 | ADC0_VIN3/GPIO38 | | PU |
| D13 | P0_05 | I2C0_SDA/GPIO05 | | PU |
| E01 | P1_03 | SPI2_MOSI/GPIO19 | | PU |
| E03 | P1_02 | SPI2_CLK/GPIO18 | | PU |
| E05 | | GND_DIG | Digital Ground. | |
| E07 | | $\overline{\text{SYS\_HWRST}}$ | System Hardware Reset. | |
| E09 | P0_04 | I2C0_SCL/GPIO04 | | PU |
| E11 | P0_07 | GPIO07/SWD0_DATA | | PU |
| E13 | P0_06 | GPIO06/SWD0_CLK | | PD |
| F02 | P2_01 | XINT0_WAKE3/TMR2_OUT/GPIO33 | | PU |
| F04 | P1_05 | SPI2_CS0/GPIO21 | | PU |
| F06 | P1_04 | SPI2_MISO/GPIO20 | | PU |
| F08 | P1_09 | SPI1_CS0/GPIO25 | | PU |
| F10 | P1_08 | SPI1_MISO/GPIO24 | | PU |
| F12 | P1_07 | SPI1_MOSI/GPIO23 | | PU |
| G01 | | VBAT_DIG2 | Digital 3 V Supply. | |
| G03 | P0_15 | XINT0_WAKE0/GPIO15 | | PU |

**Table 26. Pin Function Descriptions, 54-Ball WLCSP (Continued)**

| Ball No. | GPIO | Pin Label | Description | GPIO Pull |
|---|---|---|---|---|
| G05 | P0_13 | XINT0_WAKE2/GPIO13 | | PU |
| G07 | P1_01 | GPIO17/SYS_BMODE0 | | PU |
| G09 | P1_06 | SPI1_CLK/GPIO22 | | PU |
| G11 | P2_11 | SPI1_CS1/SYS_CLKOUT/GPIO43/RTC1_SS1 | | PU |
| G13 | | VBAT_DIG1 | Digital 3 V Supply. | |
| H02 | P1_00 | XINT0_WAKE1/GPIO16 | | PU |
| H04 | P0_14 | TMR0_OUT/SPI1_RDY/GPIO14 | | PU |
| H06 | P1_14 | SPI0_RDY/GPIO30 | | PU |
| H08 | P0_08 | BPR0_TONE_N/GPIO08 | | PU |
| H10 | P0_09 | BPR0_TONE_P/SPI2_CS1/GPIO09 | | PU |
| H12 | P0_12 | SPT0_AD0/GPIO12/UART0_SOUT_EN | | PU |

# OUTLINE DIMENSIONS

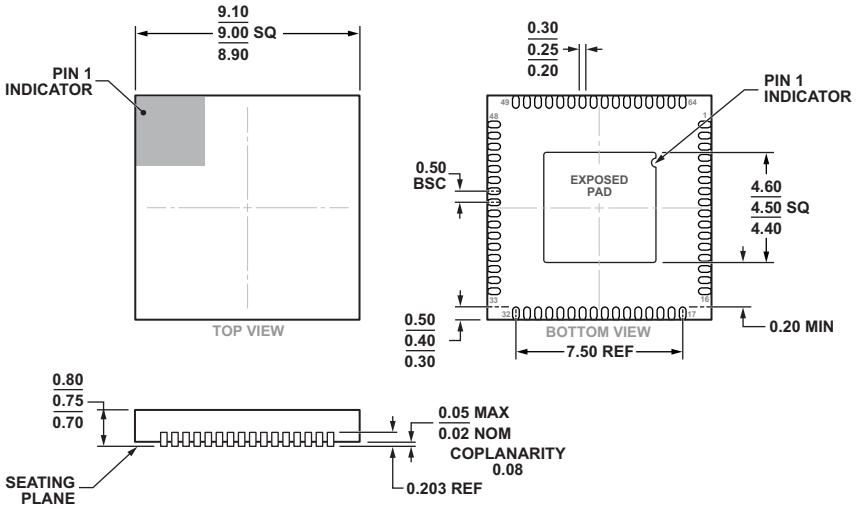


*Figure 24. 64-Lead Frame Chip Scale Package [LFCSP]*
*9 mm x 9 mm Body and 0.75 mm Package Height*
*(CP-64-16)*
*Dimensions shown in mm*
*Note: Exposed pad must be grounded*

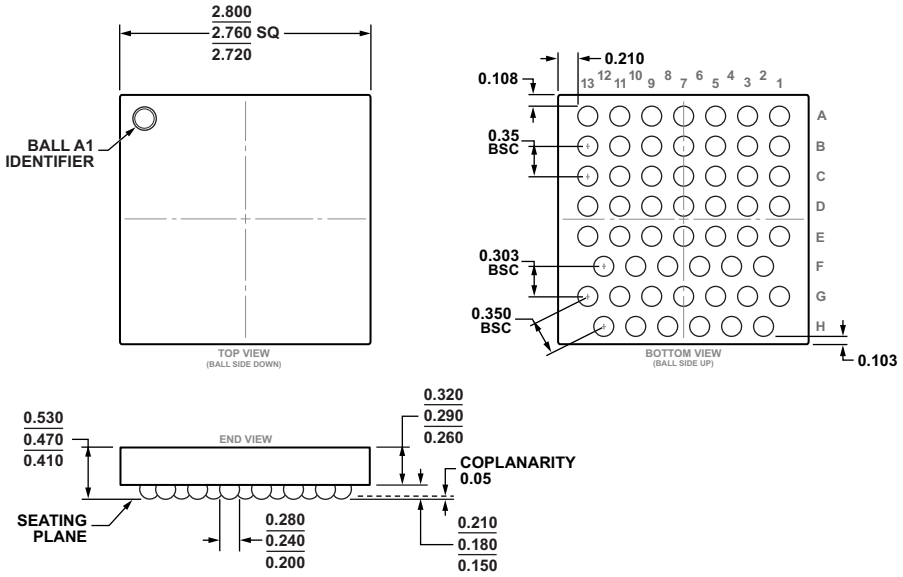


*Figure 25. 54-Ball Wafer Level Chip Scale Package [WLCSP]*
*(CB-54-1)*
*Dimensions shown in mm*

## ORDERING GUIDE

| Model[1] | Description | Temperature[2, 3] | Package Description | Package Option |
|---|---|---|---|---|
| ADUCM3027BCBZ-RL | ULP ARM Cortex-M3 with 128 KB Embedded Flash | −40°C to +85°C | 54-Ball WLCSP, 13″ Reel | CB-54-1 |
| ADUCM3027BCBZ-R7 | ULP ARM Cortex-M3 with 128 KB Embedded Flash | −40°C to +85°C | 54-Ball WLCSP, 7″ Reel | CB-54-1 |
| ADUCM3027BCPZ | ULP ARM Cortex-M3 with 128 KB Embedded Flash | −40°C to +85°C | 64-Lead LFCSP | CP-64-16 |
| ADUCM3027BCPZ-RL | ULP ARM Cortex-M3 with 128 KB Embedded Flash | −40°C to +85°C | 64-Lead LFCSP, 13″ Reel | CP-64-16 |
| ADUCM3027BCPZ-R7 | ULP ARM Cortex-M3 with 128 KB Embedded Flash | −40°C to +85°C | 64-Lead LFCSP, 7″ Reel | CP-64-16 |
| ADUCM3029BCBZ-RL | ULP ARM Cortex-M3 with 256 KB Embedded Flash | −40°C to +85°C | 54-Ball WLCSP, 13″ Reel | CB-54-1 |
| ADUCM3029BCBZ-R7 | ULP ARM Cortex-M3 with 256 KB Embedded Flash | −40°C to +85°C | 54-Ball WLCSP, 7″ Reel | CB-54-1 |
| ADUCM3029BCPZ | ULP ARM Cortex-M3 with 256 KB Embedded Flash | −40°C to +85°C | 64-Lead LFCSP | CP-64-16 |
| ADUCM3029BCPZ-RL | ULP ARM Cortex-M3 with 256 KB Embedded Flash | −40°C to +85°C | 64-Lead LFCSP, 13″ Reel | CP-64-16 |
| ADUCM3029BCPZ-R7 | ULP ARM Cortex-M3 with 256 KB Embedded Flash | −40°C to +85°C | 64-Lead LFCSP, 7″ Reel | CP-64-16 |
| ADZS-UCM3029EZLITE | ADuCM3029 Evaluation Kit | −40°C to +85°C | 64-Lead LFCSP | CP-64-16 |

[1] Z = RoHS Compliant Part.
[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. See the Absolute Maximum Ratings section for $T_J$ (junction temperature) specification which is the only temperature specification.
[3] These are preproduction devices. See ENG-Grade agreement for details.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).


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