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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVR, POR, PWM, WDT
Number of I/O	56
Program Memory Size	36KB (36K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/m0518sc2ae

List of Tables

channels
- Supports independent mode for BPWM output/Capture input channel
- Supports 12-bit pre-scalar from 1 to 4096
- Supports 16-bit resolution BPWM counter
  - Up, down and up/down counter operation type
- Supports mask function and tri-state enable for each BPWM pin
- Supports interrupt on the following events:
  - BPWM counter match zero, period value or compared value
- Supports trigger ADC on the following events:
  - BPWM counter match zero, period value or compared value
- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising edges, falling edges or both edges capture condition
- Supports input rising edges, falling edges or both edges capture interrupt
- Supports rising edges, falling edges or both edges capture with counter reload option

- PWM/Capture
  - Supports maximum clock frequency up to 100MHz
  - Supports up to two PWM modules, each module provides three 16-bit timers and 6 output channels
  - Supports independent mode for PWM output/Capture input channel
  - Supports complementary mode for 3 complementary paired PWM output channel
    - Dead-time insertion with 12-bit resolution
    - Two compared values during one period
  - Supports 12-bit pre-scalar from 1 to 4096
  - Supports 16-bit resolution PWM counter
    - Up, down and up/down counter operation type
  - Supports mask function and tri-state enable for each PWM pin
  - Supports brake function
    - Brake source from pin and system safety events (clock failed, Brown-out detection and CPU lockup)
    - Noise filter for brake source from pin
    - Edge detect brake source to control brake state until brake interrupt cleared
    - Level detect brake source to auto recover function after brake condition removed
  - Supports interrupt on the following events:
    - PWM counter match zero, period value or compared value
    - Brake condition happened
  - Supports trigger ADC on the following events:
    - PWM counter match zero, period value or compared value
  - Supports up to 12 capture input channels with 16-bit resolution
  - Supports rising edges, falling edges or both edges capture condition
  - Supports input rising edges, falling edges or both edges capture interrupt
  - Supports rising edges, falling edges or both edges capture with counter reload option
- UART
  - Up to six UART controllers
  - UART0 and UART1 ports with flow control (TXD, RXD, nCTS and nRTS)
  - UART0, UART1 and UART2 with 16-byte FIFO for standard device
  - Supports IrDA (SIR) and LIN function
  - Supports RS-485 9-bit mode and direction control
  - Supports auto baud-rate generator
- SPI
  - One set of SPI controller
  - Supports SPI Master/Slave mode
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 8 to 32 bits
  - MSB or LSB first data transfer
  - Rx and Tx on both rising or falling edge of serial clock independently

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 NuMicro™ M0518 Series Selection Code

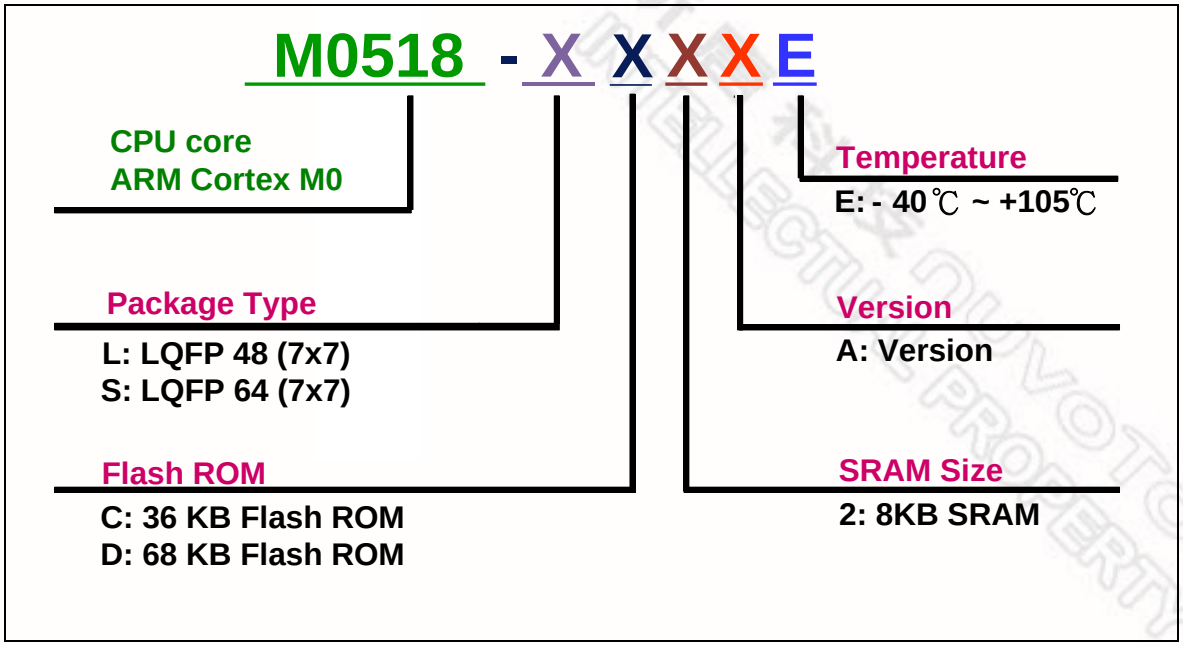


Figure 4-1 NuMicro™ M0518 Series Selection Code

4.3.1.2 NuMicro™ M0518LxxAE LQFP 48 pin (7 mm * 7mm)

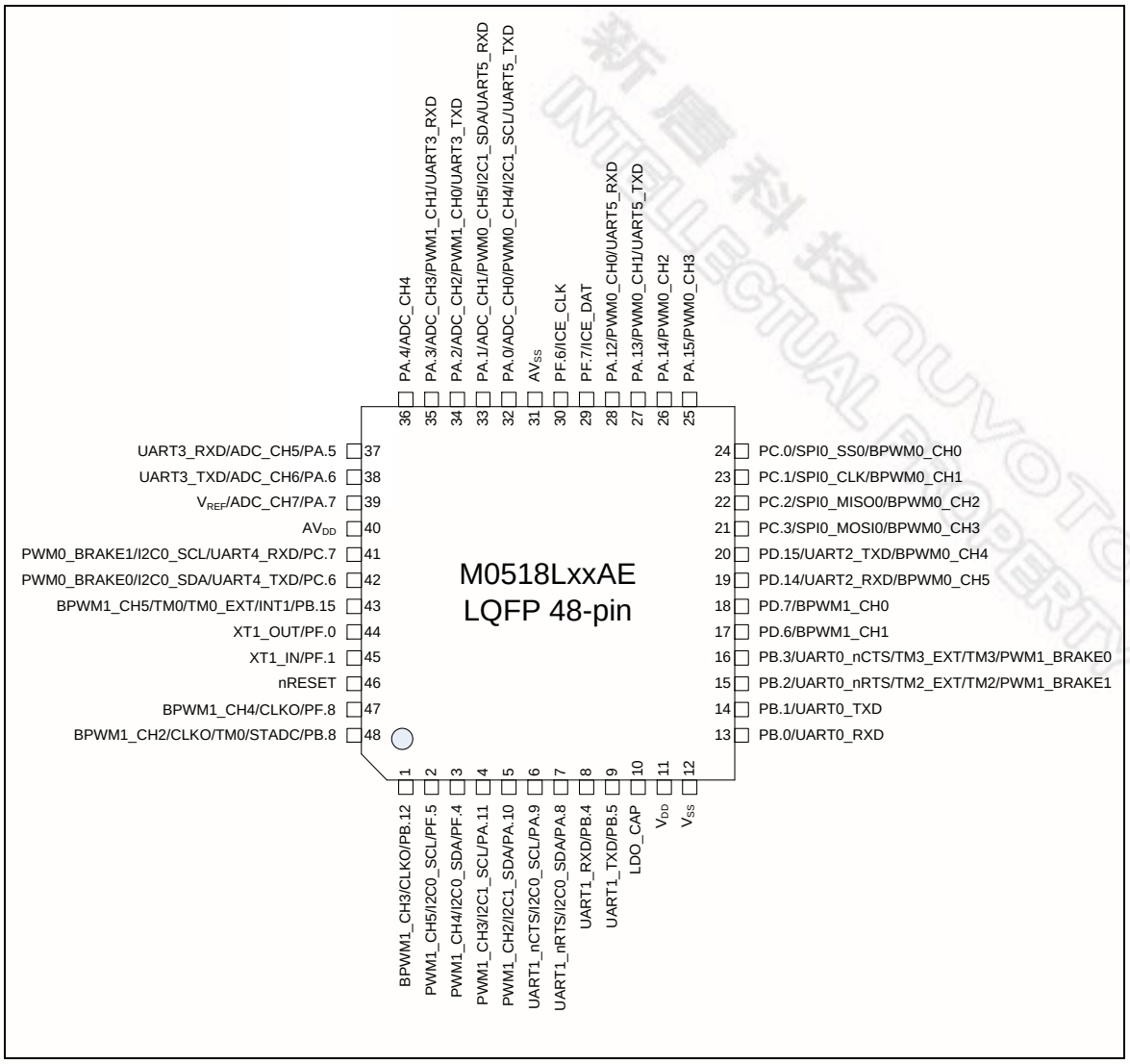


Figure 4-3 NuMicro™ M0518LxxAE LQFP 48-pin Diagram

Pin No.		Pin Name	Pin Type	Description
LQFP 64-pin	LQFP 48-pin			
		PWM0_CH3	I/O	PWM0 CH3 output/Capture input.
38	26	PA.14	I/O	General purpose digital I/O pin.
		PWM0_CH2	I/O	PWM0 CH2 output/Capture input.
39	27	PA.13	I/O	General purpose digital I/O pin.
		PWM0_CH1	I/O	PWM0 CH1 output/Capture input.
		UART5_TXD	O	Data transmitter output pin for UART5.
40	28	PA.12	I/O	General purpose digital I/O pin.
		PWM0_CH0	I/O	PWM0 CH0 output/Capture input.
		UART5_RXD	I	Data receiver input pin for UART5.
41	29	PF.7	I/O	General purpose digital I/O pin.
		ICE_DAT	I/O	Serial wire debugger data pin.
42	30	PF.6	I/O	General purpose digital I/O pin.
		ICE_CLK	I	Serial wire debugger clock pin.
43	31	AV_{SS}	AP	Ground pin for analog circuit.
44	32	PA.0	I/O	General purpose digital I/O pin.
		ADC_CH0	AI	ADC_CH0 analog input.
		PWM0_CH4	I/O	PWM0 CH4 output/Capture input.
		I2C1_SCL	I/O	I^2C1 clock pin.
		UART5_TXD	O	Data transmitter output pin for UART5.
45	33	PA.1	I/O	General purpose digital I/O pin.
		ADC_CH1	AI	ADC_CH1 analog input.
		PWM0_CH5	I/O	PWM0 CH5 output/Capture input.
		I2C1_SDA	I/O	I^2C1 data input/output pin.
		UART5_RXD	I	Data receiver input pin for UART5.
46	34	PA.2	I/O	General purpose digital I/O pin.
		ADC_CH2	AI	ADC_CH2 analog input.
		PWM1_CH0	I/O	PWM1 CH0 output/Capture input.
		UART3_TXD	O	Data transmitter output pin for UART3.
47	35	PA.3	I/O	General purpose digital I/O pin.
		ADC_CH3	AI	ADC_CH3 analog input.
		PWM1_CH1	I/O	PWM1 CH1 output/Capture input.
		UART3_RXD	I	Data receiver input pin for UART3.

6.2.5 System Timer (SysTick)

The Cortex™-M0 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to 0, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock cycle, then decrement on subsequent clocks. When the counter transitions to 0, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is unknown on reset. Software should write to the register to clear it to 0 before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is 0, the timer will be maintained with a current value of 0 after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the "ARM® Cortex™-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

30	14	**SPI0_INT**	SPI0	SPI0 interrupt
31	15	**UART3_INT**	UART3	UART3 interrupt
32	16	**UART4_INT**	UART4	UART4 interrupt
33	17	**UART5_INT**	UART5	UART5 interrupt
34	18	**I2C0_INT**	I^2C0	I^2C0 interrupt
35	19	**I2C1_INT**	I^2C1	I^2C1 interrupt
36	20	**-**	-	Reserved
37	21	**-**	-	Reserved
38	22	**PWM0_INT**	PWM0	PWM0 interrupt
39	23	**PWM1_INT**	PWM1	PWM1 interrupt
40	24	**BPWM0_INT**	BPWM0	BPWM0 interrupt
41	25	**BPWM1_INT**	BPWM1	BPWM1 interrupt
42	26	**BRAKE0_INT**	PWM0	PWM0 brake interrupt
43	27	**BRAKE1_INT**	PWM1	PWM1 brake interrupt
44	28	**PWRWU_INT**	CLKC	Clock controller interrupt for chip wake-up from Power-down state
45	29	**ADC_INT**	ADC	ADC interrupt
46	30	**CKD_INT**	CLKC	Clock detection interrupt
47	31	**-**	-	Reserved

Table 6-3 System Interrupt Map

6.2.6.2 Vector Table

When an interrupt is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For ARMv6-M, the vector table base address is fixed at 0x00000000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Vector Table Word Offset	Description
0	SP_main – The Main stack pointer
Vector Number	Exception Entry Pointer using that Vector Number

Table 6-4 Vector Table Format

6.2.6.3 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

6.2.7 System Control

The Cortex™-M0 status and operating mode control are managed by System Control Registers. Including CPUID, Cortex™-M0 interrupt priority and Cortex™-M0 power management can be controlled through these system control registers.

For more detailed information, please refer to the "ARM® Cortex™-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

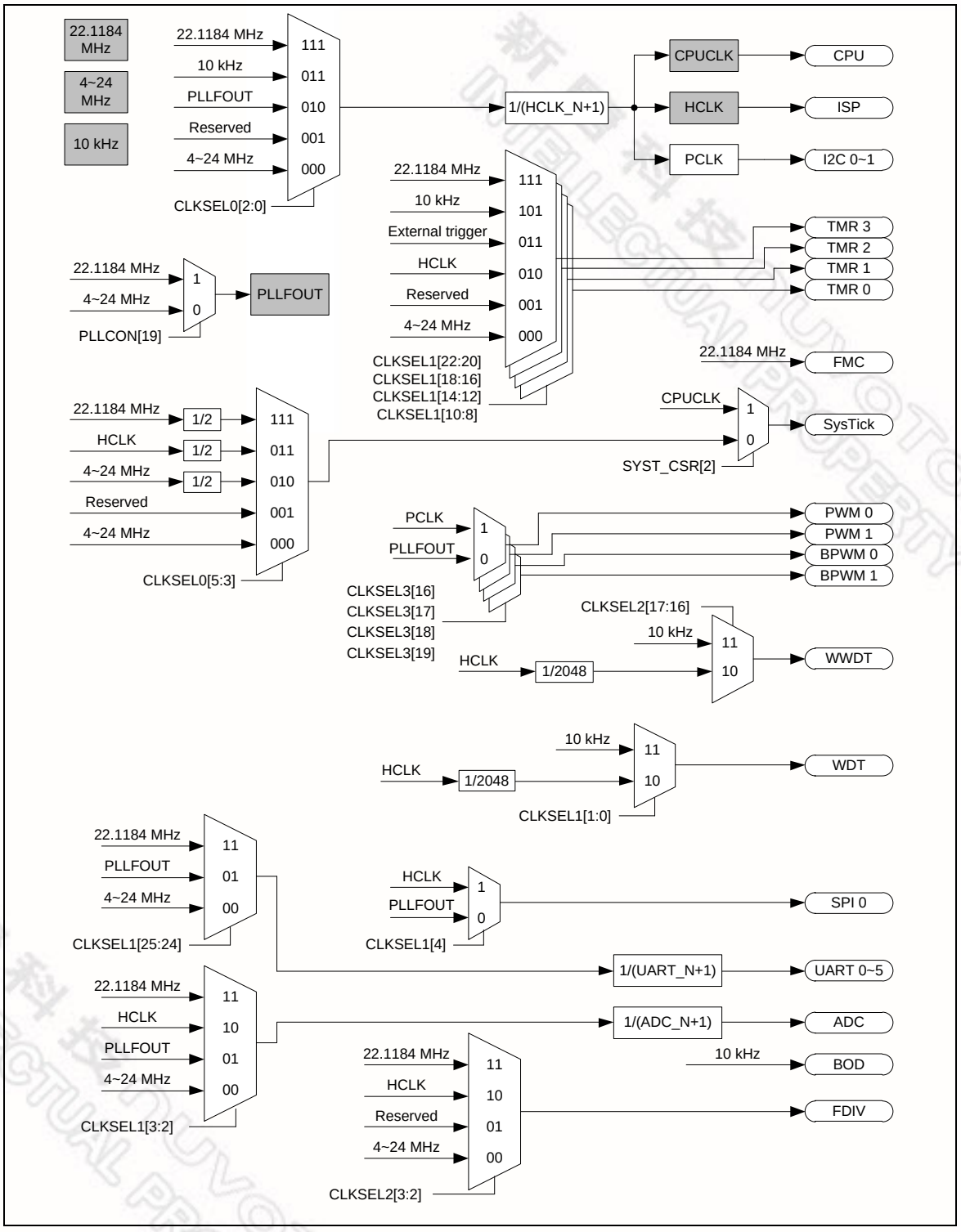


Figure 6-4 Clock Generator Global View Diagram

6.3.2 System Clock and SysTick Clock

The system clock has 4 clock sources which were generated from clock generator block. The

6.3.4 Frequency Divider Output

This device is equipped with a power-of-2 frequency divider which is composed by16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where Fin is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FSEL (FRQDIV[3:0]).

When writing 1 to DIVIDER_EN (FRQDIV[4]), the chained counter starts to count. When writing 0 to DIVIDER_EN (FRQDIV[4]), the chained counter continuously runs till divided clock reaches low state and stay in low state.

If DIVIDER1(FRQDIV[5]) is set to 1, the frequency divider clock (FRQDIV_CLK) will bypass power-of-2 frequency divider. The frequency divider clock will be output to CLKO pin directly.

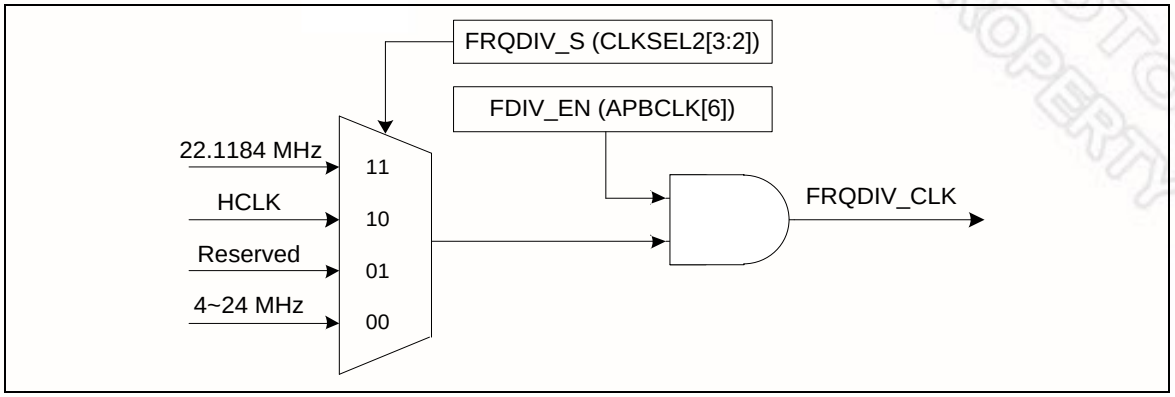


Figure 6-7 Clock Source of Frequency Divider

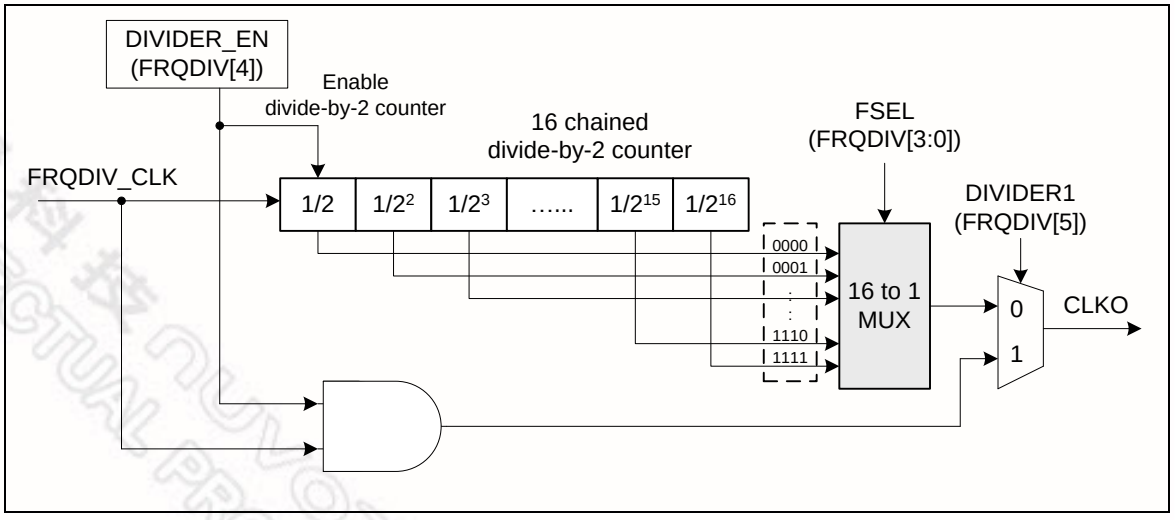


Figure 6-8 Frequency Divider Block Diagram

6.5 General Purpose I/O (GPIO)

6.5.1 Overview

The NuMicro™ M0518 series has up to 56 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 56 pins are arranged in 6 ports named as GPIOA, GPIOB, GPIOC, GPIOD, GPIOE and GPIOF. The GPIOA/B port has the maximum of 16 pins. The GPIOC port has the maximum of 12 pins. The GPIOD port has the maximum of 4 pins. The GPIOE port has the maximum of 1 pin. The GPIOF port has the maximum of 7 pins. Each of the 56 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as input, output, open-drain or Quasi-bidirectional mode. After reset, the I/O mode of all pins are depending on Config0[10] setting. In Quasi-bidirectional mode, I/O pin has a very weak individual pull-up resistor which is about 110~300 KΩ for V_{DD} from 5.0 V to 2.5 V.

6.5.2 Features

- Four I/O modes:
  - Quasi-bidirectional
  - Push-Pull output
  - Open-Drain output
  - Input only with high impendence
- TTL/Schmitt trigger input selectable by GPx_TYPE[15:0] in GPx_MFP[31:16]
- I/O pin configured as interrupt source with edge/level setting
- Configurable default I/O mode of all pins after reset by Config0[10] setting
  - If Config[10] is 0, all GPIO pins in input tri-state mode after chip reset
  - If Config[10] is 1, all GPIO pins in Quasi-bidirectional mode after chip reset
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the pin wake-up function

6.9 Watchdog Timer (WDT)

6.9.1 Overview

The purpose of Watchdog Timer is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

6.9.2 Features

- 18-bit free running up counter for Watchdog Timer time-out interval.
- Selectable time-out interval (2^4 ~ 2^{18}) WDT_CLK cycle and the time-out interval period is 104 ms ~ 26.3168 s if WDT_CLK = 10 kHz.
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports Watchdog Timer reset delay period
  - Selectable it includes (1026、130、18 or 3) * WDT_CLK reset delay period.
- Supports to force Watchdog Timer enabled after chip powered on or reset while CWDTEN (CONFIG0[31] Watchdog Enable) bit is set to 0.
- Supports Watchdog Timer time-out wake-up function only if WDT clock source is selected as 10 kHz

6.13 Serial Peripheral Interface (SPI)

6.13.1 Overview

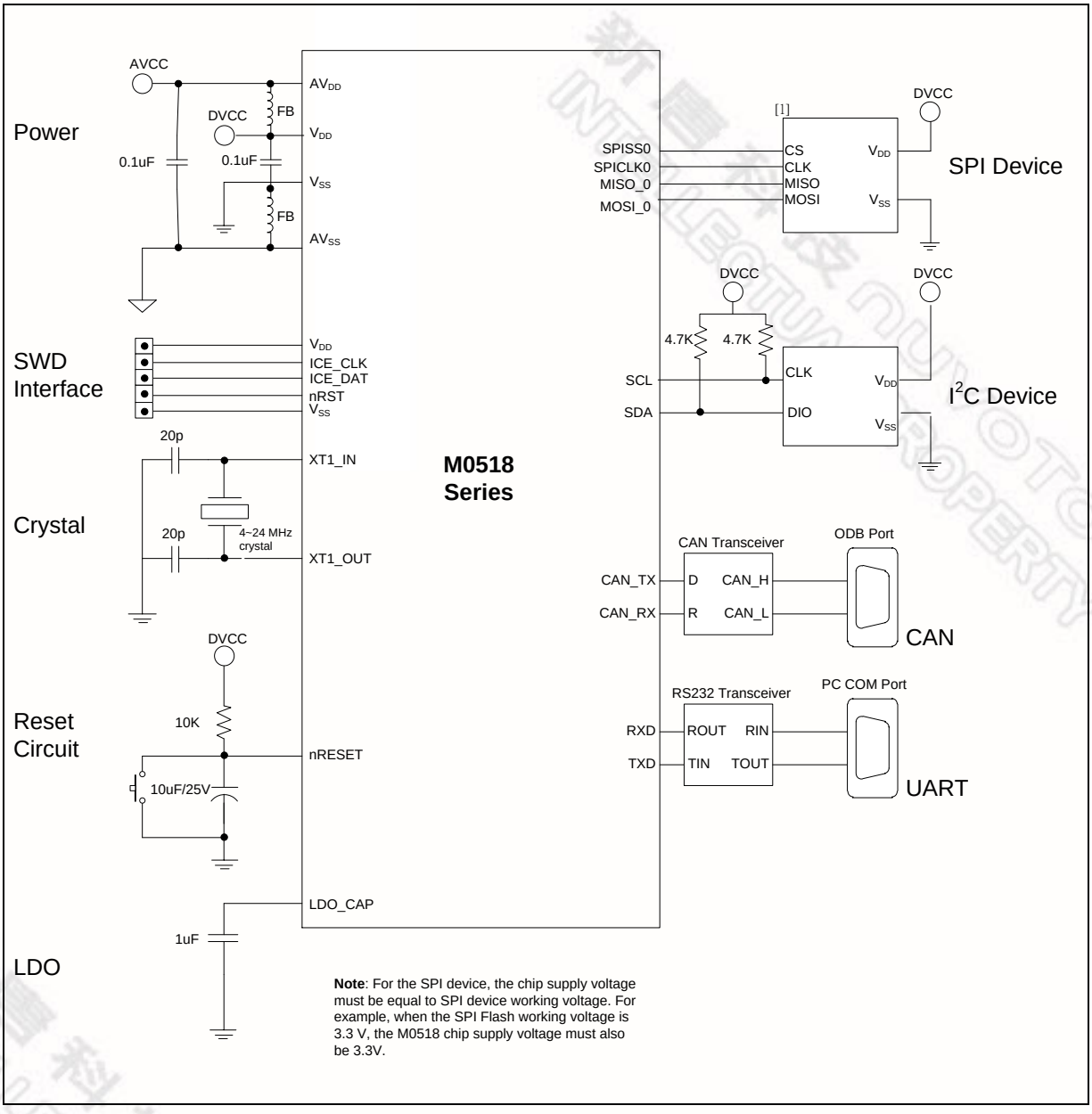
The Serial Peripheral Interface (SPI) is a synchronous serial data communication protocol that operates in full duplex mode. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The NuMicro™ M0518 series contains one set of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. This SPI controller can be configured as a master or a slave device.

The SPI controller supports the variable bus clock function for special applications.

6.13.2 Features

- One set of SPI controller
- Supports Master or Slave mode operation
- Supports Dual I/O Transfer mode
- Configurable bit length of a transaction word from 8 to 32 bits
- Provides separate 8-layer depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Supports the Byte Reorder function
- Supports Byte or Word Suspend mode
- Variable output bus clock frequency in Master mode
- Supports 3-wire, no slave select signal, bi-direction interface

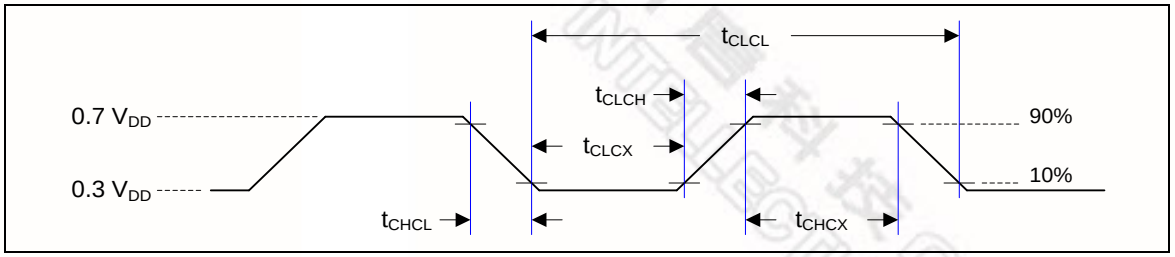
7 APPLICATION CIRCUIT



Note: For the SPI device, the chip supply voltage must be equal to SPI device working voltage. For example, when the SPI Flash working voltage is 3.3 V, the M0518 chip supply voltage must also be 3.3V.

8.3 AC Electrical Characteristics

8.3.1 External 4~24 MHz High Speed Oscillator



Note: Duty cycle is 50%.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
t_{CHCX}	Clock High Time		10	-	-	nS
t_{CLCX}	Clock Low Time		10	-	-	nS
t_{CLCH}	Clock Rise Time		2	-	15	nS
t_{CHCL}	Clock Fall Time		2	-	15	nS

8.3.2 External 4~24 MHz High Speed Crystal

SYMBOL	PARAMETER	CONDITION	MIN.	TYP..	MAX.	UNIT
V_{HXT}	Operation Voltage V_{DD}	-	2.5	-	5.5	V
T_A	Temperature	-	-40	-	105	℃
I_{HXT}	Operating Current	12 MHz at V_{DD} = 5V	-	2	-	mA
		12 MHz at V_{DD} = 3V		0.8		mA
f_{HXT}	Clock Frequency	External crystal	4		24	MHz

8.3.2.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
4 MHz ~ 24 MHz	10~20pF	10~20pF	without

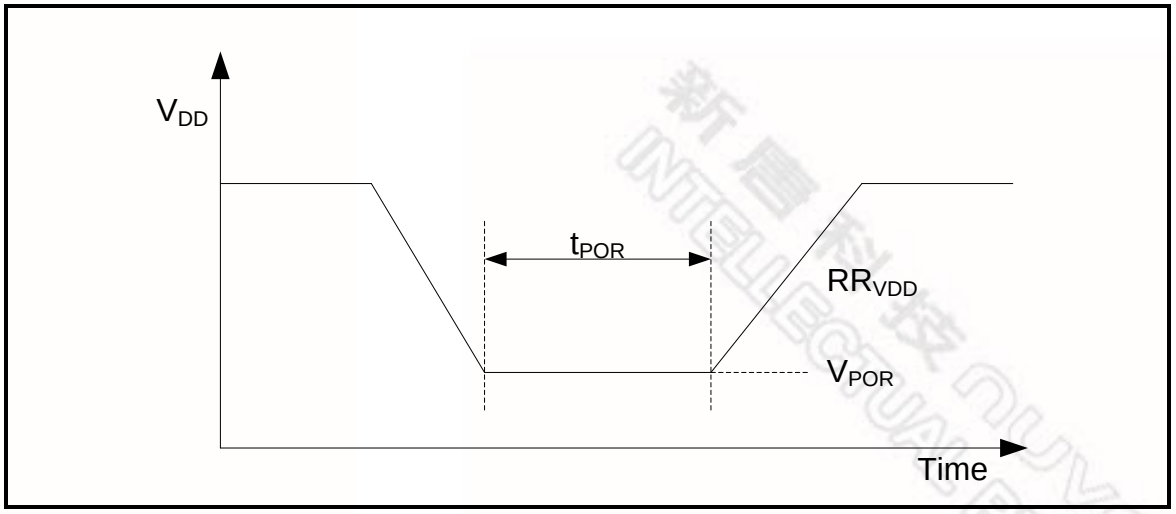


Figure 8-3 Power-up Ramp Condition

8.5 Flash DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{FLA}[2]	Supply Voltage		1.62	1.8	1.98	V[2]
N_{ENDUR}	Endurance		20000	-	-	cycles[1]
T_{RET}	Data Retention	At 85℃	100	-	-	year
T_{ERASE}	Page Erase Time		20	-	-	ms
T_{MER}	Mass Erase Time		40	-	-	ms
T_{PROG}	Program Time		40	-	-	μs

Note:

1. Number of program/erase cycles.

2. V_{FLA} is source from chip LDO output voltage.

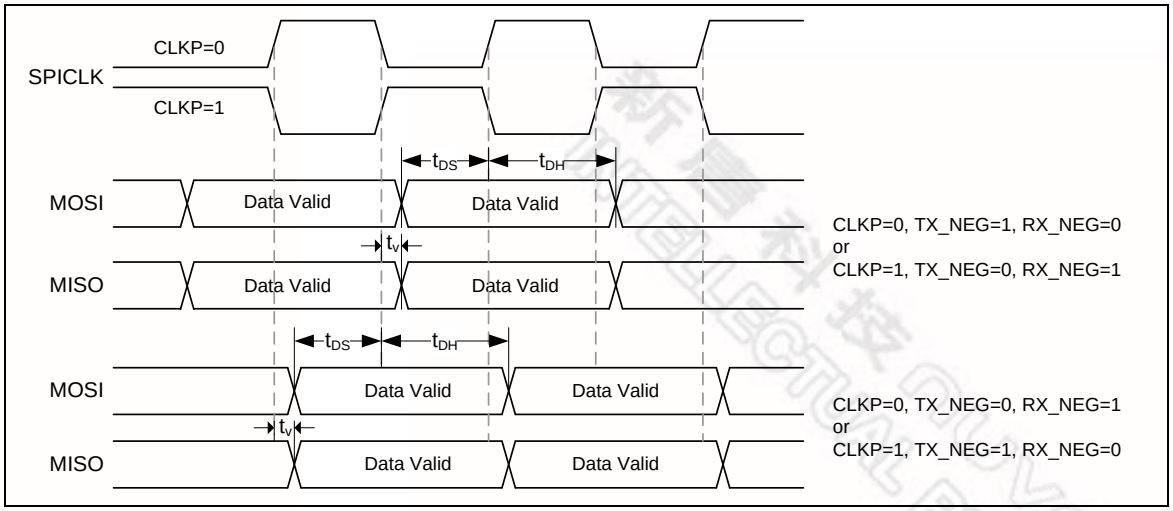


Figure 8-6 SPI Slave Mode Timing Diagram