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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVR, POR, PWM, WDT
Number of I/O	56
Program Memory Size	68KB (68K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/m0518sd2ae

2 FEATURES

- ARM® Cortex™-M0 core
  - Runs up to 50 MHz
  - One 24-bit system timer
  - Supports low power sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Built-in LDO for wide operating voltage ranged from 2.5 V to 5.5 V
- Flash Memory
  - 36K/68K bytes Flash for program code
  - Configurable Flash memory for data memory (Data Flash), 4 KB flash for ISP loader
  - Supports In-System-Program (ISP) and In-Application-Program (IAP) application code update
  - 512 byte page erase for flash
  - Supports 2-wired ICP update through SWD/ICE interface
  - Supports fast parallel programming mode by external programmer
- SRAM Memory
  - 8KB SRAM
- Clock Control
  - Flexible selection for different applications
  - Built-in 22.1184 MHz high speed oscillator for system operation
    - Trimmed to ±1 % at +25 ℃ and V_{DD} = 5 V
    - Trimmed to ±2 % at -40 ℃ ~ +105 ℃ and V_{DD} = 2.5 V ~ 5.5 V
  - Built-in 10 kHz low speed oscillator for Watchdog Timer and Wake-up operation
  - Supports one PLL output frequency up to 200 MHz, BPWM/PWM clock frequency up to 100 MHz, and System operation frequency up to 50 MHz
  - External 4~24 MHz high speed crystal input for precise timing operation
- GPIO
  - Four I/O modes:
    - Quasi-bidirectional
    - Push-pull output
    - Open-drain output
    - Input only with high impendence
  - TTL/Schmitt trigger input selectable
  - I/O pin configured as interrupt source with edge/level setting
- Timer
  - Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit prescale counter
  - Independent clock source for each timer
  - Provides one-shot, periodic, toggle and continuous counting operation modes
  - Supports event counting function
  - Supports input capture function
- Watchdog Timer
  - Multiple clock sources
    - System clock (HCLK)
    - Internal 10 kHz oscillator (LIRC)
  - 8 selectable time-out period from 1.6 ms ~ 26.0 sec (depending on clock source)
  - Wake-up from Power-down or Idle mode
  - Interrupt or reset selectable on watchdog time-out
- Window Watchdog Timer
  - 6-bit down counter with 11-bit prescale for wide range window selected
- BPWM/Capture
  - Supports maximum clock frequency up to 100MHz
  - Supports up to two BPWM modules, each module provides one 16-bit timer and 6 output

4.2 NuMicro™ M0518 Series Selection Guide

Part Number	APROM (KB)	RAM (KB)	Data Flash (KB)	ISP ROM (KB)	I/O	Timer (32-Bit)	Connectivity				PWM (16-Bit)	ADC (12-Bit)	ISP/ICP/IAP	Package
							UART	SPI	I^2C	LIN				
M0518LC2AE	36	8	Configurable	4	42	4	6	1	2	3	24	8 ch	√	LQFP48
M0518LD2AE	68	8	Configurable	4	42	4	6	1	2	3	24	8 ch	√	LQFP48
M0518SC2AE	36	8	Configurable	4	56	4	6	1	2	3	24	8 ch	√	LQFP64
M0518SD2AE	68	8	Configurable	4	56	4	6	1	2	3	24	8 ch	√	LQFP64

5 BLOCK DIAGRAM

5.1 NuMicro™ M0518 Block Diagram

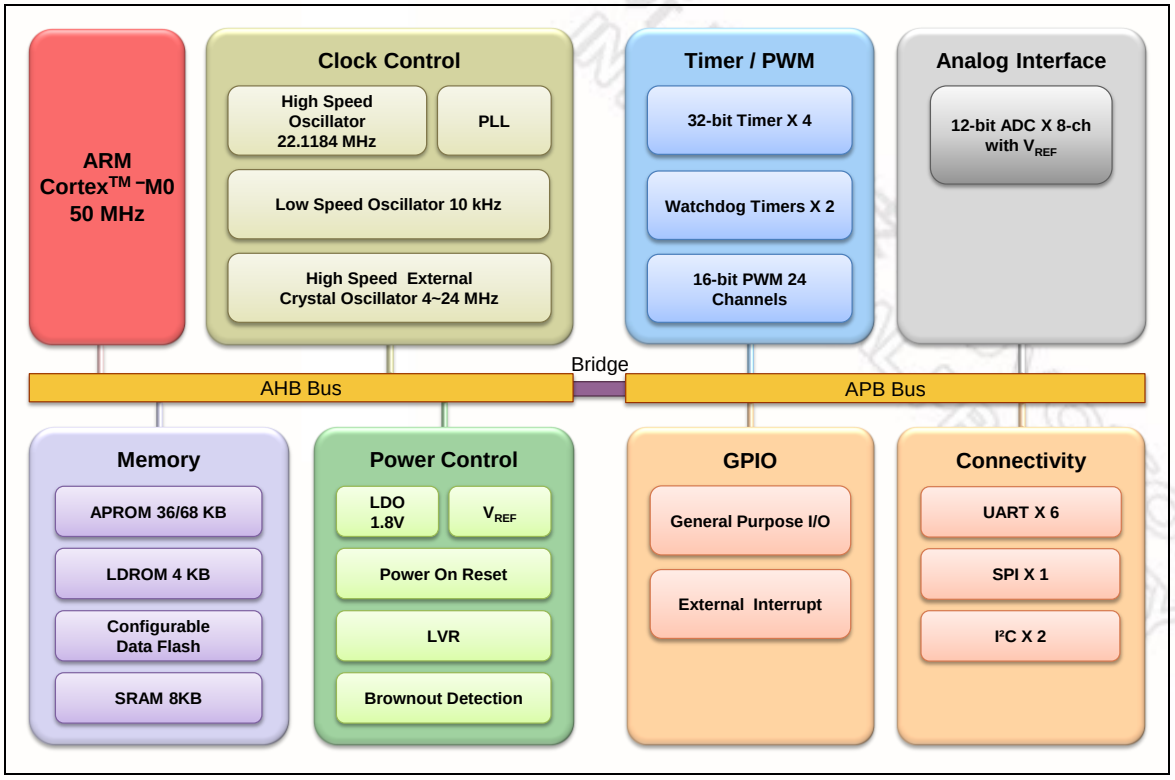


Figure 5-1 NuMicro™ M0518 Block Diagram

6.2.3 System Power Distribution

In this chip, the power distribution is divided into three segments.

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides a fixed 1.8 V power for digital operation and I/O pins.

The outputs of internal voltage regulators, LDO, require an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level with the digital power (V_{DD}). Figure 6-2 shows the NuMicro™ M0518 power distribution.

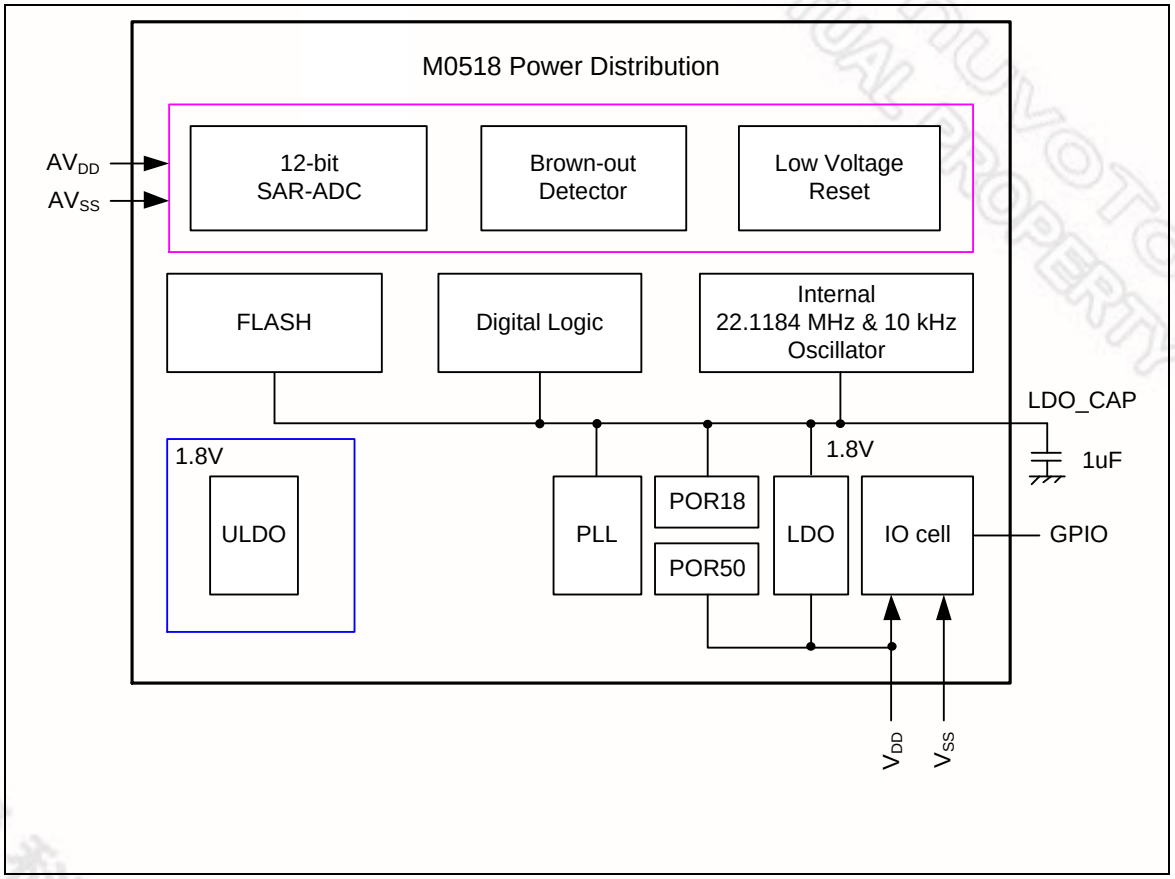


Figure 6-2 NuMicro™ M0518 Power Distribution Diagram

6.2.5 System Timer (SysTick)

The Cortex™-M0 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to 0, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock cycle, then decrement on subsequent clocks. When the counter transitions to 0, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is unknown on reset. Software should write to the register to clear it to 0 before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is 0, the timer will be maintained with a current value of 0 after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the "ARM® Cortex™-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

6.2.6.1 Exception Model and System Interrupt Map

The following table lists the exception model supported by NuMicro™ M0518 series. Software can set four levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as “0” and the lowest priority is denoted as “3”. The default priority of all the user-configurable interrupts is “0”. Note that priority “0” is treated as the fourth priority on the system, after three system exceptions “Reset”, “NMI” and “Hard Fault”.

Exception Name	Vector Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCall	11	Configurable
Reserved	12 ~ 13	Reserved
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	Configurable

Table 6-2 Exception Model

Vector Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Source Module	Interrupt Description
1 ~ 15	-	**-**	-	System exceptions
16	0	**BOD_INT**	Brown-out	Brown-out low voltage detected interrupt
17	1	**WDT_INT**	WDT	Watchdog Timer interrupt
18	2	**EINT0**	GPIO	External signal interrupt from PB.14 pin
19	3	**EINT1**	GPIO	External signal interrupt from PB.15 pin
20	4	**GPAB_INT**	GPIO	External signal interrupt from PA[15:0]/PB[13:0]
21	5	**GPCDEF_INT**	GPIO	External interrupt from PC[15:0]/PD[15:0]/PE[15:0]/PF[8:0]
22	6	**-**	-	Reserved
23	7	**-**	-	Reserved
24	8	**TMR0_INT**	TMR0	Timer 0 interrupt
25	9	**TMR1_INT**	TMR1	Timer 1 interrupt
26	10	**TMR2_INT**	TMR2	Timer 2 interrupt
27	11	**TMR3_INT**	TMR3	Timer 3 interrupt
28	12	**UART02_INT**	UART0/2	UART0 and UART2 interrupt
29	13	**UART1_INT**	UART1	UART1 interrupt

clock source switch depends on the register HCLK_S (CLKSEL0[2:0]). The block diagram is shown in Figure 6-5.

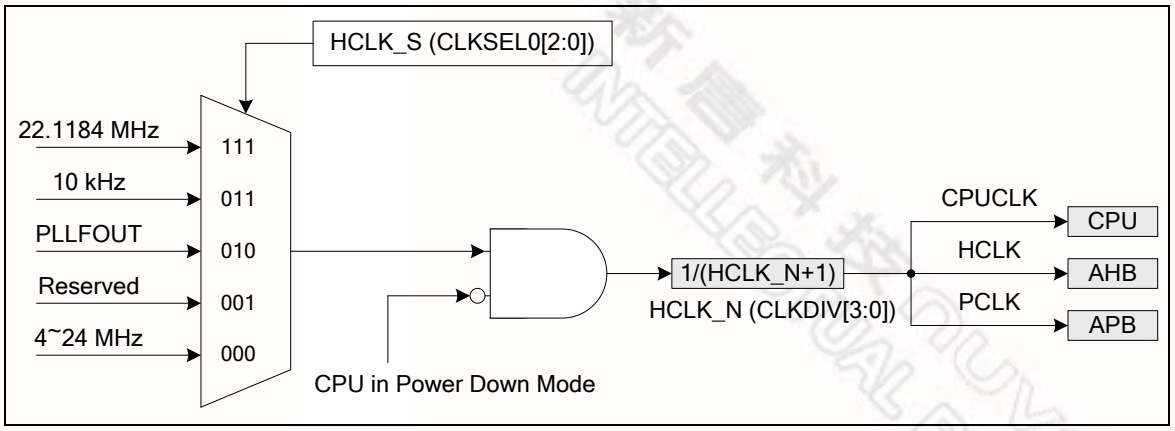


Figure 6-5 System Clock Block Diagram

The clock source of SysTick in Cortex™-M0 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 4 clock sources. The clock source switch depends on the setting of the register STCLK_S (CLKSEL0[5:3]). The block diagram is shown in Figure 6-6.

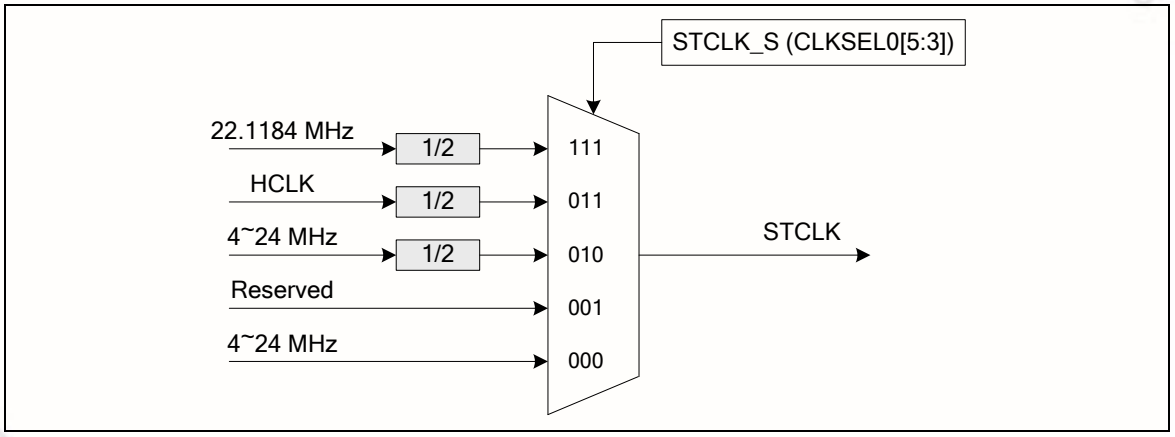


Figure 6-6 SysTick Clock Control Block Diagram

6.4 Flash Memory Controller (FMC)

6.4.1 Overview

The NuMicro™ M0518 series has 68/36K bytes on-chip embedded Flash for application program memory (APROM) that can be updated through ISP procedure. The In-System-Programming (ISP) function enables user to update program memory when chip is soldered on PCB. After chip is powered on, Cortex™-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in CONFIG0. By the way, the NuMicro™ M0518 series also provides additional Data Flash for user to store some application dependent data.

The NuMicro™ M0518 supports another flexible feature: configurable Data Flash size. The Data Flash size is decided by Data Flash variable size enable (DFVSEN), Data Flash enable (DFEN) in Config0 and Data Flash base address (DFBADR) in Config1. When DFVSEN is set to 1, the Data Flash size is fixed at 4K and the address is started from 0x0001_f000, and the APROM size is become 64/32K. When DFVSEN is set to 0 and DFEN is set to 1, the Data Flash size is zero and the APROM size is 68/36K bytes. When DFVSEN is set to 0 and DFEN is set to 0, the APROM and Data Flash share 68/36K bytes continuous address and the start address of Data Flash is defined by (DFBADR) in Config1.

6.4.2 Features

- Runs up to 50 MHz with zero wait cycle for continuous address read access
- All embedded flash memory supports 512 bytes page erase
- 68/36 KB application program memory (APROM)
- 4KB In-System-Programming (ISP) loader program memory (LDROM)
- Configurable Data Flash size
- 512 bytes page erase unit
- Supports In-Application-Programming (IAP) to switch code between APROM and LDROM without reset
- In-System-Programming (ISP) to update on-chip Flash

6.5 General Purpose I/O (GPIO)

6.5.1 Overview

The NuMicro™ M0518 series has up to 56 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 56 pins are arranged in 6 ports named as GPIOA, GPIOB, GPIOC, GPIOD, GPIOE and GPIOF. The GPIOA/B port has the maximum of 16 pins. The GPIOC port has the maximum of 12 pins. The GPIOD port has the maximum of 4 pins. The GPIOE port has the maximum of 1 pin. The GPIOF port has the maximum of 7 pins. Each of the 56 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as input, output, open-drain or Quasi-bidirectional mode. After reset, the I/O mode of all pins are depending on Config0[10] setting. In Quasi-bidirectional mode, I/O pin has a very weak individual pull-up resistor which is about 110~300 KΩ for V_{DD} from 5.0 V to 2.5 V.

6.5.2 Features

- Four I/O modes:
  - Quasi-bidirectional
  - Push-Pull output
  - Open-Drain output
  - Input only with high impendence
- TTL/Schmitt trigger input selectable by GPx_TYPE[15:0] in GPx_MFP[31:16]
- I/O pin configured as interrupt source with edge/level setting
- Configurable default I/O mode of all pins after reset by Config0[10] setting
  - If Config[10] is 0, all GPIO pins in input tri-state mode after chip reset
  - If Config[10] is 1, all GPIO pins in Quasi-bidirectional mode after chip reset
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the pin wake-up function

6.7 PWM Generator and Capture Timer (PWM)

6.7.1 Overview

The M0518 provides two PWM generators – PWM0 and PWM1. Each PWM supports 6 channels of PWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit PWM counter with 16-bit comparator. The PWM counter supports up, down and up-down counter types. PWM uses the comparator compared with counter to generate events. These events are used to generate PWM pulse, interrupt and trigger signal for ADC to start conversion.

The PWM generator supports two standard PWM output modes: Independent mode and Complementary mode, which have difference architecture. In Complementary mode, there are two comparators to generate various PWM pulse with 12-bit dead-time generator. For PWM output control unit, it supports polarity output, independent pin mask, tri-state output enable and brake functions.

The PWM generator also supports input capture function to latch PWM counter value to the corresponding register when input channel has a rising transition, falling transition or both transition is happened.

6.7.2 Features

6.7.2.1 PWM function features

- Supports maximum clock frequency up to100 MHz
- Supports up to two PWM modules, each module provides 6 output channels
- Supports independent mode for PWM output/Capture input channel
- Supports complementary mode for 3 complementary paired PWM output channel
  - Dead-time insertion with 12-bit resolution
  - Two compared values during one period
- Supports 12-bit pre-scalar from 1 to 4096
- Supports 16-bit resolution PWM counter, each module provides 3 PWM counters
  - Up, down and up/down counter operation type
- Supports mask function and tri-state enable for each PWM pin
- Supports brake function
  - Brake source from pin and system safety events (clock failed, Brown-out detection and CPU lockup)
  - Noise filter for brake source from pin
  - Edge detect brake source to control brake state until brake interrupt cleared
  - Level detect brake source to auto recover function after brake condition removed
- Supports interrupt on the following events:
  - PWM counter match zero, period value or compared value
  - Brake condition happened
- Supports trigger ADC on the following events:

- PWM counter match zero, period value or compared value

6.7.2.2 Capture Function Features

- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option

6.7.2.3 Compare table

Feature	**PWM**	**BPWM**
Counter number	2 channels share 1 timer, total 6 timers	6 channels share 1 timer, total 1 timer
Complementary mode	V	X
Dead-time function	V	X
Brake function	V	X
Capture reload	2 channels reload 1 timer	6 channels reload 1 timer

Table 6-5 PWM and BPWM Features Different Table

6.9 Watchdog Timer (WDT)

6.9.1 Overview

The purpose of Watchdog Timer is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

6.9.2 Features

- 18-bit free running up counter for Watchdog Timer time-out interval.
- Selectable time-out interval (2^4 ~ 2^{18}) WDT_CLK cycle and the time-out interval period is 104 ms ~ 26.3168 s if WDT_CLK = 10 kHz.
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports Watchdog Timer reset delay period
  - Selectable it includes (1026、130、18 or 3) * WDT_CLK reset delay period.
- Supports to force Watchdog Timer enabled after chip powered on or reset while CWDTEN (CONFIG0[31] Watchdog Enable) bit is set to 0.
- Supports Watchdog Timer time-out wake-up function only if WDT clock source is selected as 10 kHz

6.11 UART Interface Controller (UART)

6.11.1 Overview

The NuMicro™ M0518 series provides up to six channels of Universal Asynchronous Receiver/Transmitters (UART). UART0/UART1/UART2 supports 16 bytes entry FIFO and UART3/UART4/UART5 support 1 byte buffer for data payload. Besides, only UART0 and UART1 support the flow control function. The UART Controller performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART controller also supports IrDA SIR Function. UART0/UART1 provides RS-485 function mode. UART0/UART1/UART2 provides LIN master/slave function.

6.11.2 Features

- Full duplex, asynchronous communications
- Separates receive / transmit 16/16 bytes (UART0/UART1/UART2 support) entry FIFO and 1/1 bytes buffer for data payloads (UART3/UART4/UART5 support)
- Supports hardware auto-flow control function (CTS, RTS) and programmable RTS flow control trigger level (UART0/UART1 support).
- Programmable receiver buffer trigger level
- Supports programmable baud-rate generator for each channel individually
- Supports CTS wake-up function (UART0/UART1 support)
- Supports 7-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UA_TOR [15:8]) register
- Supports break error, frame error, parity error and receive / transmit buffer overflow detect function
- Fully programmable serial-interface characteristics
  - Programmable data bit length, 5-, 6-, 7-, 8-bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit length, 1, 1.5, or 2 stop bit generation
- IrDA SIR function mode
  - Supports 3/16-bit duration for normal mode
- LIN function mode (UART0/UART1/UART2 support)
  - Supports LIN master/slave mode
  - Supports programmable break generation function for transmitter
  - Supports break detect function for receiver
- RS-485 function mode. (UART0/UART1 support)
  - Supports RS-485 9-bit mode
  - Supports hardware or software direct enable control provided by RTS pin.

6.12 I2C Serial Interface Controller (I2C)

6.12.1 Overview

I^2C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I^2C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

6.12.2 Features

The I^2C bus uses two wires (I2Cn_SDA and I2Cn_SCL) to transfer information between devices connected to the bus. The main features of the I^2C bus include:

- Supports up to two I^2C serial interface controller
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allow devices with different bit rates to communicate via one serial bus
- Built-in a 14-bit time-out counter requesting the I^2C interrupt if the I^2C bus hangs up and timer-out counter overflows.
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function

8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN.	MAX	UNIT
DC Power Supply	V_{DD}–V_{SS}	-0.3	+7.0	V
Input Voltage	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	T_A	-40	+105	°C
Storage Temperature	T_{ST}	-55	+150	°C
Maximum Current into V_{DD}		-	120	mA
Maximum Current out of V_{SS}			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Source Current PA, PB, PC, PD, PE, PF (Quasi-bidirectional Mode)	I_{SR11}	-300	-400		μA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR12}	-50	-80		μA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR12}	-40	-73		μA	V_{DD} = 2.5V, V_S = 2.0V
Source Current PA, PB, PC, PD, PE, PF (Push-pull Mode)	I_{SR21}	-20	-26		mA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR22}	-3	-5.2		mA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR22}	-2.5	-5		mA	V_{DD} = 2.5V, V_S = 2.0V
Sink Current PA, PB, PC, PD, PE, PF (Quasi-bidirectional and Push-pull Mode)	I_{SK1}	10	17		mA	V_{DD} = 4.5V, V_S = 0.45V
	I_{SK1}	6	11		mA	V_{DD} = 2.7V, V_S = 0.45V
	I_{SK1}	5	10		mA	V_{DD} = 2.5V, V_S = 0.45V

Note:

1. nRESET pin is a Schmitt trigger input.
2. Crystal Input is a CMOS input.
3. Pins of PA, PB, PC, PD, PE and PF can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD} = 5.5 V, the transition current reaches its maximum value when V_{IN} approximates to 2 V.

8.4 Analog Characteristics

8.4.1 12-bit SARADC Specification

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
-	Resolution	-	-	12	Bit
DNL	Differential nonlinearity error	-	-1~2	-1~4	LSB
INL	Integral nonlinearity error	-	±2	±4	LSB
E_O	Offset error	-	3	-	LSB
E_G	Gain error (Transfer gain)	-	-3	-	-
E_A	Absolute Error	-	4	-	LSB
-	Monotonic	Guaranteed			
F_{ADC}	ADC clock frequency (AV_{DD} = 4.5V~5.5V)	-	-	21	MHz
F_S	Sample rate (F_{ADC}/T_{CONV})	-	-	1000	kSPS
T_{ACQ}	Acquisition Time (Sample Stage)	2~9			$1/F_{ADC}$
T_{CONV}	Total Conversion Time	16~23			$1/F_{ADC}$
V_{DDA}	Supplt Current	3	-	5.5	V
I_{DDA}	Supply current (Avg.)		2.9		mA
V_{IN}	Input voltage	0	-	AV_{DD}	V
C_{IN}	Input Capacitance		6		pF
R_{IN}	Input Load		6.5		kΩ

8.6 I2C Dynamic Characteristics

SYMBOL	PARAMETER	STANDARD MODE[1][2]		FAST MODE[1][2]		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{LOW}	SCL low period					uS
t_{HIGH}	SCL high period					uS
$t_{SU;\ STA}$	Repeated START condition setup time					uS
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	uS
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	uS
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	uS
$t_{SU;DAT}$	Data setup time	250	-	100	-	nS
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	uS
t_r	SCL/SDA rise time	-	1000	20+0.1Cb	300	nS
t_f	SCL/SDA fall time	-	300	-	300	nS
C_b	Capacitive load for each bus line	-	400	-	400	pF

Note:

1. Guaranteed by design, not tested in production.

2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I2C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I2C frequency.

3. I2C controller must be retriggered immediately at slave mode after receiving STOP condition.

4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

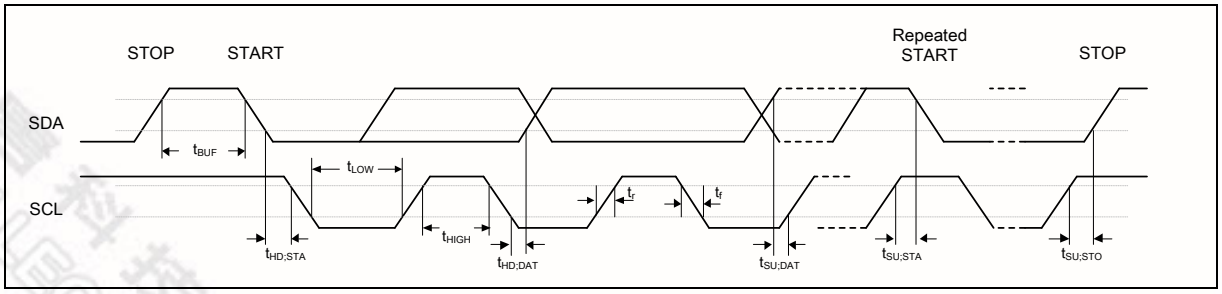


Figure 8-4 I2C Timing Diagram

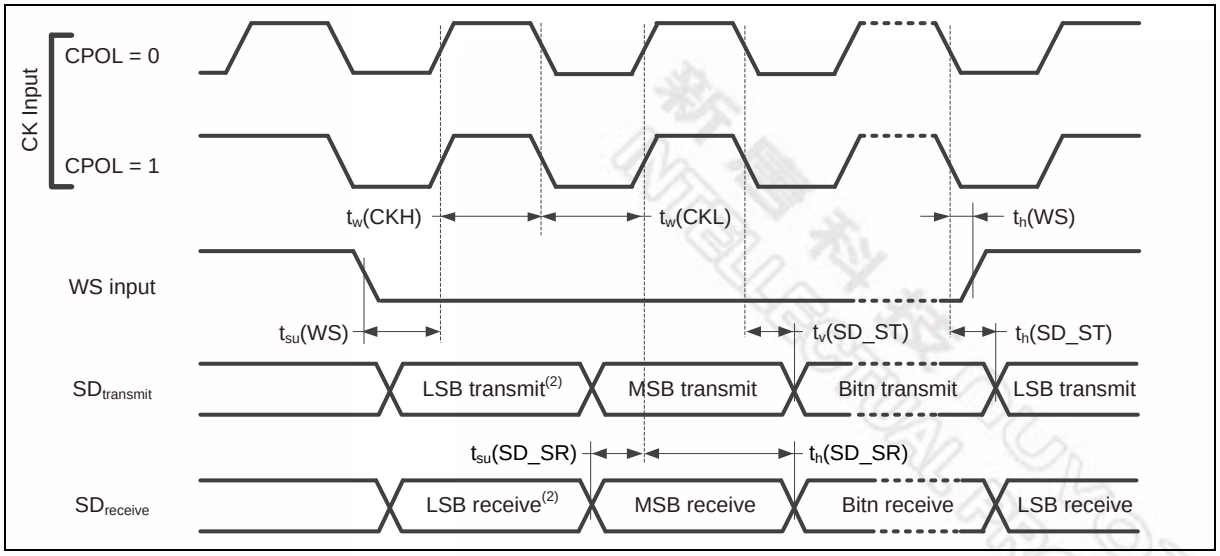
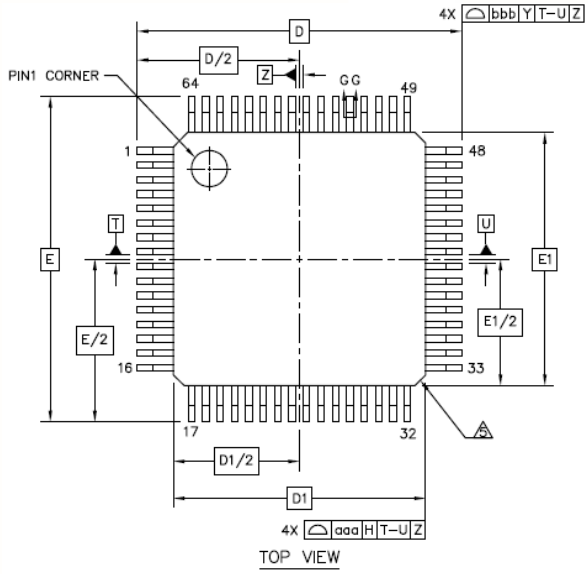


Figure 8-8 I2S Slave Mode Timing Diagram

9 ACKAGE DIMENSIONS

9.1 64-pin LQFP (7x7x1.4 mm footprint 2.0 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05