STMicroelectronics - STM32L162RET6TR Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 21x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l162ret6tr

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32L162xE ultra-low-power ARM® Cortex®-M3 based microcontroller product line. STM32L162xE devices are microcontrollers with a Flash memory density of 512 Kbytes.

The ultra-low-power STM32L162xE family includes devices in 4 different package types: from 64 pins to 144 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the ultra-low-power STM32L162xE microcontroller family suitable for a wide range of applications:

- Medical and handheld equipment
- Application control and user interface
- PC peripherals, gaming, GPS and sport equipment
- Alarm systems, wired and wireless sensors, video intercom
- Utility metering

This STM32L162xE datasheet should be read in conjunction with the STM32L1xxxx reference manual (RM0038). The application note “Getting started with STM32L1xxxx hardware development” (AN3216) gives a hardware implementation overview. Both documents are available from the STMicroelectronics website *www.st.com*.

For information on the ARM® Cortex®-M3 core please refer to the ARM® Cortex®-M3 technical reference manual, available from the www.arm.com website. *Figure 1* shows the general block diagram of the device family.

The memory protection unit (MPU) improves system reliability by defining the memory attributes (such as read/write access permissions) for different memory regions. It provides up to eight different regions and an optional predefined background region.

Owing to its embedded ARM core, the STM32L162xE devices are compatible with all ARM tools and software.

Nested vectored interrupt controller (NVIC)

The ultra-low-power STM32L162xE devices embed a nested vectored interrupt controller able to handle up to 56 maskable interrupt channels (not including the 16 interrupt lines of ARM® Cortex®-M3) and 16 priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving*, higher-priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.3 Reset and supply management

3.3.1 Power supply schemes

- V_{DD} = 1.65 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 1.65 to 3.6 V: external analog power supplies for ADC, reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 1.8 V when the ADC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.

3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR) that can be coupled with a brownout reset (BOR) circuitry.

The device exists in two versions:

- The version with BOR activated at power-on operates between 1.8 V and 3.6 V.
- The other version without BOR operates between 1.65 V and 3.6 V.

After the V_{DD} threshold is reached (1.65 V or 1.8 V depending on the BOR which is active or not at power-on), the option byte loading process starts, either to confirm or modify default thresholds, or to disable the BOR permanently: in this case, the V_{DD} min value becomes 1.65 V (whatever the version, BOR active or not, at power-on).

When BOR is active at power-on, it ensures proper operation starting from 1.8 V whatever the power ramp-up phase before it reaches 1.8 V. When BOR is not active at power-up, the

Table 8. STM32L162xE pin definitions (continued)

Pins				Pin name	Pin Type(1)	I / O structure	Main function(2) (after reset)	Pin functions	
LQFP144	LQFP100	LQFP64	WLCSP104					Alternate functions	Additional functions
112	79	52	C2	PC11	I/O	FT	PC11	SPI3_MISO/USART3_RX/ UART4_RX/ LCD_SEG29/LCD_SEG41 /LCD_COM5	-
113	80	53	B2	PC12	I/O	FT	PC12	SPI3_MOSI/I2S3_SD/ USART3_CK/ UART5_TX/LCD_SEG30/ LCD_SEG42/ LCD_COM6	-
114	81	-	A2	PD0	I/O	FT	PD0	TIM9_CH1/SPI2_NSS/ I2S2_WS	-
115	82	-	D4	PD1	I/O	FT	PD1	SPI2_SCK/I2S2_CK	-
116	83	54	C3	PD2	I/O	FT	PD2	TIM3_ETR/UART5_RX/ LCD_SEG31/ LCD_SEG43/LCD_COM7	-
117	84	-	C4	PD3	I/O	FT	PD3	SPI2_MISO/USART2_CTS	-
118	85	-	A3	PD4	I/O	FT	PD4	SPI2_MOSI/I2S2_SD/ USART2_RTS	-
119	86	-	B3	PD5	I/O	FT	PD5	USART2_TX	-
120	-	-	-	V_{SS_10}	S	-	V_{SS_10}	-	-
121	-	-	-	V_{DD_10}	S	-	V_{DD_10}	-	-
122	87	-	B4	PD6	I/O	FT	PD6	USART2_RX	-
123	88	-	A4	PD7	I/O	FT	PD7	TIM9_CH2/USART2_CK	-
124	-	-	-	PG9	I/O	FT	PG9	-	-
125	-	-	-	PG10	I/O	FT	PG10	-	-
126	-	-	-	PG11	I/O	FT	PG11	-	-
127	-	-	-	PG12	I/O	FT	PG12	-	-
128	-	-	-	PG13	I/O	FT	PG13	-	-
129	-	-	-	PG14	I/O	FT	PG14	-	-
130	-	-	-	V_{SS_11}	S	-	V_{SS_11}	-	-
131	-	-	-	V_{DD_11}	S	-	V_{DD_11}	-	-
132	-	-	-	PG15	I/O	FT	PG15	-	-

Table 9. Alternate function input/output (continued)

Port name	Digital alternate function number													
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFIO6	AFIO7	AFIO8	..	AFIO11	..	AFIO14	AFIO15
	Alternate function													
	SYSTEM	TIM2	TIM3/4/5	TIM9/10/11	I2C1/2	SPI1/2	SPI3	USART1/2/3	UART4/5	-	LCD	-	CPRI	SYSTEM
PB9	-	-	TIM4_CH4	TIM11_CH1	I2C1_SDA	-	-	-	-	-	COM3	-	-	EVENT OUT
PB10	-	TIM2_CH3	-	-	I2C2_SCL	-	-	USART3_TX	-	-	SEG10	-	-	EVENT OUT
PB11	-	TIM2_CH4	-	-	I2C2_SDA	-	-	USART3_RX	-	-	SEG11	-	-	EVENT OUT
PB12	-	-	-	TIM10_CH1	I2C2_SMBA	SPI2_NSS I2S2_WS	-	USART3_CK	-	-	SEG12	-	-	EVENT OUT
PB13	-	-	-	TIM9_CH1	-	SPI2_SCK I2S2_CK	-	USART3_CTS	-	-	SEG13	-	-	EVENT OUT
PB14	-	-	-	TIM9_CH2	-	SPI2_MISO	-	USART3_RTS	-	-	SEG14	-	-	EVENT OUT
PB15	-	-	-	TIM11_CH1	-	SPI2_MOSI I2S2_SD	-	-	-	-	SEG15	-	-	EVENT OUT
PC0	-	-	-	-	-	-	-	-	-	-	SEG18	-	TIMx_IC1	EVENT OUT
PC1	-	-	-	-	-	-	-	-	-	-	SEG19	-	TIMx_IC2	EVENT OUT
PC2	-	-	-	-	-	-	-	-	-	-	SEG20	-	TIMx_IC3	EVENT OUT
PC3	-	-	-	-	-	-	-	-	-	-	SEG21	-	TIMx_IC4	EVENT OUT
PC4	-	-	-	-	-	-	-	-	-	-	SEG22	-	TIMx_IC1	EVENT OUT
PC5	-	-	-	-	-	-	-	-	-	-	SEG23	-	TIMx_IC2	EVENT OUT
PC6	-	-	TIM3_CH1	-	-	I2S2_MCK	-	-	-	-	SEG24	-	TIMx_IC3	EVENT OUT

Table 9. Alternate function input/output (continued)

Port name	Digital alternate function number													
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFIO6	AFIO7	AFIO8	..	AFIO11	..	AFIO14	AFIO15
	Alternate function													
	SYSTEM	TIM2	TIM3/4/5	TIM9/10/11	I2C1/2	SPI1/2	SPI3	USART1/2/3	UART4/5	-	LCD	-	CPRI	SYSTEM
PC7	-	-	TIM3_CH2	-	-	-	I2S3_MCK	-	-	-	SEG25	-	TIMx_IC4	EVENT OUT
PC8	-	-	TIM3_CH3	-	-	-	-	-	-	-	SEG26	-	TIMx_IC1	EVENT OUT
PC9	-	-	TIM3_CH4	-	-	-	-	-	-	-	SEG27	-	TIMx_IC2	EVENT OUT
PC10	-	-	-	-	-	-	SPI3_SCK I2S3_CK	USART3_TX	UART4_TX	-	COM4/ SEG28/ SEG40	-	TIMx_IC3	EVENT OUT
PC11	-	-	-	-	-	-	SPI3_MISO	USART3_RX	UART4_RX	-	COM5/ SEG29 /SEG41	-	TIMx_IC4	EVENT OUT
PC12	-	-	-	-	-	-	SPI3_MOSI I2S3_SD	USART3_CK	UART5_TX	-	COM6/ SEG30/ SEG42	-	TIMx_IC1	EVENT OUT
PC13-WKUP2	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENT OUT
PC14 OSC32_IN	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENT OUT
PC15 OSC32_OUT	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC4	EVENT OUT
PD0	-	-	-	TIM9_CH1	-	SPI2_NSS I2S2_WS	-	-	-	-	-	-	TIMx_IC1	EVENT OUT
PD1	-	-	-	-	-	SPI2 SCK I2S2_CK	-	-	-	-	-	-	TIMx_IC2	EVENT OUT
PD2	-	-	TIM3_ETR	-	-	-	-	-	UART5_RX	-	COM7/ SEG31/ SEG43	-	TIMx_IC3	EVENT OUT
PD3	-	-	-	-	-	SPI2_MISO	-	USART2_CTS	-	-	-	-	TIMx_IC4	EVENT OUT

Table 9. Alternate function input/output (continued)

Port name	Digital alternate function number													
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFIO6	AFIO7	AFIO8	..	AFIO11	..	AFIO14	AFIO15
	Alternate function													
	SYSTEM	TIM2	TIM3/4/5	TIM9/10/11	I2C1/2	SPI1/2	SPI3	USART1/2/3	UART4/5	-	LCD	-	CPRI	SYSTEM
PF0	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PF1	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PF2	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PF3	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PF4	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PF5	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PF6	-	-	TIM5_ETR	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PF7	-	-	TIM5_CH2	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PF8	-	-	TIM5_CH3	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PF9	-	-	TIM5_CH4	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PF10	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PF11	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PF12	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PF13	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT

Table 9. Alternate function input/output (continued)

Port name	Digital alternate function number													
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFIO6	AFIO7	AFIO8	..	AFIO11	..	AFIO14	AFIO15
	Alternate function													
	SYSTEM	TIM2	TIM3/4/5	TIM9/10/11	I2C1/2	SPI1/2	SPI3	USART1/2/3	UART4/5	-	LCD	-	CPRI	SYSTEM
PF14	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PF15	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG0	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG1	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG2	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG3	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG4	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG5	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG6	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG7	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG8	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG9	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG10	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG11	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT

Table 9. Alternate function input/output (continued)

Port name	Digital alternate function number													
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFIO6	AFIO7	AFIO8	..	AFIO11	..	AFIO14	AFIO15
	Alternate function													
	SYSTEM	TIM2	TIM3/4/5	TIM9/10/11	I2C1/2	SPI1/2	SPI3	USART1/2/3	UART4/5	-	LCD	-	CPRI	SYSTEM
PG12	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG13	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG14	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PG15	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
PH0OSC_IN	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PH1OSC_OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PH2	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Table 19. Current consumption in Sleep mode

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)	Unit
I_{DD} (Sleep)	Supply current in Sleep mode, Flash OFF	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = $f_{HCLK}/2$ above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	51	220	µA
				2 MHz	81	300	
				4 MHz	140	380	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	175	500	
				8 MHz	330	700	
				16 MHz	625	1100	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	395	800	
				16 MHz	760	1250	
				32 MHz	1700	2700	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	670	1100	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	1750	2700	
		MSI clock, 65 kHz	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	65 kHz	19	92	
		MSI clock, 524 kHz		524 kHz	33	110	
		MSI clock, 4.2 MHz		4.2 MHz	150	273	
	Supply current in Sleep mode, Flash ON	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = $f_{HCLK}/2$ above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	63	250	
				2 MHz	93	300	
				4 MHz	155	380	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	190	500	
				8 MHz	340	700	
				16 MHz	640	1120	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	410	800	
				16 MHz	770	1300	
				32 MHz	1750	2700	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	690	1160	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	1750	2800	
	Supply current in Sleep mode, Flash ON	MSI clock, 65 kHz	Range 3, V_{CORE}=1.2V VOS[1:0] = 11	65 kHz	31	105	
		MSI clock, 524 kHz		524 kHz	45	125	
		MSI clock, 4.2 MHz		4.2 MHz	160	290	

1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register)

Table 32. MSI oscillator characteristics (continued)

Symbol	Parameter	Condition	Typ	Max	Unit
$t_{STAB(MSI)}$(2)	MSI oscillator stabilization time	MSI range 0	-	40	µs
		MSI range 1	-	20	
		MSI range 2	-	10	
		MSI range 3	-	4	
		MSI range 4	-	2.5	
		MSI range 5	-	2	
		MSI range 6, Voltage range 1 and 2	-	2	
		MSI range 3, Voltage range 3	-	3	
$f_{OVER(MSI)}$	MSI oscillator frequency overshoot	Any range to range 5	-	4	MHz
		Any range to range 6	-	6	

1. This is a deviation for an individual part, once the initial frequency has been measured.
2. Guaranteed by characterization results.

6.3.8 PLL characteristics

The parameters given in *Table 33* are derived from tests performed under the conditions summarized in *Table 13*.

Table 33. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max(1)	
f_{PLL_IN}	PLL input clock(2)	2	-	24	MHz
	PLL input clock duty cycle	45	-	55	%
f_{PLL_OUT}	PLL output clock	2	-	32	MHz
t_{LOCK}	PLL lock time PLL input = 16 MHz PLL VCO = 96 MHz	-	115	160	µs
Jitter	Cycle-to-cycle jitter	-	-	±600	ps
I_{DDA}(PLL)	Current consumption on V_{DDA}	-	220	450	µA
I_{DD}(PLL)	Current consumption on V_{DD}	-	120	150	

1. Guaranteed by characterization results.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

6.3.9 Memory characteristics

The characteristics are given at T_A = -40 to 105 °C unless otherwise specified.

RAM memory

Table 34. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VRM	Data retention mode(1)	STOP mode (or RESET)	1.65	-	-	V

1. Minimum supply voltage without losing data stored in RAM (in Stop mode or under Reset) or in hardware registers (only in Stop mode).

6.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 37*. They are based on the EMS levels and classes defined in application note AN1709.

Table 37. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144, T_A = +25 °C, f_{HCLK} = 32 MHz conforms to IEC 61000-4-2	4B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP144, T_A = +25 °C, f_{HCLK} = 32 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.

SPI characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the conditions summarized in *Table 13*.

Refer to *Section 6.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 49. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Max(2)	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	16	MHz
		Slave mode	-	16	
		Slave transmitter	-	12(3)	
$t_{r(SCK)}$(2) $t_{f(SCK)}$(2)	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	6	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode	$4t_{HCLK}$	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2t_{HCLK}$	-	
$t_{w(SCKH)}$(2) $t_{w(SCKL)}$(2)	SCK high and low time	Master mode	$t_{SCK}/2-5$	$t_{SCK}/2+3$	
$t_{su(MI)}$(2)	Data input setup time	Master mode	5	-	
$t_{su(SI)}$(2)		Slave mode	6	-	
$t_{h(MI)}$(2)	Data input hold time	Master mode	5	-	
$t_{h(SI)}$(2)		Slave mode	5	-	
$t_{a(SO)}$(4)	Data output access time	Slave mode	0	$3t_{HCLK}$	
$t_{v(SO)}$(2)	Data output valid time	Slave mode	-	33	
$t_{v(MO)}$(2)	Data output valid time	Master mode	-	6.5	
$t_{h(SO)}$(2)	Data output hold time	Slave mode	17	-	
$t_{h(MO)}$(2)		Master mode	0.5	-	

1. The characteristics above are given for voltage range 1.
2. Guaranteed by characterization results.
3. The maximum SPI clock frequency in slave transmitter mode is given for an SPI slave input clock duty cycle (DuCy(SCK)) ranging between 40 to 60%.
4. Min time is for the minimum time to drive the output and max time is for the maximum time to validate the data.

Figure 20. SPI timing diagram - slave mode and CPHA = 0

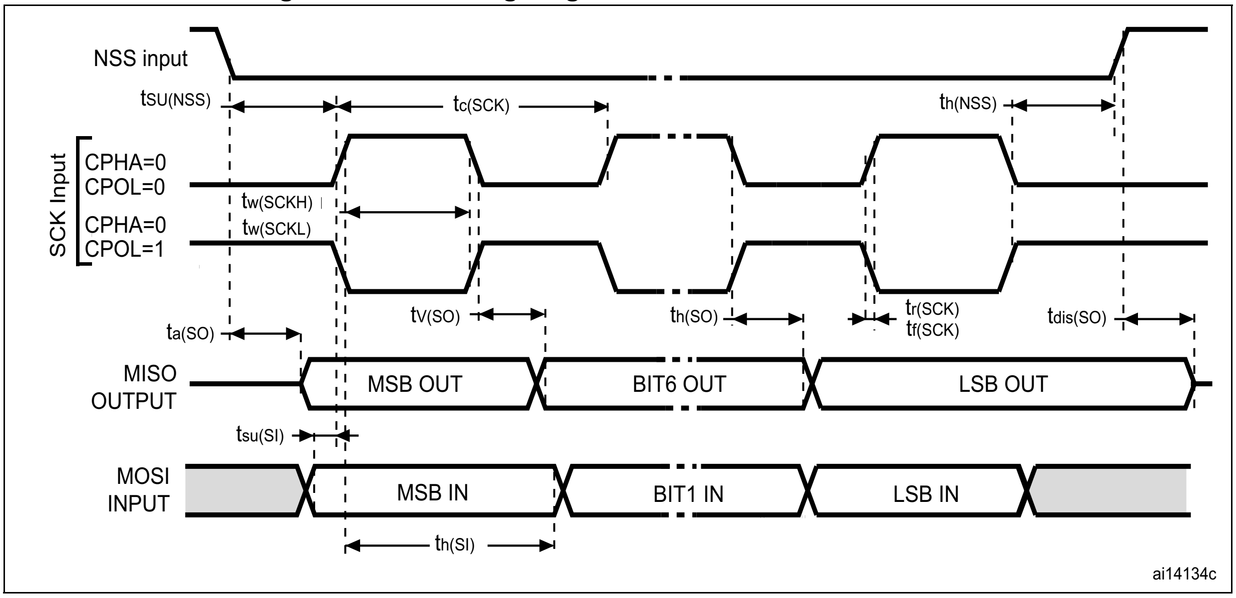
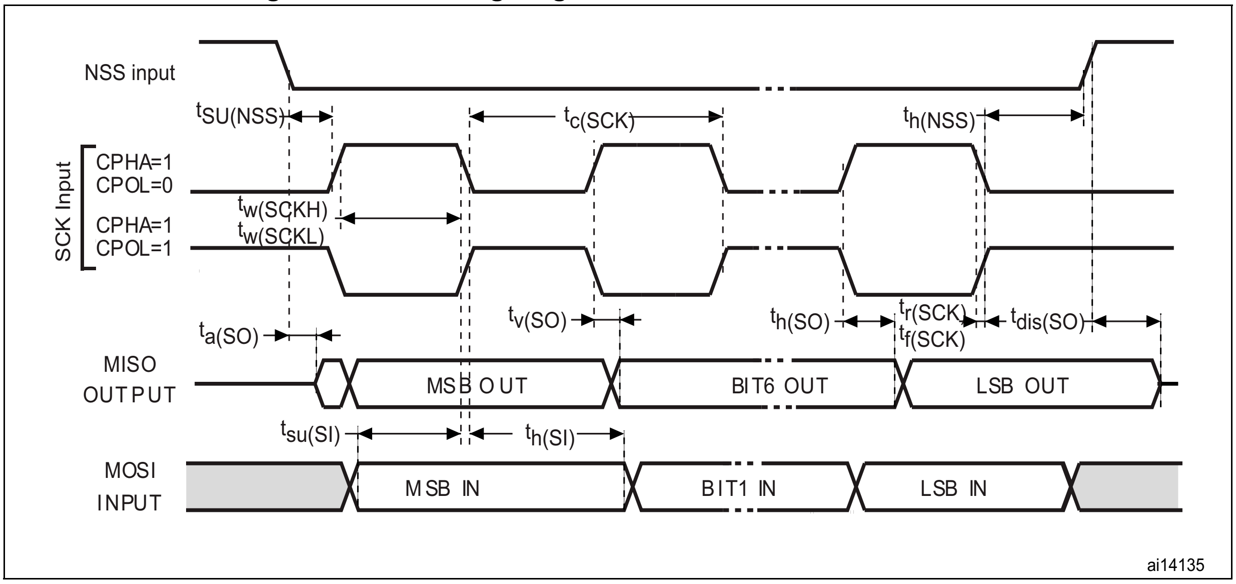
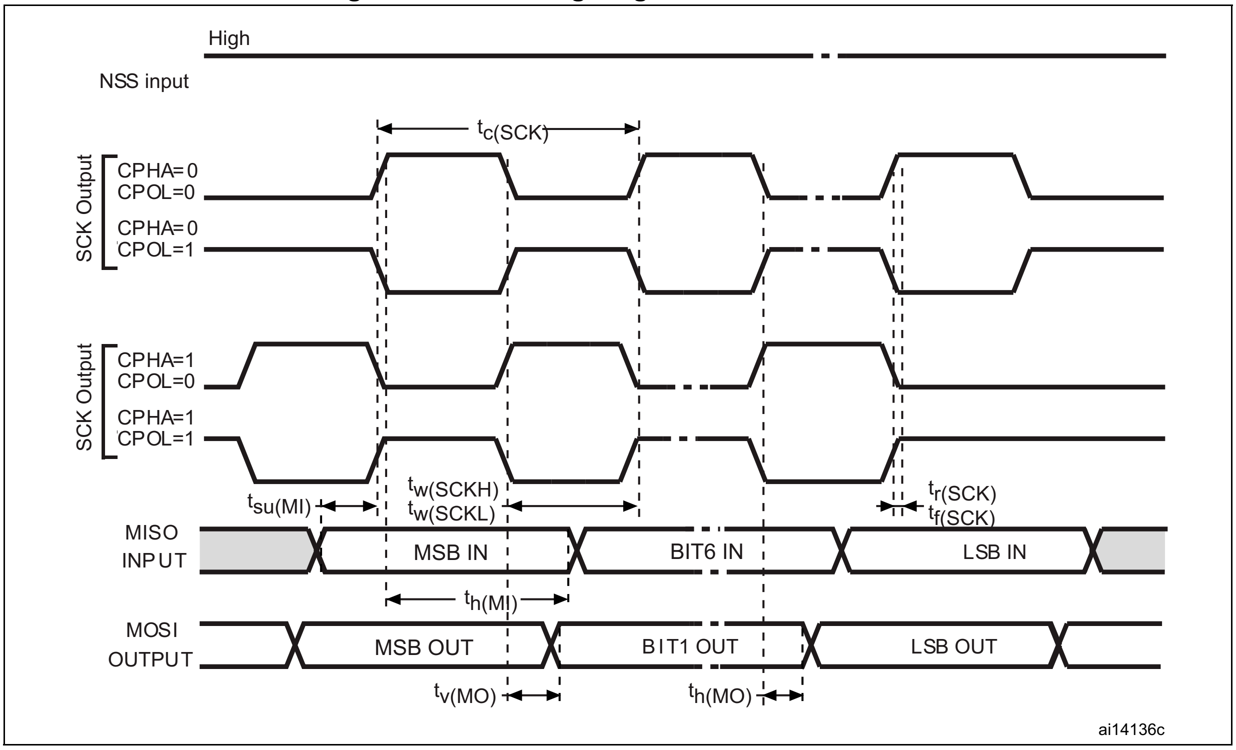


Figure 21. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 22. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

6.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in Table 55 are guaranteed by design.

Table 54. ADC clock frequency

Symbol	Parameter	Conditions			Min	Max	Unit
f_{ADC}	ADC clock frequency	Voltage range 1 & 2	2.4 V ≤ V_{DDA} ≤ 3.6 V	$V_{REF+} = V_{DDA}$	0.480	16	MHz
				$V_{REF+} < V_{DDA}$ $V_{REF+} > 2.4$ V		8	
				$V_{REF+} < V_{DDA}$ $V_{REF+} \leq 2.4$ V		4	
			1.8 V ≤ V_{DDA} ≤ 2.4 V	$V_{REF+} = V_{DDA}$		8	
				$V_{REF+} < V_{DDA}$		4	
		Voltage range 3				4	

Table 55. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	1.8	-	3.6	V
V_{REF+}	Positive reference voltage	-	1.8[1]	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-	-	V_{SSA}	-	
I_{VDDA}	Current on the V_{DDA} input pin	-	-	1000	1450	µA
I_{VREF}[2]	Current on the V_{REF} input pin	Peak	-	400	700	
		Average			450	
V_{AIN}	Conversion voltage range[3]	-	0[4]	-	V_{REF+}	V
f_S	12-bit sampling rate	Direct channels	-	-	1	Msps
		Multiplexed channels	-	-	0.76	
	10-bit sampling rate	Direct channels	-	-	1.07	Msps
		Multiplexed channels	-	-	0.8	
	8-bit sampling rate	Direct channels	-	-	1.23	Msps
		Multiplexed channels	-	-	0.89	
	6-bit sampling rate	Direct channels	-	-	1.45	Msps
		Multiplexed channels	-	-	1	

Figure 28. Maximum dynamic current consumption on V_{REF+} supply pin during ADC conversion

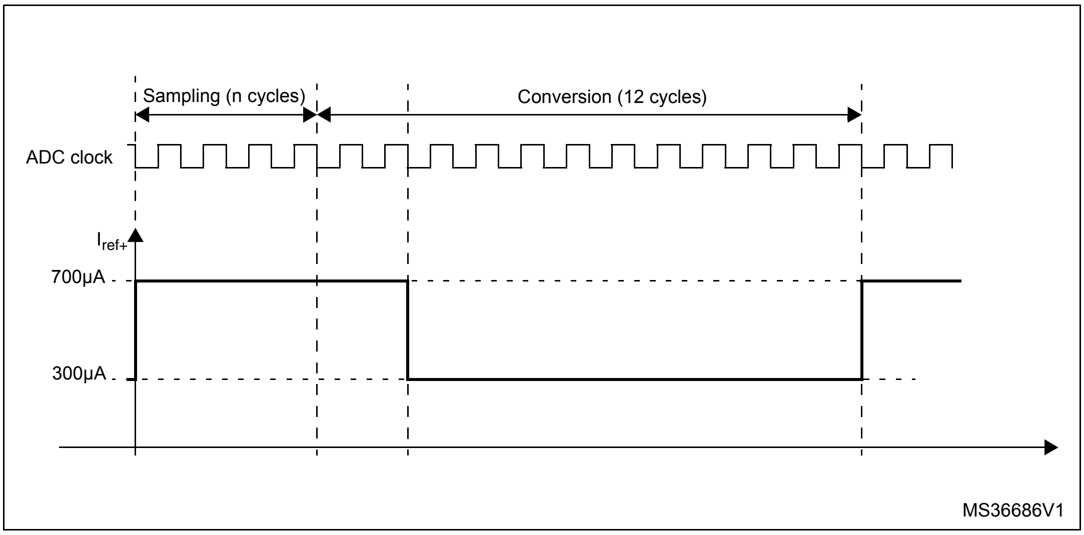


Table 57. Maximum source impedance R_{AIN} max[(1)]

Ts (µs)	R_{AIN} max (kΩ)				Ts (cycles) f_{ADC}=16 MHz[(2)]
	Multiplexed channels		Direct channels		
	2.4 V < V_{DDA} < 3.6 V	1.8 V < V_{DDA} < 2.4 V	2.4 V < V_{DDA} < 3.6 V	1.8 V < V_{DDA} < 2.4 V	
0.25	Not allowed	Not allowed	0.7	Not allowed	4
0.5625	0.8	Not allowed	2.0	1.0	9
1	2.0	0.8	4.0	3.0	16
1.5	3.0	1.8	6.0	4.5	24
3	6.8	4.0	15.0	10.0	48
6	15.0	10.0	30.0	20.0	96
12	32.0	25.0	50.0	40.0	192
24	50.0	50.0	50.0	50.0	384

1. Guaranteed by design.
2. Number of samples calculated for f_{ADC} = 16 MHz. For f_{ADC} = 8 and 4 MHz the number of sampling cycles can be reduced with respect to the minimum sampling time Ts (µs),

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 10*. The applicable procedure depends on whether V_{REF+} is connected to V_{DDA} or not. The 100 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

6.3.20 Temperature sensor characteristics

Table 60. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C ±5 °C V_{DDA}= 3 V ±10 mV	0x1FF8 00FA - 0x1FF8 00FB
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C ±5 °C V_{DDA}= 3 V ±10 mV	0x1FF8 00FE - 0x1FF8 00FF

Table 61. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	1.48	1.61	1.75	mV/°C
V_{110}	Voltage at 110°C ±5°C(2)	612	626.8	641.5	mV
$I_{DDA(TEMP)}$(3)	Current consumption	-	3.4	6	µA
t_{START}(3)	Startup time	-	-	10	µs
T_{S_temp}(3)	ADC sampling time when reading the temperature	4	-	-	µs

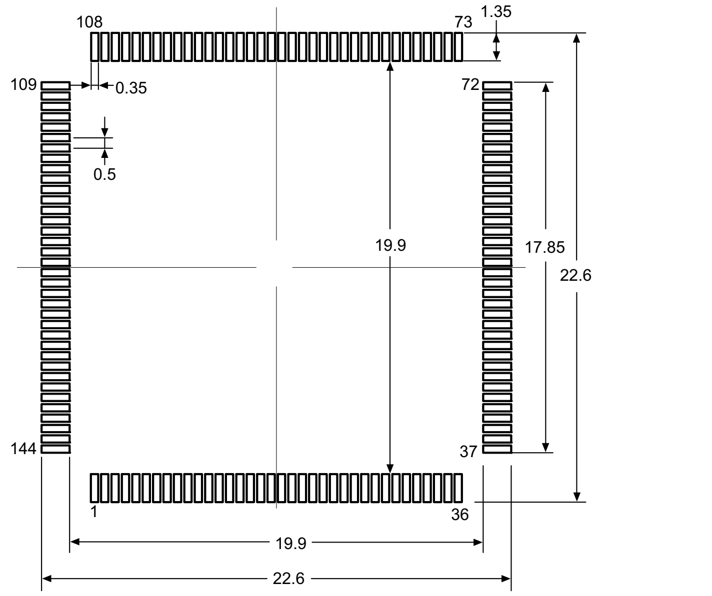
1. Guaranteed by characterization results.
2. Measured at V_{DD} = 3 V ±10 mV. V110 ADC conversion result is stored in the TS_CAL2 byte.
3. Guaranteed by design.

6.3.21 Comparator

Table 62. Comparator 1 characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	-	1.65		3.6	V
R_{400K}	R_{400K} value	-	-	400	-	kΩ
R_{10K}	R_{10K} value	-	-	10	-	kΩ
V_{IN}	Comparator 1 input voltage range	-	0.6	-	V_{DDA}	V
t_{START}	Comparator startup time	-	-	7	10	µs
td	Propagation delay(2)	-	-	3	10	µs
Voffset	Comparator offset	-	-	±3	±10	mV
$d_{Voffset}/dt$	Comparator offset variation in worst voltage stress conditions	V_{DDA} = 3.6 V V_{IN+} = 0 V V_{IN-} = V_{REFINT} T_A = 25 °C	0	1.5	10	mV/1000 h
I_{COMP1}	Current consumption(3)	-	-	160	260	nA

Figure 31. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package recommended footprint

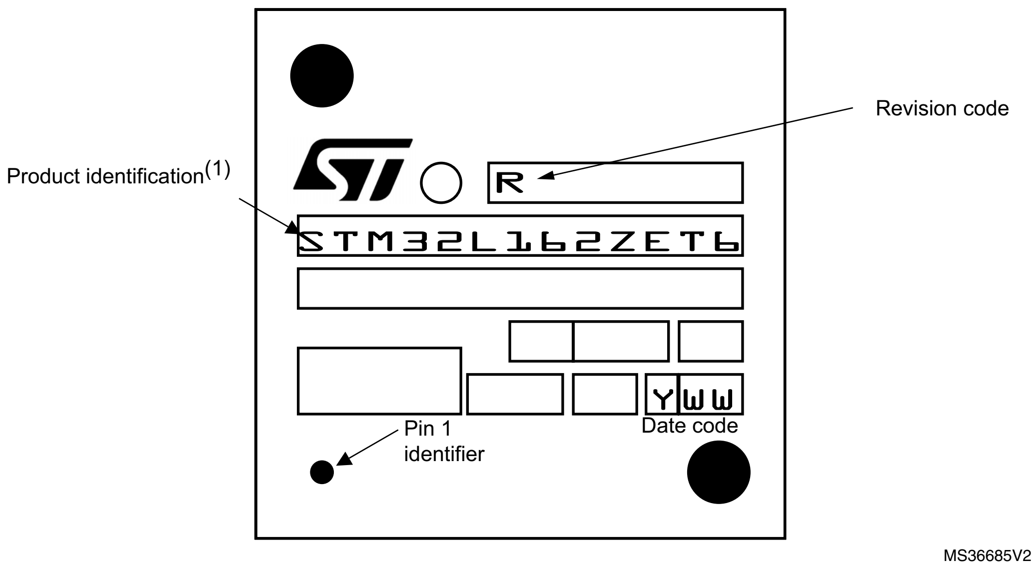


1. Dimensions are in millimeters.

Marking of engineering samples

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 32. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity