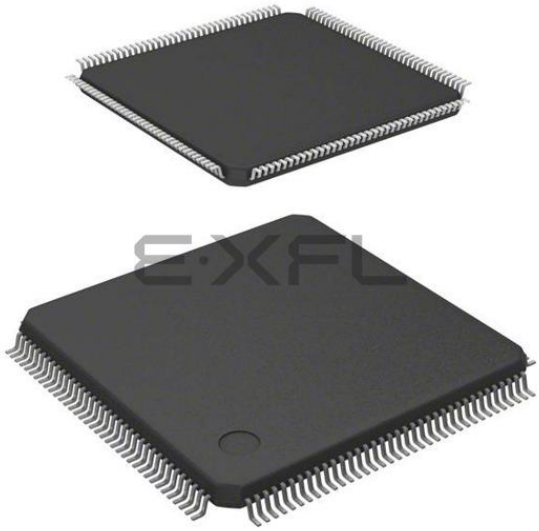

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	115
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	16K x 8
RAM Size	80K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 40x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l162zet6

Contents

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2.2 Ultra-low-power device continuum

The ultra-low-power family offers a large choice of cores and features. From proprietary 8-bit to up to Cortex-M3, including the Cortex-M0+, the STM32Lx series are the best choice to answer your needs, in terms of ultra-low-power features. The STM32 ultra-low-power series are the best fit, for instance, for gas/water meter, keyboard/mouse or fitness and healthcare, wearable applications. Several built-in features like LCD drivers, dual-bank memory, Low-power run mode, op-amp, AES 128-bit, DAC, USB crystal-less and many others will clearly allow to build very cost-optimized applications by reducing BOM.

Note: STMicroelectronics as a reliable and long-term manufacturer ensures as much as possible the pin-to-pin compatibility between any STM8Lxxxxx and STM32Lxxxxx devices and between any of the STM32Lx and STM32Fx series. Thanks to this unprecedented scalability, your old applications can be upgraded to respond to the latest market features and efficiency demand.

2.2.1 Performance

All families incorporate highly energy-efficient cores with both Harvard architecture and pipelined execution: advanced STM8 core for STM8L families and ARM Cortex-M3 core for STM32L family. In addition specific care for the design architecture has been taken to optimize the mA/DMIPS and mA/MHz ratios.

This allows the ultra-low-power performance to range from 5 up to 33.3 DMIPs.

2.2.2 Shared peripherals

STM8L15xxx, STM32L15xxx and STM32L162xx share identical peripherals which ensure a very easy migration from one family to another:

- Analog peripherals: ADC, DAC and comparators
- Digital peripherals: RTC and some communication interfaces

2.2.3 Common system strategy.

To offer flexibility and optimize performance, the STM8L15xxx, STM32L15xxx and STM32L162xx family uses a common architecture:

- Same power supply range from 1.65 V to 3.6 V
- Architecture optimized to reach ultra-low consumption both in low-power modes and Run mode
- Fast startup strategy from low-power modes
- Flexible system clock
- Ultrasafe reset: same reset strategy including power-on reset, power-down reset, brownout reset and programmable voltage detector

2.2.4 Features

ST ultra-low-power continuum also lies in feature compatibility:

- More than 15 packages with pin count from 20 to 144 pins and size down to 3 x 3 mm
- Memory density ranging from 2 to 512 Kbytes

3.4 Clock management

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler**: to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching**: clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management**: to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source**: three different clock sources can be used to drive the master clock SYSCLK:
  - 1-24 MHz high-speed external crystal (HSE), that can supply a PLL
  - 16 MHz high-speed internal RC oscillator (HSI), trimmable by software, that can supply a PLL
  - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 7 frequencies (65 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.1 MHz, 4.2 MHz). When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be trimmed by software down to a ±0.5% accuracy.
- **Auxiliary clock source**: two ultra-low-power clock sources that can be used to drive the LCD controller and the real-time clock:
  - 32.768 kHz low-speed external crystal (LSE)
  - 37 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock can be measured using the high-speed internal RC oscillator for greater precision.
- **RTC and LCD clock sources:** the LSI, LSE or HSE sources can be chosen to clock the RTC and the LCD, whatever the system clock.
- **USB clock source:** the embedded PLL has a dedicated 48 MHz clock output to supply the USB interface.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 2 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If a HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled.
- **Clock-out capability (MCO: microcontroller clock output):** it outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, each APB (APB1 and APB2) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See *Figure 2* for details on the clock tree.

3.7 Memories

The STM32L162xE devices have the following features:

- 80 Kbytes of embedded RAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
  - 512 Kbytes of embedded Flash program memory
  - 16 Kbytes of data EEPROM
  - Options bytes

  Flash program and data EEPROM are divided into two banks, this enables writing in one bank while running code or reading data in the other bank.

  The options bytes are used to write-protect or read-out protect the memory (with 4 Kbytes granularity) and/or readout-protect the whole memory with the following options:
  - Level 0: no readout protection
  - Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
  - Level 2: chip readout protection, debug features (ARM Cortex-M3 JTAG and serial wire) and boot in RAM selection disabled (JTAG fuse)

  The whole non-volatile memory embeds the error correction code (ECC) feature.

3.8 DMA (direct memory access)

The flexible 12-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: AES, SPI, I^2C, USART, general-purpose timers, DAC and ADC.

3.13 Ultra-low-power comparators and reference voltage

The STM32L162xE devices embed two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- One comparator with fixed threshold
- One comparator with rail-to-rail inputs, fast or slow mode. The threshold can be one of the following:
  - DAC output
  - External I/O
  - Internal reference voltage (V_{REFINT}) or a sub-multiple (1/4, 1/2, 3/4)

Both comparators can wake up from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low-power / low-current output buffer (driving current capability of 1 µA typical).

3.14 System configuration controller and routing interface

The system configuration controller provides the capability to remap some alternate functions on different I/O ports.

The highly flexible routing interface allows the application firmware to control the routing of different I/Os to the TIM2, TIM3 and TIM4 timer input captures. It also controls the routing of internal analog signals to ADC1, COMP1 and COMP2 and the internal reference voltage V_{REFINT}.

3.15 Touch sensing

The STM32L162xE devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 34 capacitive sensing channels distributed over 11 analog I/O groups. Both software and timer capacitive sensing acquisition modes are supported.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. The capacitive sensing acquisition only requires few external components to operate. This acquisition is managed directly by the GPIOs, timers and analog I/O groups (see *Section 3.14: System configuration controller and routing interface*).

Reliable touch sensing functionality can be quickly and easily implemented using the free STM32L1xx STMTouch touch sensing firmware library.

3.16 AES

The AES Hardware Accelerator can be used to encrypt and decrypt data using the AES

algorithm (compatible with FIPS PUB 197, 2001 Nov 26).

- Key scheduler
- Key derivation for decryption
- 128-bit data block processed
- 128-bit key length
- 213 clock cycles to encrypt/decrypt one 128-bit block
- Electronic codebook (ECB), cypher block chaining (CBC), and counter mode (CTR) supported by hardware.

AES data flow can be served by 2ch (D_{IN}/D_{OUT}) of the DMA2 controller

3.17 Timers and watchdogs

The ultra-low-power STM32L162xE devices include seven general-purpose timers, two basic timers, and two watchdog timers.

Table 6 compares the features of the general-purpose and basic timers.

Table 6. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM2, TIM3, TIM4	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM5	32-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM9	16-bit	Up, down, up/down	Any integer between 1 and 65536	No	2	No
TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.17.1 General-purpose timers (TIM2, TIM3, TIM4, TIM5, TIM9, TIM10 and TIM11)

There are seven synchronizable general-purpose timers embedded in the STM32L162xE devices (see *Table 6* for differences).

TIM2, TIM3, TIM4, TIM5

TIM2, TIM3, TIM4 are based on 16-bit auto-reload up/down counter. TIM5 is based on a 32-bit auto-reload up/down counter. They include a 16-bit prescaler. They feature four independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input captures/output compares/PWMs on the largest packages.

TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together or with the TIM10, TIM11 and TIM9 general-purpose timers via the Timer Link feature for synchronization or

Table 8. STM32L162xE pin definitions (continued)

Pins				Pin name	Pin Type(1)	I / O structure	Main function(2) (after reset)	Pin functions	
LQFP144	LQFP100	LQFP64	WLCSP104					Alternate functions	Additional functions
36	25	16	J8	PA2	I/O	FT	PA2	TIM2_CH3/TIM5_CH3/ TIM9_CH1/ USART2_TX/LCD_SEG1	ADC_IN2/ COMP1_INP/ OPAMP1_VINM
37	26	17	H7	PA3	I/O	TC	PA3	TIM2_CH4/TIM5_CH4/ TIM9_CH2/ USART2_RX/LCD_SEG2	ADC_IN3/ COMP1_INP/ OPAMP1_VOUT
38	27	18	K8	V_{SS_4}	S	-	V_{SS_4}	-	-
39	28	19	L8, M9	V_{DD_4}	S	-	V_{DD_4}	-	-
40	29	20	J7	PA4	I/O	TC	PA4	SPI1_NSS/SPI3_NSS/ I2S3_WS/ USART2_CK	ADC_IN4/DAC_OUT1 /COMP1_INP
41	30	21	M8	PA5	I/O	TC	PA5	TIM2_CH1_ETR/ SPI1_SCK	ADC_IN5/ DAC_OUT2/ COMP1_INP
42	31	22	H6	PA6	I/O	FT	PA6	TIM3_CH1/TIM10_CH1/ SPI1_MISO/ LCD_SEG3	ADC_IN6/ COMP1_INP/ OPAMP2_VINP
43	32	23	K7	PA7	I/O	FT	PA7	TIM3_CH2/TIM11_CH1/ SPI1_MOSI/ LCD_SEG4	ADC_IN7/ COMP1_INP/ OPAMP2_VINM
44	33	24	L7	PC4	I/O	FT	PC4	LCD_SEG22	ADC_IN14/ COMP1_INP
45	34	25	M7	PC5	I/O	FT	PC5	LCD_SEG23	ADC_IN15/ COMP1_INP
46	35	26	J6	PB0	I/O	TC	PB0	TIM3_CH3/LCD_SEG5	ADC_IN8/ COMP1_INP/ OPAMP2_VOUT/ VREF_OUT
47	36	27	K6	PB1	I/O	FT	PB1	TIM3_CH4/LCD_SEG6	ADC_IN9/ COMP1_INP/ VREF_OUT
48	37	28	M6	PB2	I/O	FT	PB2/ BOOT1	BOOT1	ADC_IN0b
49	-	-	-	PF11	I/O	FT	PF11	-	ADC_IN1b
50	-	-	-	PF12	I/O	FT	PF12	-	ADC_IN2b

Table 9. Alternate function input/output (continued)

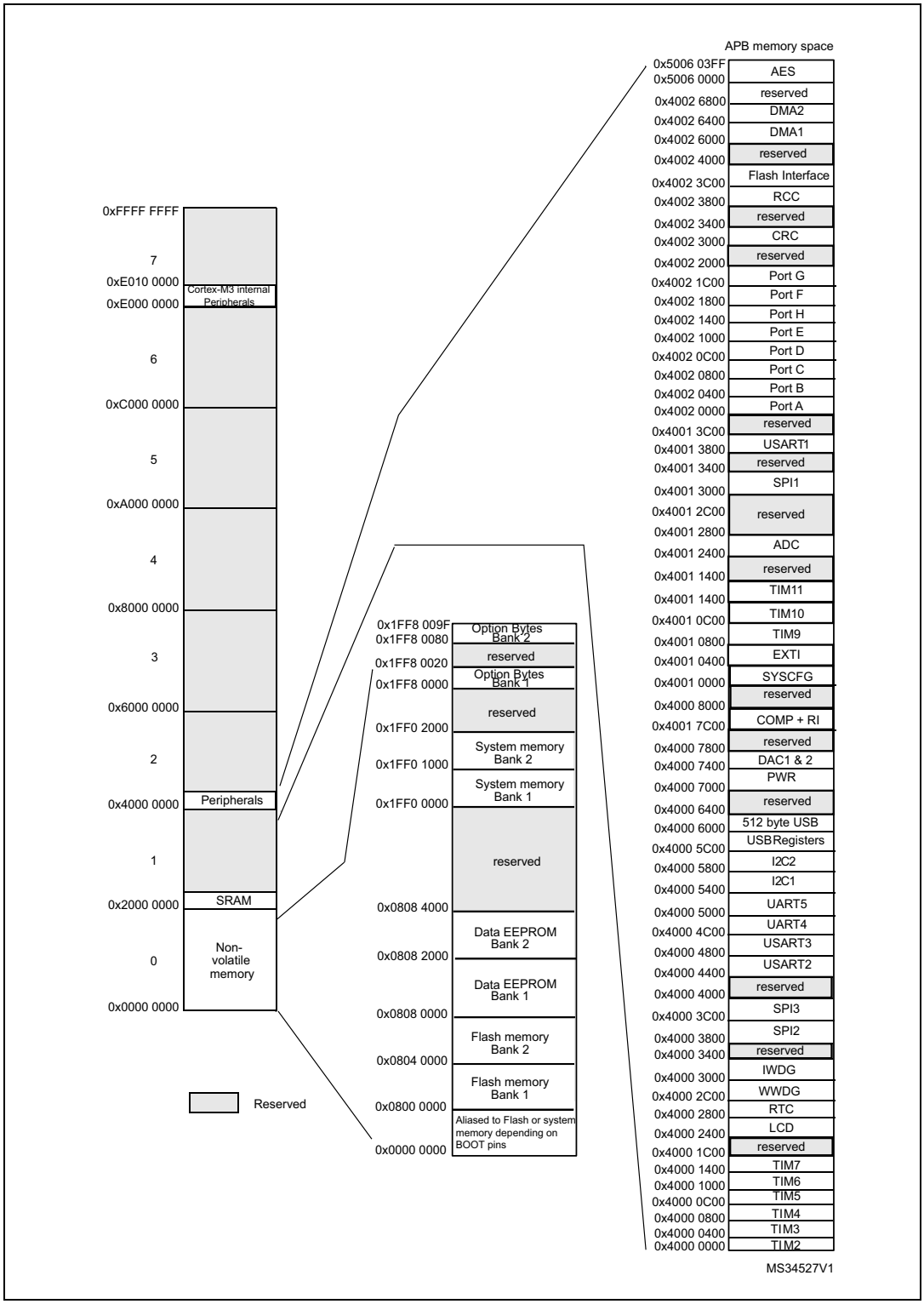
Port name	Digital alternate function number														
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFIO6	AFIO7	AFIO8	. .	AFIO11	. .	AFIO14	AFIO15
	Alternate function													
	SYSTEM	TIM2	TIM3/4/5	TIM9/10/11	I2C1/2	SPI1/2	SPI3	USART1/2/3	UART4/5	-	LCD	-	CPRI	SYSTEM
PB9	-	-	TIM4_CH4	TIM11_CH1	I2C1_SDA	-	-	-	-	-	COM3	-	-	EVENT OUT
PB10	-	TIM2_CH3	-	-	I2C2_SCL	-	-	USART3_TX	-	-	SEG10	-	-	EVENT OUT
PB11	-	TIM2_CH4	-	-	I2C2_SDA	-	-	USART3_RX	-	-	SEG11	-	-	EVENT OUT
PB12	-	-	-	TIM10_CH1	I2C2_SMBA	SPI2_NSS I2S2_WS	-	USART3_CK	-	-	SEG12	-	-	EVENT OUT
PB13	-	-	-	TIM9_CH1	-	SPI2_SCK I2S2_CK	-	USART3_CTS	-	-	SEG13	-	-	EVENT OUT
PB14	-	-	-	TIM9_CH2	-	SPI2_MISO	-	USART3_RTS	-	-	SEG14	-	-	EVENT OUT
PB15	-	-	-	TIM11_CH1	-	SPI2_MOSI I2S2_SD	-	-	-	-	SEG15	-	-	EVENT OUT
PC0	-	-	-	-	-	-	-	-	-	-	SEG18	-	TIMx_IC1	EVENT OUT
PC1	-	-	-	-	-	-	-	-	-	-	SEG19	-	TIMx_IC2	EVENT OUT
PC2	-	-	-	-	-	-	-	-	-	-	SEG20	-	TIMx_IC3	EVENT OUT
PC3	-	-	-	-	-	-	-	-	-	-	SEG21	-	TIMx_IC4	EVENT OUT
PC4	-	-	-	-	-	-	-	-	-	-	SEG22	-	TIMx_IC1	EVENT OUT
PC5	-	-	-	-	-	-	-	-	-	-	SEG23	-	TIMx_IC2	EVENT OUT
PC6	-	-	TIM3_CH1	-	-	I2S2_MCK	-	-	-	-	SEG24	-	TIMx_IC3	EVENT OUT

Table 9. Alternate function input/output (continued)

Port name	Digital alternate function number														
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFIO6	AFIO7	AFIO8	. .	AFIO11	. .	AFIO14	AFIO15
	Alternate function													
	SYSTEM	TIM2	TIM3/4/5	TIM9/10/11	I2C1/2	SPI1/2	SPI3	USART1/2/3	UART4/5	-	LCD	-	CPRI	SYSTEM
PC7	-	-	TIM3_CH2	-	-	-	I2S3_MCK	-	-	-	SEG25	-	TIMx_IC4	EVENT OUT
PC8	-	-	TIM3_CH3	-	-	-	-	-	-	-	SEG26	-	TIMx_IC1	EVENT OUT
PC9	-	-	TIM3_CH4	-	-	-	-	-	-	-	SEG27	-	TIMx_IC2	EVENT OUT
PC10	-	-	-	-	-	-	SPI3_SCK I2S3_CK	USART3_TX	UART4_TX	-	COM4/ SEG28/ SEG40	-	TIMx_IC3	EVENT OUT
PC11	-	-	-	-	-	-	SPI3_MISO	USART3_RX	UART4_RX	-	COM5/ SEG29 /SEG41	-	TIMx_IC4	EVENT OUT
PC12	-	-	-	-	-	-	SPI3_MOSI I2S3_SD	USART3_CK	UART5_TX	-	COM6/ SEG30/ SEG42	-	TIMx_IC1	EVENT OUT
PC13-WKUP2	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC2	EVENT OUT
PC14 OSC32_IN	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC3	EVENT OUT
PC15 OSC32_OUT	-	-	-	-	-	-	-	-	-	-	-	-	TIMx_IC4	EVENT OUT
PD0	-	-	-	TIM9_CH1	-	SPI2_NSS I2S2_WS	-	-	-	-	-	-	TIMx_IC1	EVENT OUT
PD1	-	-	-	-	-	SPI2 SCK I2S2_CK	-	-	-	-	-	-	TIMx_IC2	EVENT OUT
PD2	-	-	TIM3_ETR	-	-	-	-	-	UART5_RX	-	COM7/ SEG31/ SEG43	-	TIMx_IC3	EVENT OUT
PD3	-	-	-	-	-	SPI2_MISO	-	USART2_CTS	-	-	-	-	TIMx_IC4	EVENT OUT

5 Memory mapping

Figure 7. Memory map



6.3.3 Embedded internal reference voltage

The parameters given in *Table 16* are based on characterization results, unless otherwise specified.

Table 15. Embedded internal reference voltage calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 30 °C ±5 °C V_{DDA}= 3 V ±10 mV	0x1FF8 00F8 - 0x1FF8 00F9

Table 16. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{REFINT\ out}$ (1)	Internal reference voltage	– 40 °C < T_J < +110 °C	1.202	1.224	1.242	V
I_{REFINT}	Internal reference current consumption	-	-	1.4	2.3	µA
$T_{VREFINT}$	Internal reference startup time	-	-	2	3	ms
V_{VREF_MEAS}	V_{DDA} and V_{REF+} voltage during V_{REFINT} factory measure	-	2.99	3	3.01	V
A_{VREF_MEAS}	Accuracy of factory-measured V_{REF} value(2)	Including uncertainties due to ADC and V_{DDA}/V_{REF+} values	-	-	±5	mV
T_{Coeff}(3)	Temperature coefficient	–40 °C < T_J < +110 °C	-	25	100	ppm/°C
A_{Coeff}(3)	Long-term stability	1000 hours, T= 25 °C	-	-	1000	ppm
$V_{DDCoeff}$(3)	Voltage coefficient	3.0 V < V_{DDA} < 3.6 V	-	-	2000	ppm/V
$T_{S\_vrefint}$(3)	ADC sampling time when reading the internal reference voltage	-	4	-	-	µs
T_{ADC_BUF}(3)	Startup time of reference voltage buffer for ADC	-	-	-	10	µs
I_{BUF_ADC}(3)	Consumption of reference voltage buffer for ADC	-	-	13.5	25	µA
I_{VREF_OUT}(3)	VREF_OUT output current (4)	-	-	-	1	µA
C_{VREF_OUT}(3)	VREF_OUT output load	-	-	-	50	pF
I_{LPBUF}(3)	Consumption of reference voltage buffer for VREF_OUT and COMP	-	-	730	1200	nA
V_{REFINT_DIV1}(3)	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}(3)	1/2 reference voltage	-	49	50	51	
V_{REFINT_DIV3}(3)	3/4 reference voltage	-	74	75	76	

1. Guaranteed by test in production.
2. The internal V_{REF} value is individually measured in production and stored in dedicated EEPROM bytes.
3. Guaranteed by characterization results.
4. To guarantee less than 1% VREF_OUT deviation.

Table 17. Current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)	Unit
I_{DD} (Run from Flash)	Supply current in Run mode, code executed from Flash	$f_{HSE} = f_{HCLK}$ up to 16 MHz included, $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	225	500	µA
				2 MHz	420	750	
				4 MHz	780	1200	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	0.98	1.6	mA
				8 MHz	1.85	2.9	
				16 MHz	3.6	5.2	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	2.2	3.5	
				16 MHz	4.4	6.5	
				32 MHz	8.6	12	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	3.6	5.2	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	8.7	12.3	
		MSI clock, 65 kHz	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	65 kHz	42	145	µA
		MSI clock, 524 kHz		524 kHz	135	250	
		MSI clock, 4.2 MHz		4.2 MHz	820	1200	

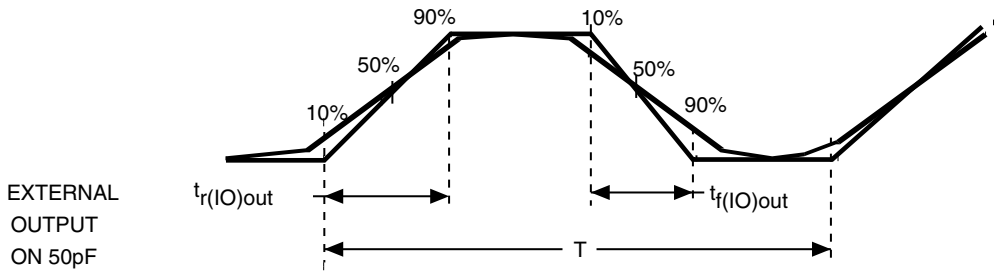
1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 19. Current consumption in Sleep mode

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)	Unit
I_{DD} (Sleep)	Supply current in Sleep mode, Flash OFF	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	51	220	µA
				2 MHz	81	300	
				4 MHz	140	380	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	175	500	
				8 MHz	330	700	
				16 MHz	625	1100	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	395	800	
				16 MHz	760	1250	
				32 MHz	1700	2700	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	670	1100	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	1750	2700	
		MSI clock, 65 kHz	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	65 kHz	19	92	
		MSI clock, 524 kHz		524 kHz	33	110	
		MSI clock, 4.2 MHz		4.2 MHz	150	273	
	Supply current in Sleep mode, Flash ON	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	1 MHz	63	250	
				2 MHz	93	300	
				4 MHz	155	380	
			Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	4 MHz	190	500	
				8 MHz	340	700	
				16 MHz	640	1120	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	8 MHz	410	800	
				16 MHz	770	1300	
				32 MHz	1750	2700	
		HSI clock source (16 MHz)	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	16 MHz	690	1160	
			Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	32 MHz	1750	2800	
	Supply current in Sleep mode, Flash ON	MSI clock, 65 kHz	Range 3, V_{CORE}=1.2V VOS[1:0] = 11	65 kHz	31	105	
		MSI clock, 524 kHz		524 kHz	45	125	
		MSI clock, 4.2 MHz		4.2 MHz	160	290	

1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register)

Figure 17. I/O AC characteristics definition



6.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 45*)

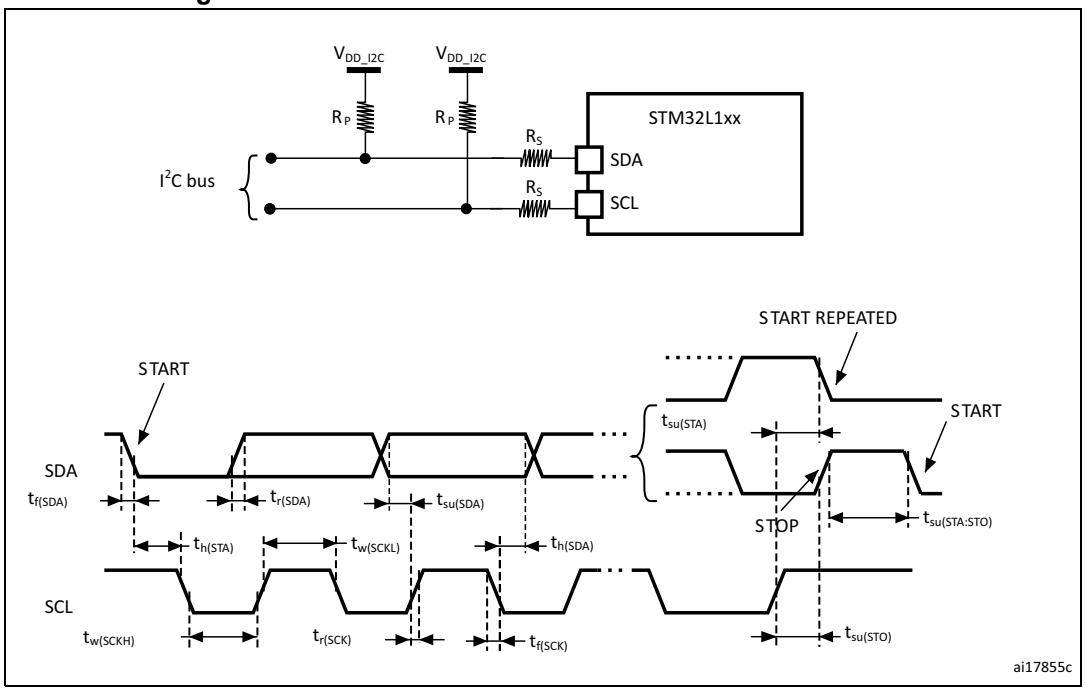
Unless otherwise specified, the parameters given in *Table 45* are derived from tests performed under the conditions summarized in *Table 13*.

Table 45. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage	-	-	-	0.3 V_{DD}	V
$V_{IH(NRST)}$(1)	NRST input high level voltage	-	0.39V_{DD}+0.59	-	-	
$V_{OL(NRST)}$(1)	NRST output low level voltage	I_{OL} = 2 mA 2.7 V < V_{DD} < 3.6 V	-	-	0.4	
		I_{OL} = 1.5 mA 1.65 V < V_{DD} < 2.7 V	-	-		
$V_{hys(NRST)}$(1)	NRST Schmitt trigger voltage hysteresis	-	-	10%V_{DD}(2)	-	mV
R_{PU}	Weak pull-up equivalent resistor(3)	V_{IN} = V_{SS}	30	45	60	kΩ
$V_{F(NRST)}$(1)	NRST input filtered pulse	-	-	-	50	ns
$V_{NF(NRST)}$(3)	NRST input not filtered pulse	-	350	-	-	ns

1. Guaranteed by design.
2. With a minimum of 200 mV.
3. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is around 10%.

Figure 19. I²C bus AC waveforms and measurement circuit



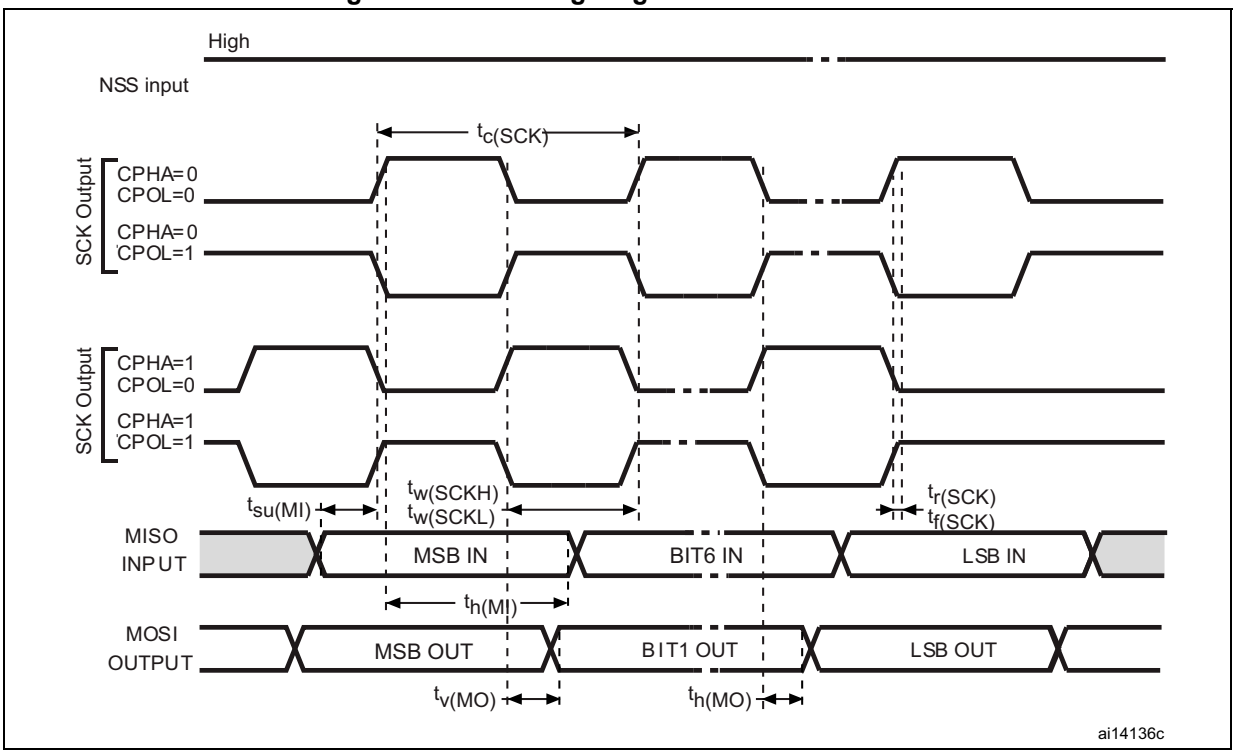
1. R_S = series protection resistor.
2. R_P = external pull-up resistor.
3. V_{DD_I2C} is the I2C bus power supply.
4. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 48. SCL frequency (f_{PCLK1}= 32 MHz, V_{DD} = V_{DD_I2C} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x801B
300	0x8024
200	0x8035
100	0x00A0
50	0x0140
20	0x0320

1. R_P = External pull-up resistance, f_{SCL} = I²C speed.
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed is ±2%. These variations depend on the accuracy of the external components used to design the application.

Figure 22. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 28. Maximum dynamic current consumption on V_{REF+} supply pin during ADC conversion

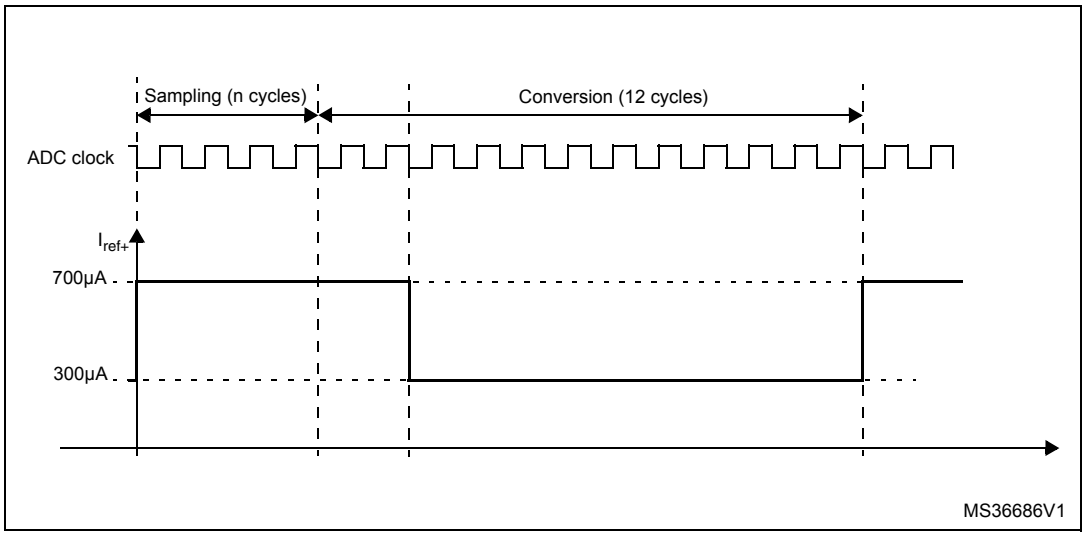


Table 57. Maximum source impedance R_{AIN} max(1)

Ts (µs)	R_{AIN} max (kΩ)				Ts (cycles) f_{ADC}=16 MHz(2)
	Multiplexed channels		Direct channels		
	2.4 V < V_{DDA} < 3.6 V	1.8 V < V_{DDA} < 2.4 V	2.4 V < V_{DDA} < 3.6 V	1.8 V < V_{DDA} < 2.4 V	
0.25	Not allowed	Not allowed	0.7	Not allowed	4
0.5625	0.8	Not allowed	2.0	1.0	9
1	2.0	0.8	4.0	3.0	16
1.5	3.0	1.8	6.0	4.5	24
3	6.8	4.0	15.0	10.0	48
6	15.0	10.0	30.0	20.0	96
12	32.0	25.0	50.0	40.0	192
24	50.0	50.0	50.0	50.0	384

1. Guaranteed by design.
2. Number of samples calculated for f_{ADC} = 16 MHz. For f_{ADC} = 8 and 4 MHz the number of sampling cycles can be reduced with respect to the minimum sampling time Ts (µs),

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 10*. The applicable procedure depends on whether V_{REF+} is connected to V_{DDA} or not. The 100 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

Table 58. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
dOffset/dT(1)	Offset error temperature coefficient (code 0x800)	V_{DDA} = 3.3V V_{REF+} = 3.0V T_A = 0 to 50 °C DAC output buffer OFF	-20	-10	0	µV/°C
		V_{DDA} = 3.3V V_{REF+} = 3.0V T_A = 0 to 50 °C DAC output buffer ON	0	20	50	
Gain(1)	Gain error(7)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON	-	+0.1 / -0.2%	+0.2 / -0.5%	%
		No R_L, $C_L \leq 50$ pF DAC output buffer OFF	-	+0 / -0.2%	+0 / -0.4%	
dGain/dT(1)	Gain error temperature coefficient	V_{DDA} = 3.3V V_{REF+} = 3.0V T_A = 0 to 50 °C DAC output buffer OFF	-10	-2	0	µV/°C
		V_{DDA} = 3.3V V_{REF+} = 3.0V T_A = 0 to 50 °C DAC output buffer ON	-40	-8	0	
TUE(1)	Total unadjusted error	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON	-	12	30	LSB
		No R_L, $C_L \leq 50$ pF DAC output buffer OFF	-	8	12	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes till DAC_OUT reaches final value ±1LSB	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ	-	7	12	µs
Update rate	Max frequency for a correct DAC_OUT change (95% of final value) with 1 LSB variation in the input code	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ	-	-	1	Msps
t_{WAKEUP}	Wakeup time from off state (setting the ENx bit in the DAC Control register)(8)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ	-	9	15	µs
PSRR+	V_{DDA} supply rejection ratio (static DC measurement)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ	-	-60	-35	dB

1. Data based on characterization results.
2. Connected between DAC_OUT and V_{SSA}.
3. Difference between two consecutive codes - 1 LSB.