Infineon Technologies - SAF-XE167FM-48F80L AA Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	119
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	34K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-144-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-xe167fm-48f80l-aa

PLL frequency band selection

Different frequency bands can be selected for the VCO so that the operation of the PLL can be adjusted to a wide range of input and output frequencies:

Table 23 System PLL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VCO output frequency (VCO controlled)	f_{VCO} CC	50		110	MHz	VCOSEL = 00_B
		100		160	MHz	VCOSEL = 01_B
VCO output frequency (VCO free-running)	f_{VCO} CC	10		40	MHz	VCOSEL = 00_B
		20		80	MHz	VCOSEL = 01_B

4.6.2.2 Wakeup Clock

When wakeup operation is selected (SYSCON0.CLKSEL = 00_B), the system clock is derived from the low-frequency wakeup clock source:

$f_{SYS} = f_{WU}$.

In this mode, a basic functionality can be maintained without requiring an external clock source and while minimizing the power consumption.

4.6.2.3 Selecting and Changing the Operating Frequency

When selecting a clock source and the clock generation method, the required parameters must be carefully written to the respective bit fields, to avoid unintended intermediate states.

Many applications change the frequency of the system clock (f_{SYS}) during operation in order to optimize system performance and power consumption. Changing the operating frequency also changes the switching currents, which influences the power supply.

To ensure proper operation of the on-chip EVRs while they generate the core voltage, the operating frequency shall only be changed in certain steps. This prevents overshoots and undershoots of the supply voltage.

To avoid the indicated problems, recommended sequences are provided which ensure the intended operation of the clock system interacting with the power system.
Please refer to the Programmer's Guide.

Table 26 is valid under the following conditions:
V_{DDP} t3.0 V; V_{DDPtyp} = 3.3 V; V_{DDP} d4.5 V; C_L t20 pF; C_L d100 pF;

Table 26 Standard Pad Parameters for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum output driver current (absolute value)[1]	I_{Omax} CC			10	mA	Strong driver
				2.5	mA	Medium driver
				0.5	mA	Weak driver
Nominal output driver current (absolute value)	I_{Onom} CC			2.5	mA	Strong driver
				1.0	mA	Medium driver
				0.1	mA	Weak driver
Rise and Fall times (10% - 90%)	t_{RF} CC			6.2 + 0.24 x C_L	ns	Strong driver; Sharp edge
				24 + 0.3 x C_L	ns	Strong driver; Medium edge
				34 + 0.3 x C_L	ns	Strong driver; Slow edge
				37 + 0.65 x C_L	ns	Medium driver
				500 + 2.5 x C_L	ns	Weak driver

1) The total output current that may be drawn at a given time must be limited to protect the supply rails from damage. For any group of 16 neighboring output pins, the total output current in each direction (I_{OL} and I_{OH}) must remain below 50 mA.

Table 30 EBC External Bus Timi ng for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output valid delay for $\overline{RD}$, WR($\overline{L}$/$\overline{H}$)	t_{10} CC		11	20	ns	
Output valid delay for $\overline{BHE}$, ALE	t_{11} CC		10	21	ns	
Address output valid delay for A23 ... A0	t_{12} CC		11	22	ns	
Address output valid delay for AD15 ... AD0 (MUX mode)	t_{13} CC		10	22	ns	
Output valid delay for $\overline{CS}$	t_{14} CC		10	13	ns	
Data output valid delay for AD15 ... AD0 (write data, MUX mode)	t_{15} CC		10	22	ns	
Data output valid delay for D15 ... D0 (write data, DEMUX mode)	t_{16} CC		10	22	ns	
Output hold time for $\overline{RD}$, WR($\overline{L}$/$\overline{H}$)	t_{20} CC	-2	8	10	ns	
Output hold time for $\overline{BHE}$, ALE	t_{21} CC	-2	8	10	ns	
Address output hold time for AD15 ... AD0	t_{23} CC	-3	8	10	ns	
Output hold time for $\overline{CS}$	t_{24} CC	-3	8	11	ns	
Data output hold time for D15 ... D0 and AD15 ... AD0	t_{25} CC	-3	8	10	ns	
Input setup time for READY, D15 ... D0, AD15 ... AD0	t_{30} SR	29	17		ns	
Input hold time READY, D15 ... D0, AD15 ... AD0[1)]	t_{31} SR	0	-9		ns	

1) Read data are latched with the same internal clock edge that triggers the address change and the rising edge of $\overline{RD}$. Address changes before the end of $\overline{RD}$ have no impact on (demultiplexed) read cycles. Read data can change after the rising edge of $\overline{RD}$.

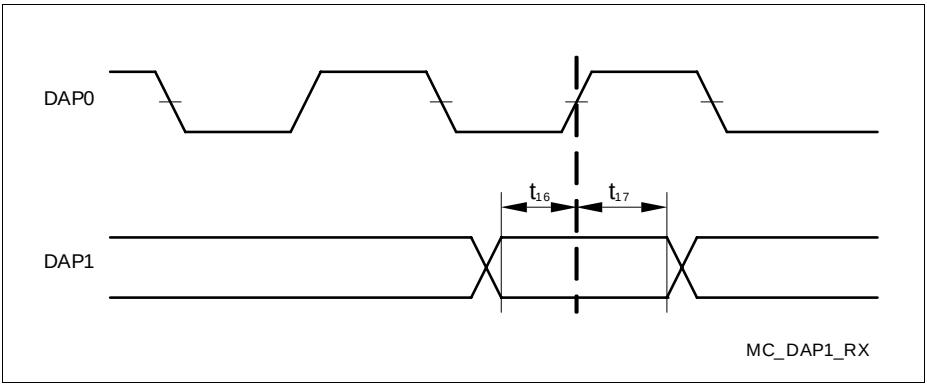

Figure 30 DAP Timing Host to Device

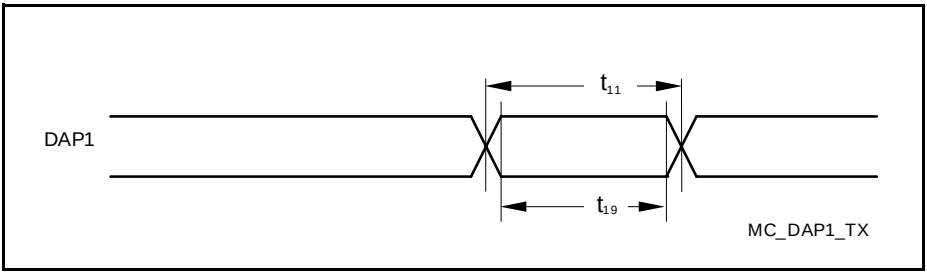

Figure 31 DAP Timing Device to Host

Note: The transmission timing is determined by the receiving debugger by evaluating the sync-request synchronization pattern telegram.