# Infineon Technologies - SAF-XE167HM-48F80L AA Datasheet

**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | C166SV2 |
| Core Size | 16-Bit |
| Speed | 80MHz |
| Connectivity | EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI |
| Peripherals | I²S, POR, PWM, WDT |
| Number of I/O | 119 |
| Program Memory Size | 384KB (384K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 34K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 24x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP Exposed Pad |
| Supplier Device Package | PG-LQFP-144-4 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/saf-xe167hm-48f80l-aa |

# 16-Bit

Architecture

# XE167FM, XE167GM, XE167HM, XE167KM

16-Bit Single-Chip Real Time Signal Controller
XE166 Family / Base Line

## Data Sheet

V2.1 2011-07

Microcontrollers

### Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. This ordering code identifies:

- the function set of the corresponding product type
- the temperature range:
  - SAF-…: -40°C to 85°C
  - SAK-…: -40°C to 125°C
- the package and the type of delivery.

For ordering codes for the XE167xM please contact your sales representative or local distributor.

This document describes several derivatives of the XE167xM group:

**Table 1** lists these derivatives and summarizes the differences.

As this document refers to all of these derivatives, some descriptions may not apply to a specific product, in particular to the special device types.

For simplicity the term **XE167xM** is used for all derivatives throughout this document.

## 2.1 Pin Configuration and Definition

The pins of the XE167xM are described in detail in **Table 5**, which includes all alternate functions. For further explanations please refer to the footnotes at the end of the table. The following figure summarizes all pins, showing their locations on the four sides of the package.

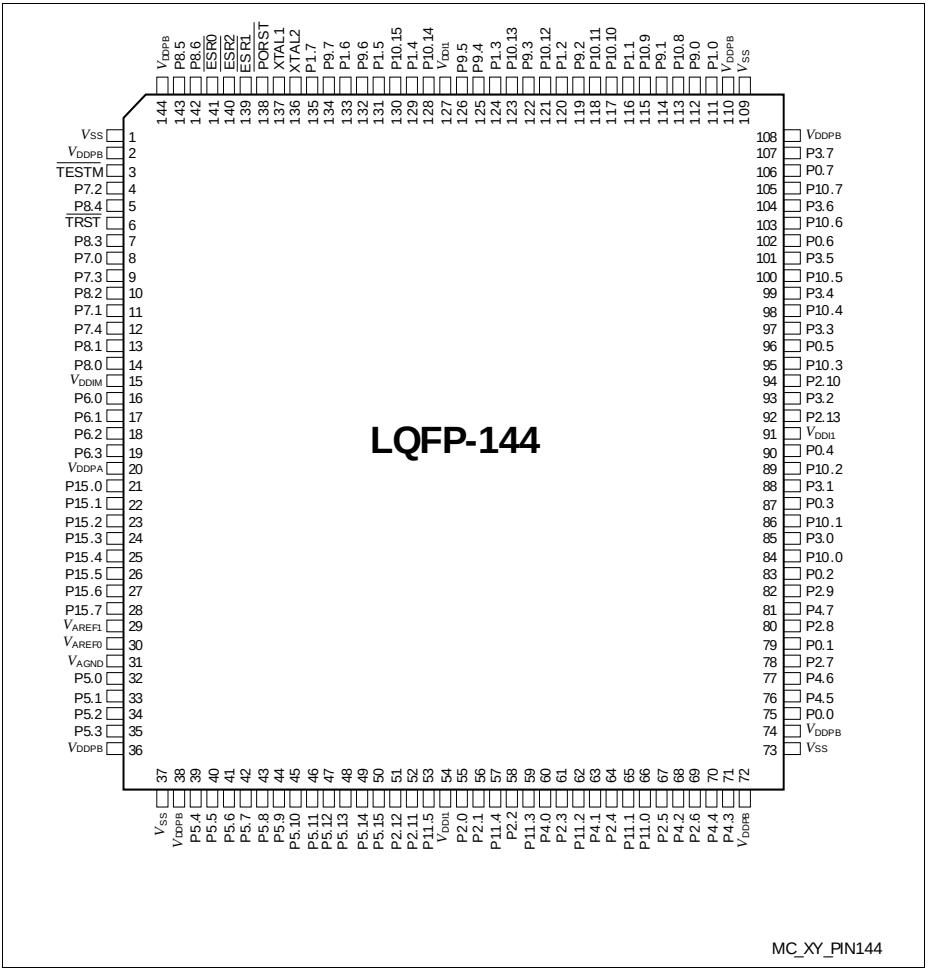


**Figure 3 XE167xM Pin Configuration (top view)**

**Table 5 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 101 | P3.5 | O0 / I | St/B | **Bit 5 of Port 3, General Purpose Input/Output** |
| | U2C1_SCLKOUT | O1 | St/B | **USIC2 Channel 1 Shift Clock Output** |
| | U2C0_SELO2 | O2 | St/B | **USIC2 Channel 0 Select/Control 2 Output** |
| | U0C0_SELO5 | O3 | St/B | **USIC0 Channel 0 Select/Control 5 Output** |
| | U2C1_DX1A | I | St/B | **USIC2 Channel 1 Shift Clock Input** |
| 102 | P0.6 | O0 / I | St/B | **Bit 6 of Port 0, General Purpose Input/Output** |
| | U1C1_DOUT | O1 | St/B | **USIC1 Channel 1 Shift Data Output** |
| | TxDC1 | O2 | St/B | **CAN Node 1 Transmit Data Output** |
| | CCU61_COUT63 | O3 | St/B | **CCU61 Channel 3 Output** |
| | A6 | OH | St/B | **External Bus Interface Address Line 6** |
| | U1C1_DX0A | I | St/B | **USIC1 Channel 1 Shift Data Input** |
| | CCU61_CTRAPA | I | St/B | **CCU61 Emergency Trap Input** |
| | U1C1_DX1B | I | St/B | **USIC1 Channel 1 Shift Clock Input** |
| 103 | P10.6 | O0 / I | St/B | **Bit 6 of Port 10, General Purpose Input/Output** |
| | U0C0_DOUT | O1 | St/B | **USIC0 Channel 0 Shift Data Output** |
| | TxDC4 | O2 | St/B | **CAN Node 4 Transmit Data Output** |
| | U1C0_SELO0 | O3 | St/B | **USIC1 Channel 0 Select/Control 0 Output** |
| | AD6 | OH / IH | St/B | **External Bus Interface Address/Data Line 6** |
| | U0C0_DX0C | I | St/B | **USIC0 Channel 0 Shift Data Input** |
| | U1C0_DX2D | I | St/B | **USIC1 Channel 0 Shift Control Input** |
| | CCU60_CTRAPA | I | St/B | **CCU60 Emergency Trap Input** |

**Table 5 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 104 | P3.6 | O0 / I | St/B | **Bit 6 of Port 3, General Purpose Input/Output** |
| | U2C1_DOUT | O1 | St/B | **USIC2 Channel 1 Shift Data Output** |
| | TxDC4 | O2 | St/B | **CAN Node 4 Transmit Data Output** |
| | U0C0_SELO 6 | O3 | St/B | **USIC0 Channel 0 Select/Control 6 Output** |
| | U2C1_DX0A | I | St/B | **USIC2 Channel 1 Shift Data Input** |
| | U2C1_DX1B | I | St/B | **USIC2 Channel 1 Shift Clock Input** |
| 105 | P10.7 | O0 / I | St/B | **Bit 7 of Port 10, General Purpose Input/Output** |
| | U0C1_DOUT | O1 | St/B | **USIC0 Channel 1 Shift Data Output** |
| | CCU60_COU T63 | O2 | St/B | **CCU60 Channel 3 Output** |
| | AD7 | OH / IH | St/B | **External Bus Interface Address/Data Line 7** |
| | U0C1_DX0B | I | St/B | **USIC0 Channel 1 Shift Data Input** |
| | CCU60_CCP OS0A | I | St/B | **CCU60 Position Input 0** |
| | RxDC4C | I | St/B | **CAN Node 4 Receive Data Input** |
| | T4INB | I | St/B | **GPT12E Timer T4 Count/Gate Input** |
| 106 | P0.7 | O0 / I | St/B | **Bit 7 of Port 0, General Purpose Input/Output** |
| | U1C1_DOUT | O1 | St/B | **USIC1 Channel 1 Shift Data Output** |
| | U1C0_SELO 3 | O2 | St/B | **USIC1 Channel 0 Select/Control 3 Output** |
| | TxDC3 | O3 | St/B | **CAN Node 3 Transmit Data Output** |
| | A7 | OH | St/B | **External Bus Interface Address Line 7** |
| | U1C1_DX0B | I | St/B | **USIC1 Channel 1 Shift Data Input** |
| | CCU61_CTR APB | I | St/B | **CCU61 Emergency Trap Input** |

**Table 5 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 117 | P10.10 | O0 / I | St/B | **Bit 10 of Port 10, General Purpose Input/Output** |
| | U0C0_SELO 0 | O1 | St/B | **USIC0 Channel 0 Select/Control 0 Output** |
| | CCU60_COU T63 | O2 | St/B | **CCU60 Channel 3 Output** |
| | AD10 | OH / IH | St/B | **External Bus Interface Address/Data Line 10** |
| | U0C0_DX2C | I | St/B | **USIC0 Channel 0 Shift Control Input** |
| | U0C1_DX1A | I | St/B | **USIC0 Channel 1 Shift Clock Input** |
| | TDI_B | IH | St/B | **JTAG Test Data Input**<br>If JTAG pos. B is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it. |
| 118 | P10.11 | O0 / I | St/B | **Bit 11 of Port 10, General Purpose Input/Output** |
| | U1C0_SCLK OUT | O1 | St/B | **USIC1 Channel 0 Shift Clock Output** |
| | $\overline{\text{BRKOUT}}$ | O2 | St/B | **OCDS Break Signal Output** |
| | U3C0_SELO 0 | O3 | St/B | **USIC3 Channel 0 Select/Control 0 Output** |
| | AD11 | OH / IH | St/B | **External Bus Interface Address/Data Line 11** |
| | U1C0_DX1D | I | St/B | **USIC1 Channel 0 Shift Clock Input** |
| | RxDC2B | I | St/B | **CAN Node 2 Receive Data Input** |
| | TMS_B | IH | St/B | **JTAG Test Mode Selection Input**<br>If JTAG pos. B is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it. |
| | U3C0_DX2A | I | St/B | **USIC3 Channel 0 Shift Control Input** |
| 119 | P9.2 | O0 / I | St/B | **Bit 2 of Port 9, General Purpose Input/Output** |
| | CCU63_CC6 2 | O1 | St/B | **CCU63 Channel 2 Output** |
| | CCU63_CC6 2INA | I | St/B | **CCU63 Channel 2 Input** |
| | CAPINB | I | St/B | **GPT12E Register CAPREL Capture Input** |

With this hardware most XE167xM instructions are executed in a single machine cycle of 12.5 ns with an 80-MHz CPU clock. For example, shift and rotate instructions are always processed during one machine cycle, no matter how many bits are shifted. Also, multiplication and most MAC instructions execute in one cycle. All multiple-cycle instructions have been optimized so that they can be executed very fast; for example, a 32-/16-bit division is started within 4 cycles while the remaining cycles are executed in the background. Another pipeline optimization, the branch target prediction, eliminates the execution time of branch instructions if the prediction was correct.

The CPU has a register context consisting of up to three register banks with 16 word-wide GPRs each at its disposal. One of these register banks is physically allocated within the on-chip DPRAM area. A Context Pointer (CP) register determines the base address of the active register bank accessed by the CPU at any time. The number of these register bank copies is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 32 Kwords is provided for storage of temporary data. The system stack can be allocated to any location within the address space (preferably in the on-chip RAM area); it is accessed by the CPU with the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared with the stack pointer value during each stack access to detect stack overflow or underflow.

The high performance of the CPU hardware implementation can be best utilized by the programmer with the highly efficient XE167xM instruction set. This includes the following instruction classes:

- Standard Arithmetic Instructions
- DSP-Oriented Arithmetic Instructions
- Logical Instructions
- Boolean Bit Manipulation Instructions
- Compare and Loop Control Instructions
- Shift and Rotate Instructions
- Prioritize Instruction
- Data Movement Instructions
- System Stack Instructions
- Jump and Call Instructions
- Return Instructions
- System Control Instructions
- Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

## 3.6 Interrupt System

The architecture of the XE167xM supports several mechanisms for fast and flexible response to service requests; these can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to be serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

Where in a standard interrupt service the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is ‘stolen’ from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source pointer, the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source-related vector location. PEC services are particularly well suited to supporting the transmission or reception of blocks of data. The XE167xM has eight PEC channels, each whith fast interrupt-driven data transfer capabilities.

With a minimum interrupt response time of 7/11[1)] CPU clocks, the XE167xM can react quickly to the occurrence of non-deterministic events.

### Interrupt Nodes and Source Selection

The interrupt system provides 96 physical nodes with separate control register containing an interrupt request flag, an interrupt enable flag and an interrupt priority bit field. Most interrupt sources are assigned to a dedicated node. A particular subset of interrupt sources shares a set of nodes. The source selection can be programmed using the interrupt source selection (ISSR) registers.

### External Request Unit (ERU)

A dedicated External Request Unit (ERU) is provided to route and preprocess selected on-chip peripheral and external interrupt requests. The ERU features 4 programmable input channels with event trigger logic (ETL) a routing matrix and 4 output gating units (OGU). The ETL features rising edge, falling edge, or both edges event detection. The OGU combines the detected interrupt events and provides filtering capabilities depending on a programmable pattern match or miss.

### Trap Processing

The XE167xM provides efficient mechanisms to identify and process exceptions or error conditions that arise during run-time, the so-called ‘Hardware Traps’. A hardware trap causes an immediate system reaction similar to a standard interrupt service (branching

1) Depending if the jump cache is used or not.

to a dedicated vector table location). The occurrence of a hardware trap is also indicated by a single bit in the trap flag register (TFR). Unless another higher-priority trap service is in progress, a hardware trap will interrupt any ongoing program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Depending on the package option up to 3 External Service Request (ESR) pins are provided. The ESR unit processes their input values and allows to implement user controlled trap functions (System Requests SR0 and SR1). In this way reset, wakeup and power control can be efficiently realized.

Software interrupts are supported by the 'TRAP' instruction in combination with an individual trap (interrupt) number. Alternatively to emulate an interrupt by software a program can trigger interrupt requests by writing the Interrupt Request (IR) bit of an interrupt control register.

## 3.7 On-Chip Debug Support (OCDS)

The On-Chip Debug Support system built into the XE167xM provides a broad range of debug and emulation features. User software running on the XE167xM can be debugged within the target system environment.

The OCDS is controlled by an external debugging device via the debug interface. This either consists of the 2-pin Device Access Port (DAP) or of the JTAG port conforming to IEEE-1149. The debug interface can be completed with an optional break interface.

The debugger controls the OCDS with a set of dedicated registers accessible via the debug interface (DAP or JTAG). In addition the OCDS system can be controlled by the CPU, e.g. by a monitor program. An injection interface allows the execution of OCDS-generated instructions by the CPU.

Multiple breakpoints can be triggered by on-chip hardware, by software, or by an external trigger input. Single stepping is supported, as is the injection of arbitrary instructions and read/write access to the complete internal address space. A breakpoint trigger can be answered with a CPU halt, a monitor call, a data transfer, or/and the activation of an external signal.

Tracing data can be obtained via the debug interface, or via the external bus interface for increased performance.

Tracing of program execution is supported by the XE166 Family emulation device.

The DAP interface uses two interface signals, the JTAG interface uses four interface signals, to communicate with external circuitry. The debug interface can be amended with two optional break lines.

**Table 8 Compare Modes** (cont'd)

| Compare Modes | Function |
|---|---|
| Mode 2 | Interrupt-only compare mode;<br>Only one compare interrupt per timer period is generated |
| Mode 3 | Pin set '1' on match; pin reset '0' on compare timer overflow;<br>Only one compare event per timer period is generated |
| Double Register Mode | Two registers operate on one pin;<br>Pin toggles on each compare match;<br>Several compare events per timer period are possible |
| Single Event Mode | Generates single edges or pulses;<br>Can be used with any compare mode |

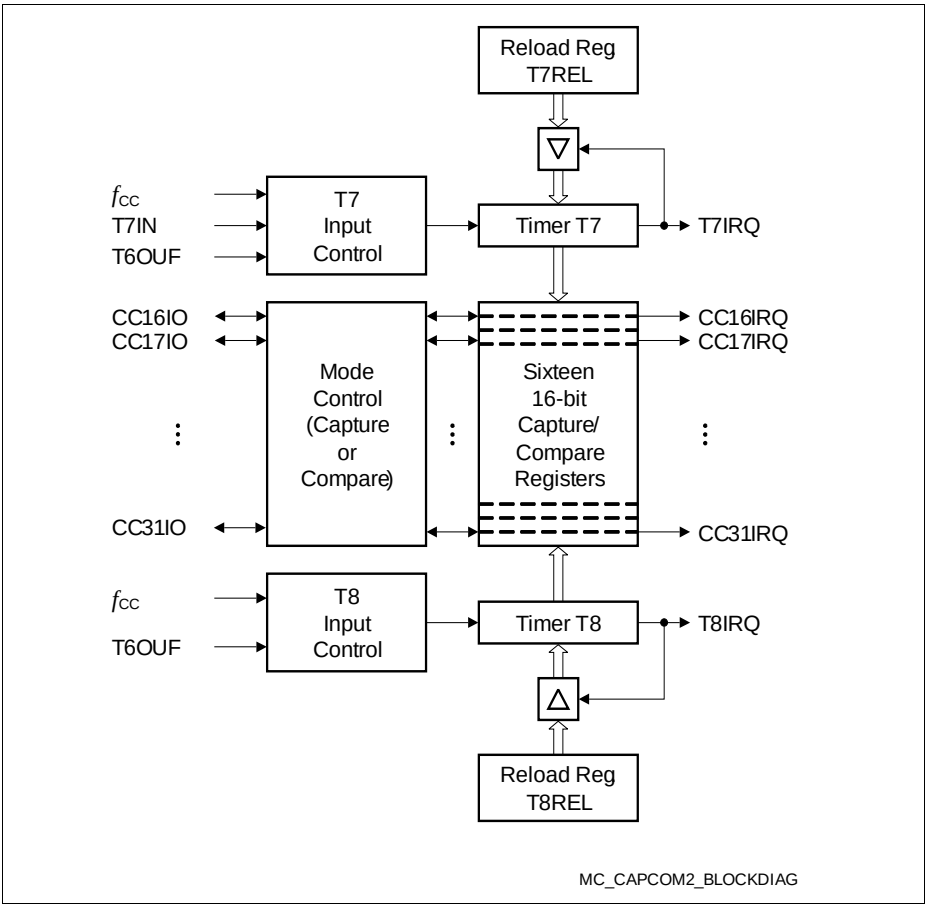


**Figure 6 CAPCOM2 Unit Block Diagram**

## 3.14 MultiCAN Module

The MultiCAN module contains independently operating CAN nodes with Full-CAN functionality which are able to exchange Data and Remote Frames using a gateway function. Transmission and reception of CAN frames is handled in accordance with CAN specification V2.0 B (active). Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

All CAN nodes share a common set of message objects. Each message object can be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects can be combined to build gateways between the CAN nodes or to set up a FIFO buffer.

*Note: The number of CAN nodes and message objects depends on the selected device type.*

The message objects are organized in double-chained linked lists, where each CAN node has its own list of message objects. A CAN node stores frames only into message objects that are allocated to its own message object list and it transmits only messages belonging to this message object list. A powerful, command-driven list controller performs all message object list operations.

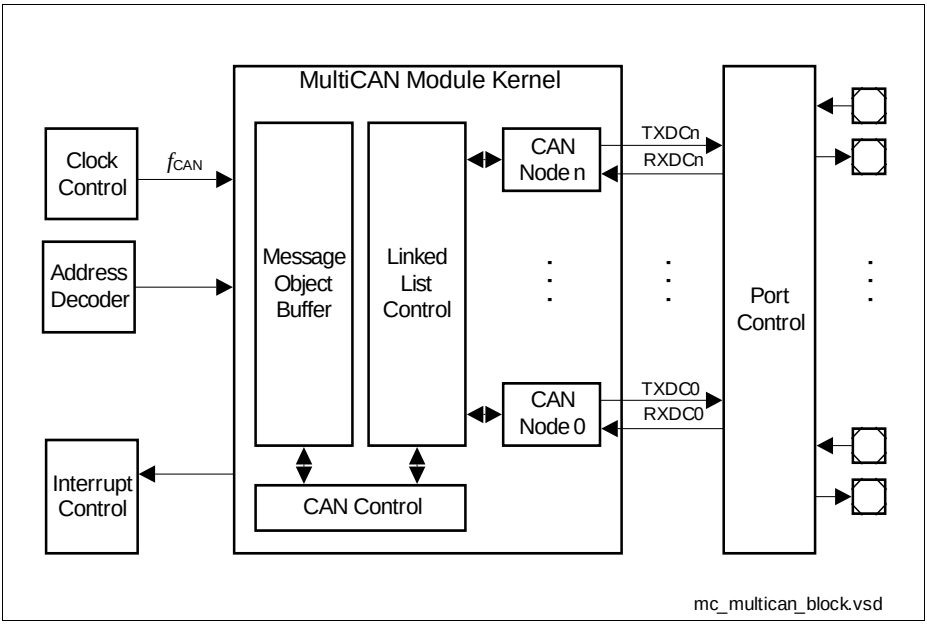


**Figure 12 Block Diagram of MultiCAN Module**

**Table 17 ADC Parameters** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Broken wire detection delay against VAGND[2] | $t_{BWG}$ CC | – | – | 50 | [3] | |
| Broken wire detection delay against VAREF[2] | $t_{BWR}$ CC | – | – | 50 | [4] | |
| Conversion time for 8-bit result[2] | $t_{c8}$ CC | (11 + STC) x $t_{ADCI}$ + 2 x $t_{SYS}$ | | | | |
| Conversion time for 10-bit result[2] | $t_{c10}$ CC | (13 + STC) x $t_{ADCI}$ + 2 x $t_{SYS}$ | | | | |
| Total Unadjusted Error | \|TUE\| CC | – | 1 | 2 | LSB | [5] |
| Wakeup time from analog powerdown, fast mode[2] | $t_{WAF}$ CC | – | – | 4 | µs | |
| Wakeup time from analog powerdown, slow mode[2] | $t_{WAS}$ CC | – | – | 15 | µs | |
| Analog reference ground | $V_{AGND}$ SR | $V_{SS}$ - 0.05 | – | 1.5 | V | |
| Analog input voltage range | $V_{AIN}$ SR | $V_{AGND}$ | – | $V_{AREF}$ | V | [6] |
| Analog reference voltage | $V_{AREF}$ SR | $V_{AGND}$ + 1.0 | – | $V_{DDPA}$ + 0.05 | V | [5] |

1) These parameter values cover the complete operating range. Under relaxed operating conditions (room temperature, nominal supply voltage) the typical values can be used for calculation.

2) This parameter includes the sample time (also the additional sample time specified by STC), the time to determine the digital result and the time to load the result register with the conversion result. Values for the basic clock $t_{ADCI}$ depend on programming.

3) The broken wire detection delay against $V_{AGND}$ is measured in numbers of consecutive precharge cycles at a conversion rate of not more than 500 µs. Result below 10% ($66_H$).

4) The broken wire detection delay against $V_{AREF}$ is measured in numbers of consecutive precharge cycles at a conversion rate of not more than 10 µs. This function is influenced by leakage current, in particular at high temperature. Result above 80% ($332_H$).

5) TUE is tested at $V_{AREF}$ = $V_{DDPA}$ = 5.0 V, $V_{AGND}$ = 0 V. It is verified by design for all other voltages within the defined voltage range. The specified TUE is valid only if the absolute sum of input overload currents on analog port pins (see $I_{OV}$ specification) does not exceed 10 mA, and if $V_{AREF}$ and $V_{AGND}$ remain stable during the measurement time.

6) $V_{AIN}$ may exceed $V_{AGND}$ or $V_{AREF}$ up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

## 4.5 Flash Memory Parameters

The XE167xM is delivered with all Flash sectors erased and with no protection installed.

The data retention time of the XE167xM's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

*Note: These parameters are not subject to production test but verified by design and/or characterization.*

*Note: Operating Conditions apply.*

**Table 22 Flash Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Parallel Flash module program/erase limit depending on Flash read activity | $N_{PP}$ SR | – | – | 4[1] | | $N_{FL\_RD} \leq 1$, $f_{SYS} \leq 80$ MHz |
| | | – | – | 1[2] | | $N_{FL\_RD} > 1$ |
| Flash erase endurance for security pages | $N_{SEC}$ SR | 10 | – | – | cycles | $t_{RET} \geq 20$ years |
| Flash wait states[3] | $N_{WSFLASH}$ SR | 1 | – | – | | $f_{SYS} \leq 8$ MHz |
| | | 2 | – | – | | $f_{SYS} \leq 13$ MHz |
| | | 3 | – | – | | $f_{SYS} \leq 17$ MHz |
| | | 4 | – | – | | $f_{SYS} > 17$ MHz |
| Erase time per sector/page | $t_{ER}$ CC | – | 7[4] | 8.0 | ms | |
| Programming time per page | $t_{PR}$ CC | – | 3[4] | 3.5 | ms | |
| Data retention time | $t_{RET}$ CC | 20 | – | – | years | $N_{Er} \leq 1\,000$ cycles |
| Drain disturb limit | $N_{DD}$ SR | 32 | – | – | cycles | |

### 4.6.3 External Clock Input Parameters

These parameters specify the external clock generation for the XE167xM. The clock can be generated in two ways:

- By connecting a **crystal or ceramic resonator** to pins XTAL1/XTAL2
- By supplying an **external clock signal**
  - This clock signal can be supplied either to pin XTAL1 (core voltage domain) or to pin CLKIN1 (IO voltage domain)

If connected to CLKIN1, the input signal must reach the defined input levels $V_{IL}$ and $V_{IH}$. If connected to XTAL1, a minimum amplitude $V_{AX1}$ (peak-to-peak voltage) is sufficient for the operation of the on-chip oscillator.

*Note: The given clock timing parameters ($t_1$ … $t_4$) are only valid for an external clock input signal.*

*Note: Operating Conditions apply.*

**Table 24 External Clock Input Characteristics**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Oscillator frequency | $f_{OSC}$ SR | 4 | – | 40 | MHz | Input = clock signal |
| | | 4 | – | 16 | MHz | Input = crystal or ceramic resonator |
| XTAL1 input current absolute value | $\|I_{IL}\|$ CC | – | – | 20 | µA | |
| Input clock high time | $t_1$ SR | 6 | – | – | ns | |
| Input clock low time | $t_2$ SR | 6 | – | – | ns | |
| Input clock rise time | $t_3$ SR | – | – | 8 | ns | |
| Input clock fall time | $t_4$ SR | – | – | 8 | ns | |
| Input voltage amplitude on XTAL1[1)] | $V_{AX1}$ SR | 0.3 x $V_{DDIM}$ | – | – | V | 4 to 16 MHz |
| | | 0.4 x $V_{DDIM}$ | – | – | V | 16 to 25 MHz |
| | | 0.5 x $V_{DDIM}$ | – | – | V | 25 to 40 MHz |
| Input voltage range limits for signal on XTAL1 | $V_{IX1}$ SR | -1.7 + $V_{DDIM}$ | – | 1.7 | V | [2)] |

**Table 26** is valid under the following conditions:
$V_{DDP} \geq 3.0$ V; $V_{DDPtyp} = 3.3$ V; $V_{DDP} \leq 4.5$ V; $C_L \geq 20$ pF; $C_L \leq 100$ pF;

**Table 26 Standard Pad Parameters for Lower Voltage Range**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Maximum output driver current (absolute value)[1] | $I_{Omax}$ CC | – | – | 10 | mA | Strong driver |
| | | – | – | 2.5 | mA | Medium driver |
| | | – | – | 0.5 | mA | Weak driver |
| Nominal output driver current (absolute value) | $I_{Onom}$ CC | – | – | 2.5 | mA | Strong driver |
| | | – | – | 1.0 | mA | Medium driver |
| | | – | – | 0.1 | mA | Weak driver |
| Rise and Fall times (10% - 90%) | $t_{RF}$ CC | – | – | 6.2 + 0.24 x $C_L$ | ns | Strong driver; Sharp edge |
| | | – | – | 24 + 0.3 x $C_L$ | ns | Strong driver; Medium edge |
| | | – | – | 34 + 0.3 x $C_L$ | ns | Strong driver; Slow edge |
| | | – | – | 37 + 0.65 x $C_L$ | ns | Medium driver |
| | | – | – | 500 + 2.5 x $C_L$ | ns | Weak driver |

1) The total output current that may be drawn at a given time must be limited to protect the supply rails from damage. For any group of 16 neighboring output pins, the total output current in each direction ($\Sigma I_{OL}$ and $\Sigma I_{OH}$) must remain below 50 mA.

### 4.6.5 External Bus Timing

The following parameters specify the behavior of the XE167xM bus interface.

*Note: These parameters are not subject to production test but verified by design and/or characterization.*

*Note: Operating Conditions apply.*

**Bus Interface Performance Limits**

The output frequency at the bus interface pins is limited by the performance of the output drivers. The fast clock driver (used for CLKOUT) can drive 80-MHz signals, the standard drivers can drive 40-MHz signals
Therefore, the speed of the EBC must be limited, either by limiting the system frequency to $f_{SYS} \leq 80$ MHz or by adding waitstates so that signal transitions have a minimum distance of 12.5 ns.
For a description of the bus protocol and the programming of its variable timing parameters, please refer to the User's Manual.

**Table 27 EBC Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| CLKOUT Cycle Time[1)] | $t_5$ CC | – | 1 / $f_{SYS}$ | – | ns | |
| CLKOUT high time | $t_6$ CC | 2 | – | – | | |
| CLKOUT low time | $t_7$ CC | 2 | – | – | | |
| CLKOUT rise time | $t_8$ CC | – | – | 3 | ns | |
| CLKOUT fall time | $t_9$ CC | – | – | 3 | | |

1) The CLKOUT cycle time is influenced by PLL jitter. For longer periods the relative deviation decreases (see PLL deviation formula).

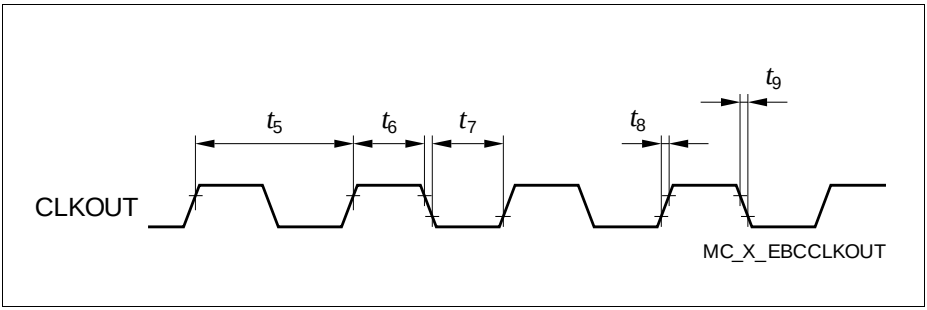


**Figure 22 CLKOUT Signal Timing**

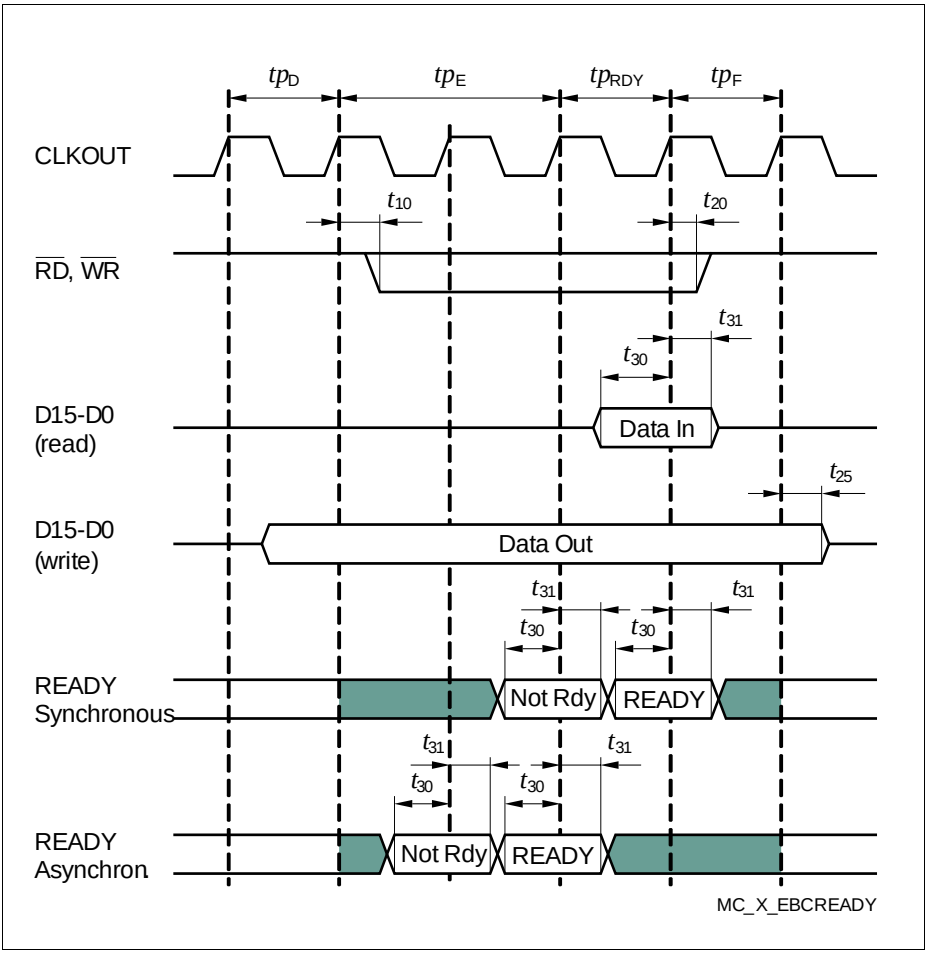


**Figure 25 READY Timing**

*Note: If the READY input is sampled inactive at the indicated sampling point (“Not Rdy”) a READY-controlled waitstate is inserted (tpRDY),*
*sampling the READY input active at the indicated sampling point (“Ready”) terminates the currently running bus cycle.*
*Note the different sampling points for synchronous and asynchronous READY.*
*This example uses one mandatory waitstate (see tpE) before the READY input value is used.*

### 4.6.6 Synchronous Serial Interface Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

*Note: These parameters are not subject to production test but verified by design and/or characterization.*

*Note: Operating Conditions apply; $C_L$ = 20 pF.*

**Table 33 USIC SSC Master Mode Timing for Upper Voltage Range**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Slave select output SELO active to first SCLKOUT transmit edge | $t_1$ CC | $t_{SYS}$ - 8 [1] | – | – | ns | |
| Slave select output SELO inactive after last SCLKOUT receive edge | $t_2$ CC | $t_{SYS}$ - 6 [1] | – | – | ns | |
| Data output DOUT valid time | $t_3$ CC | -6 | – | 9 | ns | |
| Receive data input setup time to SCLKOUT receive edge | $t_4$ SR | 31 | – | – | ns | |
| Data input DX0 hold time from SCLKOUT receive edge | $t_5$ SR | -4 | – | – | ns | |

1) $t_{SYS} = 1 / f_{SYS}$

**Table 34 USIC SSC Master Mode Timing for Lower Voltage Range**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Slave select output SELO active to first SCLKOUT transmit edge | $t_1$ CC | $t_{SYS}$ - 10 [1] | – | – | ns | |
| Slave select output SELO inactive after last SCLKOUT receive edge | $t_2$ CC | $t_{SYS}$ - 9 [1] | – | – | ns | |
| Data output DOUT valid time | $t_3$ CC | -7 | – | 11 | ns | |

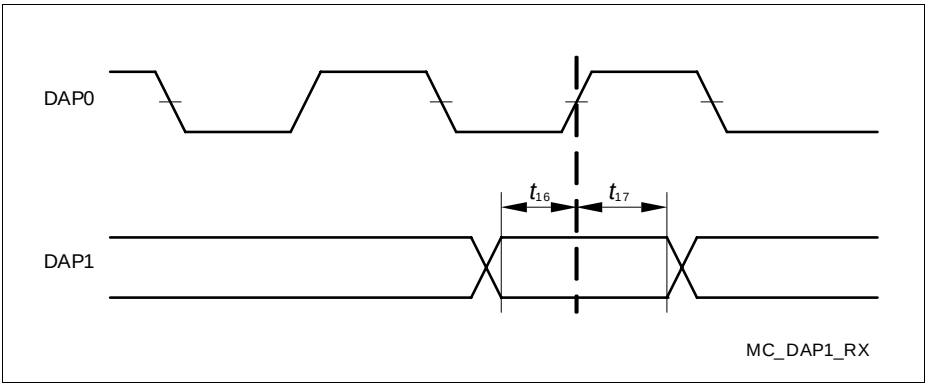


**Figure 30 DAP Timing Host to Device**

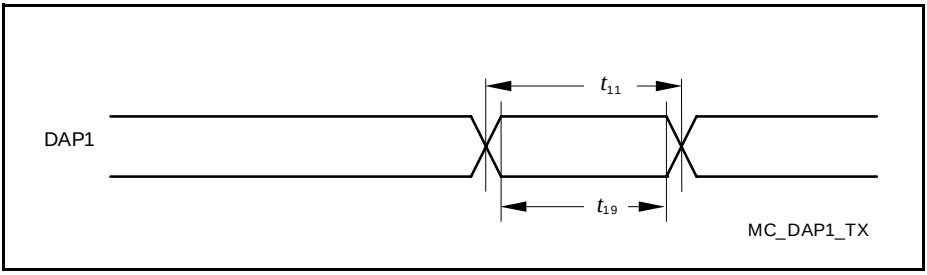


**Figure 31 DAP Timing Device to Host**

*Note: The transmission timing is determined by the receiving debugger by evaluating the sync-request synchronization pattern telegram.*