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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | C166SV2 |
| Core Size | 16-Bit |
| Speed | 80MHz |
| Connectivity | CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI |
| Peripherals | I²S, POR, PWM, WDT |
| Number of I/O | 119 |
| Program Memory Size | 576KB (576K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 50K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 24x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP Exposed Pad |
| Supplier Device Package | PG-LQFP-144-4 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/xe167fm72f80laakxqma1 |

**Table 5 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 5 | P8.4 | O0 / I | St/B | **Bit 4 of Port 8, General Purpose Input/Output** |
| | CCU60_COUT61 | O1 | St/B | **CCU60 Channel 1 Output** |
| | CCU62_CC61 | O2 | St/B | **CCU62 Channel 1 Output** |
| | TMS_D | IH | St/B | **JTAG Test Mode Selection Input**<br>If JTAG pos. D is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it. |
| | CCU62_CC61INB | I | St/B | **CCU62 Channel 1 Input** |
| 6 | $\overline{\text{TRST}}$ | I | In/B | **Test-System Reset Input**<br>For normal system operation, pin $\overline{\text{TRST}}$ should be held low. A high level at this pin at the rising edge of $\overline{\text{PORST}}$ activates the XE167xM's debug system. In this case, pin $\overline{\text{TRST}}$ must be driven low once to reset the debug system.<br>An internal pull-down device will hold this pin low when nothing is driving it. |
| 7 | P8.3 | O0 / I | St/B | **Bit 3 of Port 8, General Purpose Input/Output** |
| | CCU60_COUT60 | O1 | St/B | **CCU60 Channel 0 Output** |
| | CCU62_CC60 | O2 | St/B | **CCU62 Channel 0 Output** |
| | TDI_D | IH | St/B | **JTAG Test Data Input**<br>If JTAG pos. D is selected during start-up, an internal pull-up device will hold this pin low when nothing is driving it. |
| | CCU62_CC60INB | I | St/B | **CCU62 Channel 0 Input** |

**Table 5 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 63 | P4.1 | O0 / I | St/B | **Bit 1 of Port 4, General Purpose Input/Output** |
| | U3C0_SELO 3 | O1 | St/B | **USIC3 Channel Select/Control 3 Output** |
| | TxDC2 | O2 | St/B | **CAN Node 2 Transmit Data Output** |
| | CC2_CC25 | O3 / I | St/B | **CAPCOM2 CC25IO Capture Inp./ Compare Out.** |
| | $\overline{CS1}$ | OH | St/B | **External Bus Interface Chip Select 1 Output** |
| | CCU62_CCP OS0B | I | St/B | **CCU62 Position Input 0** |
| | T4EUDB | I | St/B | **GPT12E Timer T4 External Up/Down Control Input** |
| | ESR1_8 | I | St/B | **ESR1 Trigger Input 8** |
| 64 | P2.4 | O0 / I | St/B | **Bit 4 of Port 2, General Purpose Input/Output** |
| | U0C1_DOUT | O1 | St/B | **USIC0 Channel 1 Shift Data Output** |
| | TxDC0 | O2 | St/B | **CAN Node 0 Transmit Data Output** |
| | CC2_CC17 | O3 / I | St/B | **CAPCOM2 CC17IO Capture Inp./ Compare Out.** |
| | A17 | OH | St/B | **External Bus Interface Address Line 17** |
| | ESR1_0 | I | St/B | **ESR1 Trigger Input 0** |
| | U0C0_DX0F | I | St/B | **USIC0 Channel 0 Shift Data Input** |
| | RxDC1A | I | St/B | **CAN Node 1 Receive Data Input** |
| 65 | P11.1 | O0 / I | St/B | **Bit 1 of Port 11, General Purpose Input/Output** |
| | CCU61_COU T61 | O1 | St/B | **CCU61 Channel 1 Output** |
| | TxDC0 | O2 | St/B | **CAN Node 0 Transmit Data Output** |
| | U3C1_SELO 0 | O3 | St/B | **USIC3 Channel 1 Select/Control 0 Output** |
| | CCU63_CCP OS1A | I | St/B | **CCU63 Position Input 1** |
| | CCU61_CTR APD | I | St/B | **CCU61 Emergency Trap Input** |
| | U3C1_DX2A | I | St/B | **USIC3 Channel 1 Shift Control Input** |

**Table 5 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 117 | P10.10 | O0 / I | St/B | **Bit 10 of Port 10, General Purpose Input/Output** |
| | U0C0_SELO 0 | O1 | St/B | **USIC0 Channel 0 Select/Control 0 Output** |
| | CCU60_COU T63 | O2 | St/B | **CCU60 Channel 3 Output** |
| | AD10 | OH / IH | St/B | **External Bus Interface Address/Data Line 10** |
| | U0C0_DX2C | I | St/B | **USIC0 Channel 0 Shift Control Input** |
| | U0C1_DX1A | I | St/B | **USIC0 Channel 1 Shift Clock Input** |
| | TDI_B | IH | St/B | **JTAG Test Data Input**<br>If JTAG pos. B is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it. |
| 118 | P10.11 | O0 / I | St/B | **Bit 11 of Port 10, General Purpose Input/Output** |
| | U1C0_SCLK OUT | O1 | St/B | **USIC1 Channel 0 Shift Clock Output** |
| | $\overline{\text{BRKOUT}}$ | O2 | St/B | **OCDS Break Signal Output** |
| | U3C0_SELO 0 | O3 | St/B | **USIC3 Channel 0 Select/Control 0 Output** |
| | AD11 | OH / IH | St/B | **External Bus Interface Address/Data Line 11** |
| | U1C0_DX1D | I | St/B | **USIC1 Channel 0 Shift Clock Input** |
| | RxDC2B | I | St/B | **CAN Node 2 Receive Data Input** |
| | TMS_B | IH | St/B | **JTAG Test Mode Selection Input**<br>If JTAG pos. B is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it. |
| | U3C0_DX2A | I | St/B | **USIC3 Channel 0 Shift Control Input** |
| 119 | P9.2 | O0 / I | St/B | **Bit 2 of Port 9, General Purpose Input/Output** |
| | CCU63_CC6 2 | O1 | St/B | **CCU63 Channel 2 Output** |
| | CCU63_CC6 2INA | I | St/B | **CCU63 Channel 2 Input** |
| | CAPINB | I | St/B | **GPT12E Register CAPREL Capture Input** |

## 3.1 Memory Subsystem and Organization

The memory space of the XE167xM is configured in the von Neumann architecture. In this architecture all internal and external resources, including code memory, data memory, registers and I/O ports, are organized in the same linear address space.

**Table 7 XE167xM Memory Map [1)]**

| Address Area | Start Loc. | End Loc. | Area Size[2)] | Notes |
|---|---|---|---|---|
| IMB register space | FF'FF00$_H$ | FF'FFFF$_H$ | 256 Bytes | – |
| Reserved (Access trap) | F0'0000$_H$ | FF'FEFF$_H$ | <1 Mbyte | Minus IMB registers |
| Reserved for EPSRAM | E8'8000$_H$ | EF'FFFF$_H$ | 480 Kbytes | Mirrors EPSRAM |
| Emulated PSRAM | E8'0000$_H$ | E8'7FFF$_H$ | 32 Kbytes | With Flash timing |
| Reserved for PSRAM | E0'8000$_H$ | E7'FFFF$_H$ | 480 Kbytes | Mirrors PSRAM |
| Program SRAM | E0'0000$_H$ | E0'7FFF$_H$ | 32 Kbytes | Maximum speed |
| Reserved for Flash | CD'0000$_H$ | DF'FFFF$_H$ | <1.25 Mbytes | – |
| Program Flash 3 | CC'0000$_H$ | CC'FFFF$_H$ | 64 Kbytes | – |
| Program Flash 2 | C8'0000$_H$ | CB'FFFF$_H$ | 256 Kbytes | – |
| Program Flash 1 | C4'0000$_H$ | C7'FFFF$_H$ | 256 Kbytes | – |
| Program Flash 0 | C0'0000$_H$ | C3'FFFF$_H$ | 256 Kbytes | [3)] |
| External memory area | 40'0000$_H$ | BF'FFFF$_H$ | 8 Mbytes | – |
| Available Ext. IO area[4)] | 21'0000$_H$ | 3F'FFFF$_H$ | < 2 Mbytes | Minus USIC/CAN |
| Reserved | 20'BC00$_H$ | 20'FFFF$_H$ | 17 Kbytes | – |
| USIC alternate regs. | 20'B000$_H$ | 20'BFFF$_H$ | 4 Kbytes | Accessed via EBC |
| MultiCAN alternate regs. | 20'8000$_H$ | 20'AFFF$_H$ | 12 Kbytes | Accessed via EBC |
| Reserved | 20'6000$_H$ | 20'7FFF$_H$ | 8 Kbytes | – |
| USIC registers | 20'4000$_H$ | 20'5FFF$_H$ | 8 Kbytes | Accessed via EBC |
| MultiCAN registers | 20'0000$_H$ | 20'3FFF$_H$ | 16 Kbytes | Accessed via EBC |
| External memory area | 01'0000$_H$ | 1F'FFFF$_H$ | < 2 Mbytes | Minus segment 0 |
| SFR area | 00'FE00$_H$ | 00'FFFF$_H$ | 0.5 Kbyte | – |
| Dual-Port RAM | 00'F600$_H$ | 00'FDFF$_H$ | 2 Kbytes | – |
| Reserved for DPRAM | 00'F200$_H$ | 00'F5FF$_H$ | 1 Kbyte | – |
| ESFR area | 00'F000$_H$ | 00'F1FF$_H$ | 0.5 Kbyte | – |
| XSFR area | 00'E000$_H$ | 00'EFFF$_H$ | 4 Kbytes | – |

With its maximum resolution of 2 system clock cycles, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The counting direction (up/down) for each timer can be programmed by software or altered dynamically with an external signal on a port pin (TxEUD). Concatenation of the timers is supported with the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can also be used to clock the CAPCOM2 timers and to initiate a reload from the CAPREL register.

The CAPREL register can capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN); timer T5 may optionally be cleared after the capture procedure. This allows the XE167xM to measure absolute time differences or to perform pulse multiplication without software overhead.

The capture trigger (timer T5 to CAPREL) can also be generated upon transitions of GPT1 timer T3 inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.

## 3.11 Real Time Clock

The Real Time Clock (RTC) module of the XE167xM can be clocked with a clock signal selected from internal sources or external sources (pins).

The RTC basically consists of a chain of divider blocks:

- Selectable 32:1 and 8:1 dividers (on - off)
- The reloadable 16-bit timer T14
- The 32-bit RTC timer block (accessible via registers RTCH and RTCL) consisting of:
  – a reloadable 10-bit timer
  – a reloadable 6-bit timer
  – a reloadable 6-bit timer
  – a reloadable 10-bit timer

All timers count up. Each timer can generate an interrupt request. All requests are combined to a common node request.

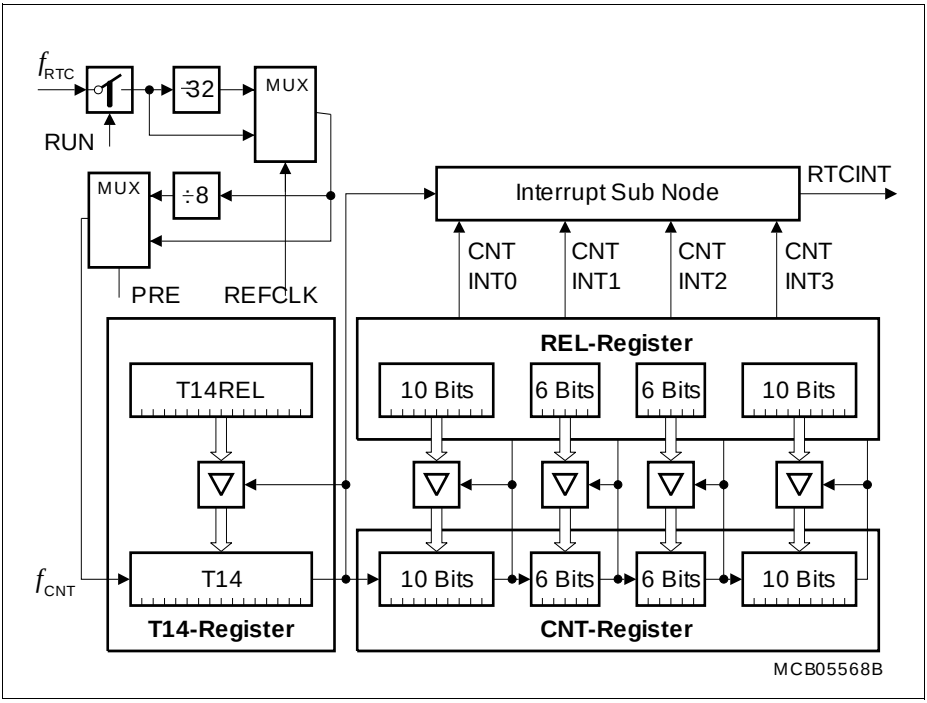


**Figure 10 RTC Block Diagram**

*Note: The registers associated with the RTC are only affected by a power reset.*

**Table 10 Instruction Set Summary** (cont'd)

| Mnemonic | Description | Bytes |
|---|---|---|
| ROL/ROR | Rotate left/right direct word GPR | 2 |
| ASHR | Arithmetic (sign bit) shift right direct word GPR | 2 |
| MOV(B) | Move word (byte) data | 2 / 4 |
| MOVBS/Z | Move byte operand to word op. with sign/zero extension | 2 / 4 |
| JMPA/I/R | Jump absolute/indirect/relative if condition is met | 4 |
| JMPS | Jump absolute to a code segment | 4 |
| JB(C) | Jump relative if direct bit is set (and clear bit) | 4 |
| JNB(S) | Jump relative if direct bit is not set (and set bit) | 4 |
| CALLA/I/R | Call absolute/indirect/relative subroutine if condition is met | 4 |
| CALLS | Call absolute subroutine in any code segment | 4 |
| PCALL | Push direct word register onto system stack and call absolute subroutine | 4 |
| TRAP | Call interrupt service routine via immediate trap number | 2 |
| PUSH/POP | Push/pop direct word register onto/from system stack | 2 |
| SCXT | Push direct word register onto system stack and update register with word operand | 4 |
| RET(P) | Return from intra-segment subroutine (and pop direct word register from system stack) | 2 |
| RETS | Return from inter-segment subroutine | 2 |
| RETI | Return from interrupt service subroutine | 2 |
| SBRK | Software Break | 2 |
| SRST | Software Reset | 4 |
| IDLE | Enter Idle Mode | 4 |
| PWRDN | Unused instruction[1)] | 4 |
| SRVWDT | Service Watchdog Timer | 4 |
| DISWDT/ENWDT | Disable/Enable Watchdog Timer | 4 |
| EINIT | End-of-Initialization Register Lock | 4 |
| ATOMIC | Begin ATOMIC sequence | 2 |
| EXTR | Begin EXTended Register sequence | 2 |
| EXTP(R) | Begin EXTended Page (and Register) sequence | 2 / 4 |
| EXTS(R) | Begin EXTended Segment (and Register) sequence | 2 / 4 |

# 4 Electrical Parameters

The operating range for the XE167xM is defined by its electrical parameters. For proper operation the specified limits must be respected when integrating the device in its target environment.

## 4.1 General Parameters

These parameters are valid for all subsequent descriptions, unless otherwise noted.

### 4.1.1 Absolut Maximum Rating Conditions

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for an extended time may affect device reliability.
During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < V_{SS}$) the voltage on $V_{DDP}$ pins with respect to ground ($V_{SS}$) must not exceed the values defined by the absolute maximum ratings.

**Table 11 Absolute Maximum Rating Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output current on a pin when high value is driven | $I_{OH}$ SR | -30 | – | – | mA | |
| Output current on a pin when low value is driven | $I_{OL}$ SR | – | – | 30 | mA | |
| Overload current | $I_{OV}$ SR | -10 | – | 10 | mA | 1) |
| Absolute sum of overload currents | $\Sigma\lvert I_{OV}\rvert$ SR | – | – | 100 | mA | 1) |
| Junction Temperature | $T_J$ SR | -40 | – | 150 | °C | |
| Storage Temperature | $T_{ST}$ SR | -65 | – | 150 | °C | |
| Digital supply voltage for IO pads and voltage regulators | $V_{DDPA}$, $V_{DDPB}$ SR | -0.5 | – | 6.0 | V | |
| Voltage on any pin with respect to ground (Vss) | $V_{IN}$ SR | -0.5 | – | $V_{DDP}$ + 0.5 | V | $V_{IN} \le V_{DDP(max)}$ |

1) Overload condition occurs if the input voltage $V_{IN}$ is out of the absolute maximum rating range. In this case the current must be limited to the listed values by design measures.

### 4.2.2 DC Parameters for Lower Voltage Area

Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current $I_{OV}$.

*Note: Operating Conditions apply.*

**Table 14** is valid under the following conditions:
$V_{DDP} \geq 3.0$ V; $V_{DDPtyp} = 3.3$ V; $V_{DDP} \leq 4.5$ V

**Table 14 DC Characteristics for Lower Voltage Range**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Pin capacitance (digital inputs/outputs). To be doubled for double bond pins.[1)] | $C_{IO}$ CC | – | – | 10 | pF | not subject to production test |
| Input Hysteresis[2)] | HYS CC | 0.07 x $V_{DDP}$ | – | – | V | $R_S$ = 0 Ohm |
| Absolute input leakage current on pins of analog ports[3)] | $\|I_{OZ1}\|$ CC | – | 10 | 200 | nA | $V_{IN} > V_{SS}$; $V_{IN} < V_{DDP}$ |
| Absolute input leakage current for all other pins. To be doubled for double bond pins.[3)1)4)] | $\|I_{OZ2}\|$ CC | – | 0.2 | 2.5 | µA | $T_J \leq 110$ °C; $V_{IN} < V_{DDP}$; $V_{IN} > V_{SS}$ |
| | | – | 0.2 | 8 | µA | $T_J \leq 150$ °C; $V_{IN} < V_{DDP}$; $V_{IN} > V_{SS}$ |
| Pull Level Force Current[5)] | $\|I_{PLF}\|$ SR | 150 | – | – | | [6)] |
| Pull Level Keep Current[7)] | $\|I_{PLK}\|$ SR | – | – | 10 | µA | [6)] |
| Input high voltage (all except XTAL1) | $V_{IH}$ SR | 0.7 x $V_{DDP}$ | – | $V_{DDP}$ + 0.3 | V | |
| Input low voltage (all except XTAL1) | $V_{IL}$ SR | -0.3 | – | 0.3 x $V_{DDP}$ | V | |
| Output High voltage[8)] | $V_{OH}$ CC | $V_{DDP}$ - 1.0 | – | – | V | $I_{OH} \geq I_{OHmax}$ |
| | | $V_{DDP}$ - 0.4 | – | – | V | $I_{OH} \geq I_{OHnom}$[9)] |

### 4.2.3 Power Consumption

The power consumed by the XE167xM depends on several factors such as supply voltage, operating frequency, active circuits, and operating temperature. The power consumption specified here consists of two components:

- The switching current $I_S$ depends on the device activity
- The leakage current $I_{LK}$ depends on the device temperature

To determine the actual power consumption, always both components, switching current $I_S$ and leakage current $I_{LK}$ must be added:

$I_{DDP} = I_S + I_{LK}$.

*Note: The power consumption values are not subject to production test. They are verified by design/characterization.*
*To determine the total power consumption for dimensioning the external power supply, also the pad driver currents must be considered.*

The given power consumption parameters and their values refer to specific operating conditions:

- **Active mode**:
  Regular operation, i.e. peripherals are active, code execution out of Flash.
- **Stopover mode**:
  Crystal oscillator and PLL stopped, Flash switched off, clock in domain DMP_1 stopped.

*Note: The maximum values cover the complete specified operating range of all manufactured devices.*
*The typical values refer to average devices under typical conditions, such as nominal supply voltage, room temperature, application-oriented activity.*
*After a power reset, the decoupling capacitors for $V_{DDIM}$ and $V_{DDI1}$ are charged with the maximum possible current.*

For additional information, please refer to **Section 5.2**, **Thermal Considerations**.

*Note: Operating Conditions apply.*

**Table 15 Switching Power Consumption**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Power supply current (active) with all peripherals active and EVVRs on | $I_{SACT}$ CC | – | 10 + 0.6 x $f_{SYS}$ [1)] | 10 + 1.0 x $f_{SYS}$ [1)] | mA | 2)3) |
| Power supply current in stopover mode, EVVRs on | $I_{SSO}$ CC | – | 0.7 | 2.0 | mA | |

1) $f_{SYS}$ in MHz.

3) $f_{WU}$ in MHz
4) This value includes a hysteresis of approximately 50 mV for rising voltage.
5) $V_{LV}$ = selected SWD voltage level
6) The limit $V_{LV}$ - 0.10 V is valid for the OK1 level. The limit for the OK2 level is $V_{LV}$ - 0.15 V.

### Conditions for $t_{SPO}$ Timing Measurement

The time required for the transition from **Power-On** to **Base** mode is called $t_{SPO}$. It is measured under the following conditions:

Precondition: The pad supply is valid, i.e. $V_{DDPB}$ is above 3.0 V and remains above 3.0 V even though the XE167xM is starting up. No debugger is attached.

Start condition: Power-on reset is removed ($\overline{\text{PORST}}$ = 1).

End condition: External pin toggle caused by first user instruction executed from FLASH after startup.

### Conditions for $t_{SSO}$ Timing Measurement

The time required for the transition from **Stopover** to **Stopover Waked-Up** mode is called $t_{SSO}$. It is measured under the following conditions:

Precondition: The **Stopover** mode has been entered using the procedure defined in the Programmer's Guide.

Start condition: Pin toggle on $\overline{\text{ESR}}$ pin triggering the startup sequence.

End condition: External pin toggle caused by first user instruction executed from PSRAM after startup.

### Coding of bit fields LEVxV in SWD and PVC Configuration Registers

**Table 20 Coding of bit fields LEVxV in Register SWDCON0**

| Code | Default Voltage Level | Notes[1)] |
|---|---|---|
| $0000_B$ | 2.9 V | |
| $0001_B$ | 3.0 V | LEV1V: reset request |
| $0010_B$ | 3.1 V | |
| $0011_B$ | 3.2 V | |
| $0100_B$ | 3.3 V | |
| $0101_B$ | 3.4 V | |
| $0110_B$ | 3.6 V | |
| $0111_B$ | 4.0 V | |
| $1000_B$ | 4.2 V | |

## 4.5 Flash Memory Parameters

The XE167xM is delivered with all Flash sectors erased and with no protection installed.

The data retention time of the XE167xM's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

*Note: These parameters are not subject to production test but verified by design and/or characterization.*

*Note: Operating Conditions apply.*

**Table 22 Flash Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Parallel Flash module program/erase limit depending on Flash read activity | $N_{PP}$ SR | – | – | 4[1] | | $N_{FL\_RD} \leq 1$, $f_{SYS} \leq 80$ MHz |
| | | – | – | 1[2] | | $N_{FL\_RD} > 1$ |
| Flash erase endurance for security pages | $N_{SEC}$ SR | 10 | – | – | cycles | $t_{RET} \geq 20$ years |
| Flash wait states[3] | $N_{WSFLASH}$ SR | 1 | – | – | | $f_{SYS} \leq 8$ MHz |
| | | 2 | – | – | | $f_{SYS} \leq 13$ MHz |
| | | 3 | – | – | | $f_{SYS} \leq 17$ MHz |
| | | 4 | – | – | | $f_{SYS} > 17$ MHz |
| Erase time per sector/page | $t_{ER}$ CC | – | 7[4] | 8.0 | ms | |
| Programming time per page | $t_{PR}$ CC | – | 3[4] | 3.5 | ms | |
| Data retention time | $t_{RET}$ CC | 20 | – | – | years | $N_{Er} \leq 1\,000$ cycles |
| Drain disturb limit | $N_{DD}$ SR | 32 | – | – | cycles | |

## 4.6 AC Parameters

These parameters describe the dynamic behavior of the XE167xM.

### 4.6.1 Testing Waveforms

These values are used for characterization and production testing (except pin XTAL1).

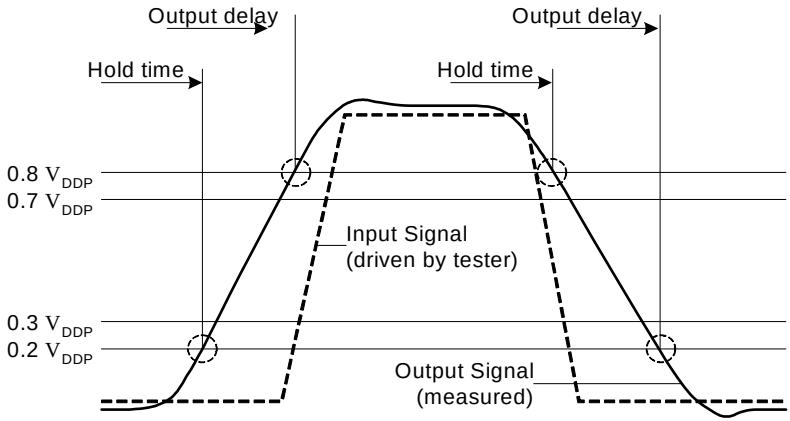


**Figure 17 Input Output Waveforms**

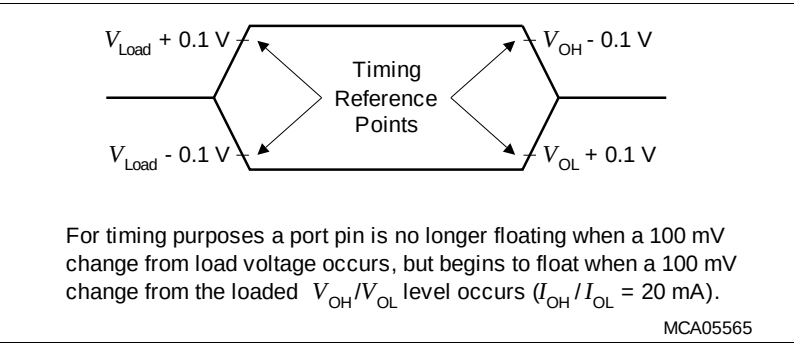


**Figure 18 Floating Waveforms**

**Direct Drive**

When direct drive operation is selected (SYSCON0.CLKSEL = $11_B$), the system clock is derived directly from the input clock signal CLKIN1:

$f_{SYS} = f_{IN}$.

The frequency of $f_{SYS}$ is the same as the frequency of $f_{IN}$. In this case the high and low times of $f_{SYS}$ are determined by the duty cycle of the input clock $f_{IN}$.

Selecting Bypass Operation from the XTAL1[1)] input and using a divider factor of 1 results in a similar configuration.

**Prescaler Operation**

When prescaler operation is selected (SYSCON0.CLKSEL = $10_B$, PLLCON0.VCOBY = $1_B$), the system clock is derived either from the crystal oscillator (input clock signal XTAL1) or from the internal clock source through the output prescaler K1 (= K1DIV+1):

$f_{SYS} = f_{OSC}$ / K1.

If a divider factor of 1 is selected, the frequency of $f_{SYS}$ equals the frequency of $f_{OSC}$. In this case the high and low times of $f_{SYS}$ are determined by the duty cycle of the input clock $f_{OSC}$ (external or internal).

The lowest system clock frequency results from selecting the maximum value for the divider factor K1:

$f_{SYS} = f_{OSC}$ / 1024.

### 4.6.2.1 Phase Locked Loop (PLL)

When PLL operation is selected (SYSCON0.CLKSEL = $10_B$, PLLCON0.VCOBY = $0_B$), the on-chip phase locked loop is enabled and provides the system clock. The PLL multiplies the input frequency by the factor **F** ($f_{SYS} = f_{IN} \times$ **F**).
**F** is calculated from the input divider P (= PDIV+1), the multiplication factor N (= NDIV+1), and the output divider K2 (= K2DIV+1):
(**F** = N / (P $\times$ K2)).

The input clock can be derived either from an external source at XTAL1 or from the on-chip clock source.

The PLL circuit synchronizes the system clock to the input clock. This synchronization is performed smoothly so that the system clock frequency does not change abruptly.

Adjustment to the input clock continuously changes the frequency of $f_{SYS}$ so that it is locked to $f_{IN}$. The slight variation causes a jitter of $f_{SYS}$ which in turn affects the duration of individual TCSs.

1) Voltages on XTAL1 must comply to the core supply voltage $V_{DDIM}$.

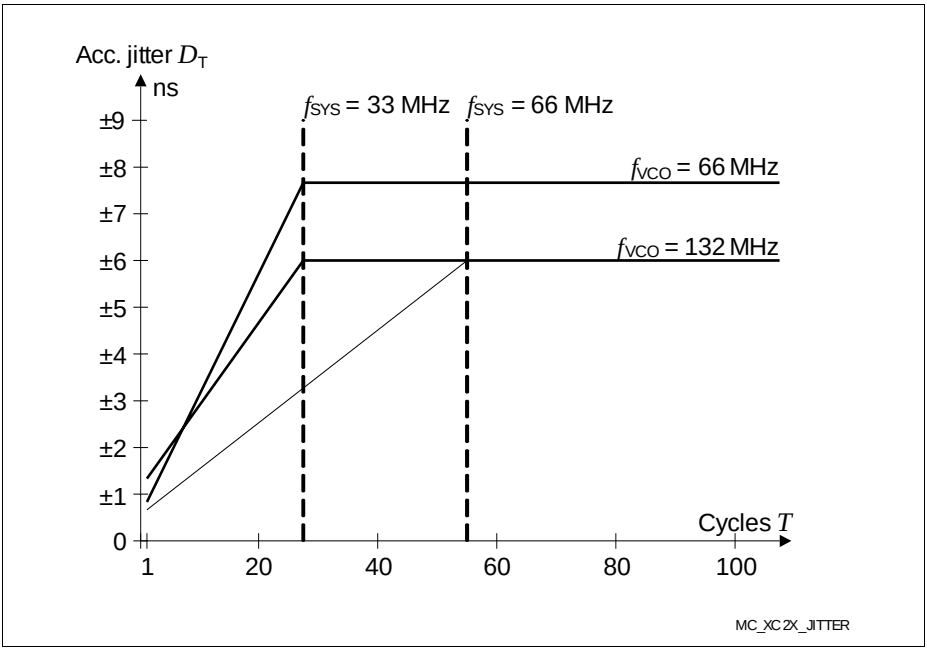


**Figure 20 Approximated Accumulated PLL Jitter**

*Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed $C_L$ = 20 pF.*
*The maximum peak-to-peak noise on the pad supply voltage (measured between $V_{DDPB}$ pin 100 and $V_{SS}$ pin 1) is limited to a peak-to-peak voltage of $V_{PP}$ = 50 mV. This can be achieved by appropriate blocking of the supply voltage as close as possible to the supply pins and using PCB supply and ground planes.*

**Table 26** is valid under the following conditions:
$V_{DDP} \geq 3.0$ V; $V_{DDPtyp} = 3.3$ V; $V_{DDP} \leq 4.5$ V; $C_L \geq 20$ pF; $C_L \leq 100$ pF;

**Table 26 Standard Pad Parameters for Lower Voltage Range**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Maximum output driver current (absolute value)[1] | $I_{Omax}$ CC | – | – | 10 | mA | Strong driver |
| | | – | – | 2.5 | mA | Medium driver |
| | | – | – | 0.5 | mA | Weak driver |
| Nominal output driver current (absolute value) | $I_{Onom}$ CC | – | – | 2.5 | mA | Strong driver |
| | | – | – | 1.0 | mA | Medium driver |
| | | – | – | 0.1 | mA | Weak driver |
| Rise and Fall times (10% - 90%) | $t_{RF}$ CC | – | – | 6.2 + 0.24 x $C_L$ | ns | Strong driver; Sharp edge |
| | | – | – | 24 + 0.3 x $C_L$ | ns | Strong driver; Medium edge |
| | | – | – | 34 + 0.3 x $C_L$ | ns | Strong driver; Slow edge |
| | | – | – | 37 + 0.65 x $C_L$ | ns | Medium driver |
| | | – | – | 500 + 2.5 x $C_L$ | ns | Weak driver |

1) The total output current that may be drawn at a given time must be limited to protect the supply rails from damage. For any group of 16 neighboring output pins, the total output current in each direction ($\Sigma I_{OL}$ and $\Sigma I_{OH}$) must remain below 50 mA.

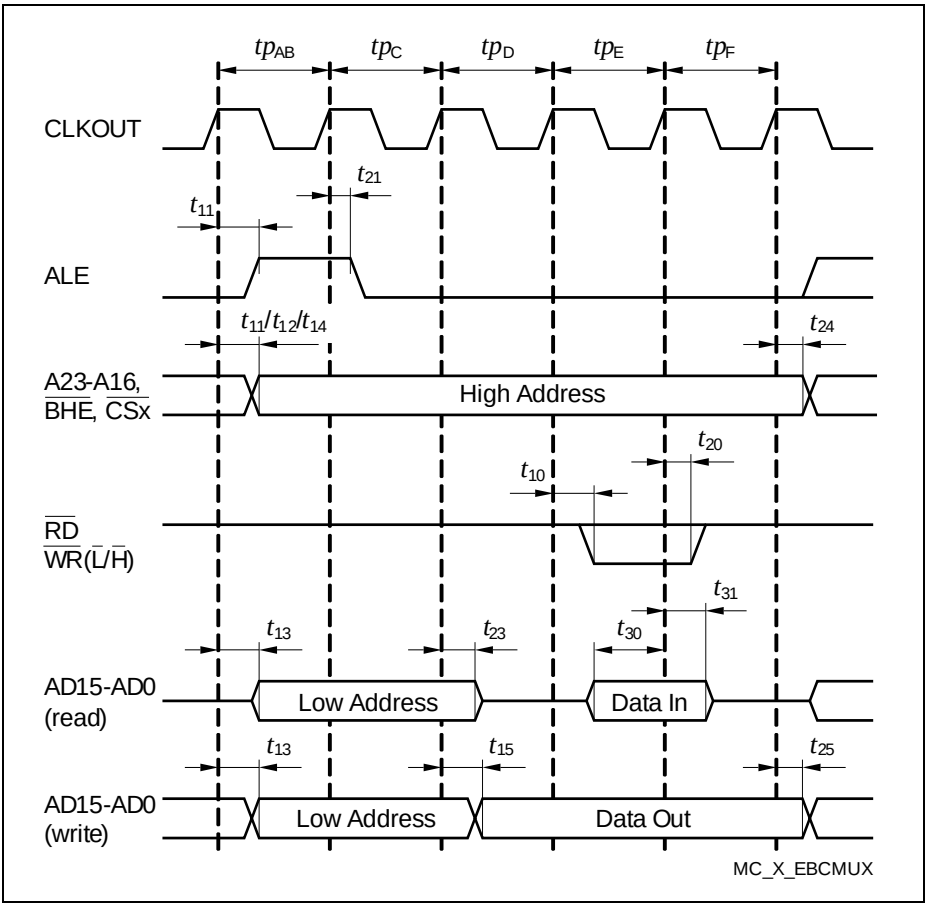


**Figure 23 Multiplexed Bus Cycle**

### 4.6.5.1 Bus Cycle Control with the READY Input

The duration of an external bus cycle can be controlled by the external circuit using the READY input signal. The polarity of this input signal can be selected.

Synchronous READY permits the shortest possible bus cycle but requires the input signal to be synchronous to the reference signal CLKOUT.

An asynchronous READY signal puts no timing constraints on the input signal but incurs a minimum of one waitstate due to the additional synchronization stage. The minimum duration of an asynchronous READY signal for safe synchronization is one CLKOUT period plus the input setup time.

An active READY signal can be deactivated in response to the trailing (rising) edge of the corresponding command ($\overline{RD}$ or $\overline{WR}$).

If the next bus cycle is controlled by READY, an active READY signal must be disabled before the first valid sample point in the next bus cycle. This sample point depends on the programmed phases of the next cycle.

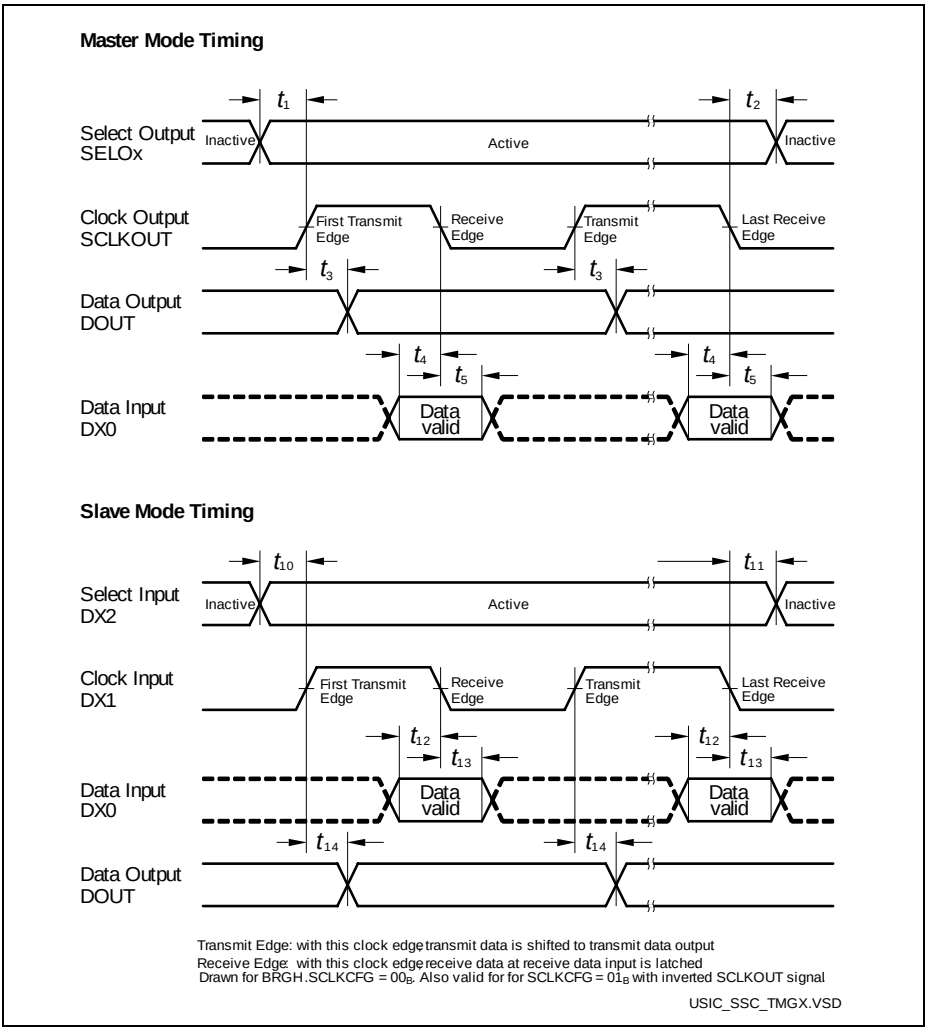


**Figure 28 USIC - SSC Master/Slave Mode Timing**

*Note: This timing diagram shows a standard configuration where the slave select signal is low-active and the serial clock signal is not shifted and not inverted.*

**Table 38 DAP Interface Timing for Lower Voltage Range**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| DAP0 clock period | $t_{11}$ SR | 25[1)] | – | – | ns | |
| DAP0 high time | $t_{12}$ SR | 8 | – | – | ns | |
| DAP0 low time | $t_{13}$ SR | 8 | – | – | ns | |
| DAP0 clock rise time | $t_{14}$ SR | – | – | 4 | ns | |
| DAP0 clock fall time | $t_{15}$ SR | – | – | 4 | ns | |
| DAP1 setup to DAP0 rising edge | $t_{16}$ SR | 6 | – | – | ns | pad_type= standard |
| DAP1 hold after DAP0 rising edge | $t_{17}$ SR | 6 | – | – | ns | pad_type= standard |
| DAP1 valid per DAP0 clock period[2)] | $t_{19}$ CC | 12 | 17 | – | ns | pad_type= standard |

1) The debug interface cannot operate faster than the overall system, therefore $t_{11} \geq t_{SYS}$.

2) The Host has to find a suitable sampling point by analyzing the sync telegram response.

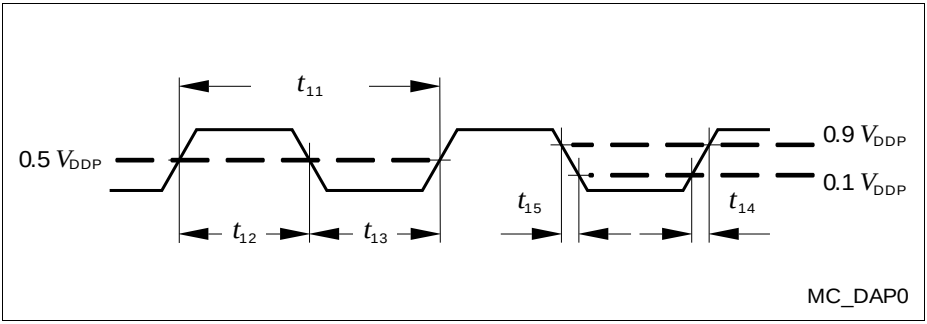


**Figure 29 Test Clock Timing (DAP0)**