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Details

Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I ² S, POR, PWM, WDT
Number of I/O	119
Program Memory Size	576KB (576K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	50K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-144-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xe167fm72f80laakxuma1

Summary of Features

The XE167xM types are offered with several SRAM memory sizes. [Figure 1](#) shows the allocation rules for PSRAM and DSRAM. Note that the rules differ:

- PSRAM allocation starts from the **lower** address
- DSRAM allocation starts from the **higher** address

For example 8 Kbytes of PSRAM will be allocated at E0'0000h-E0'1FFFh and 8 Kbytes of DSRAM will be at 00'C000h-00'DFFFh.

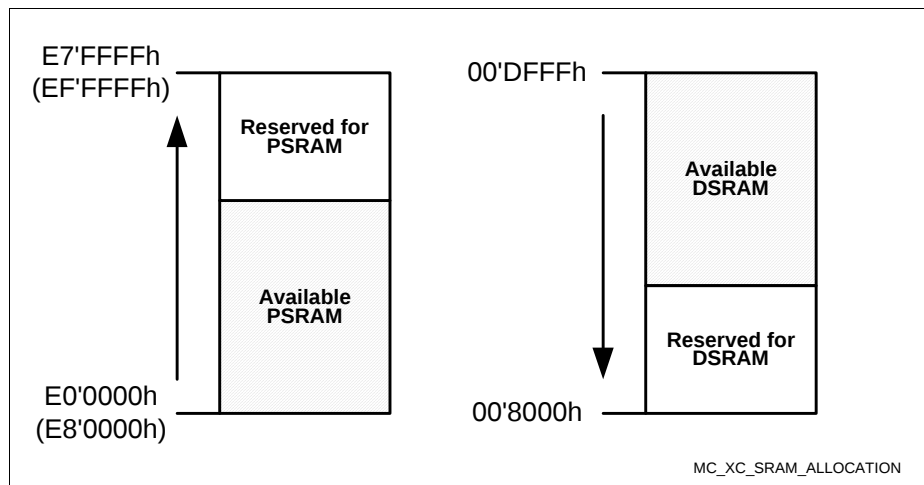


Figure 1 **SRAM Allocation**

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
8	P7.0	O0 / I	St/B	Bit 0 of Port 7, General Purpose Input/Output
	T3OUT	O1	St/B	GPT12E Timer T3 Toggle Latch Output
	T6OUT	O2	St/B	GPT12E Timer T6 Toggle Latch Output
	TDO_A	OH / IH	St/B	JTAG Test Data Output / DAP1 Input/Output If DAP pos. 0 or 2 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	ESR2_1	I	St/B	ESR2 Trigger Input 1
	RxDC4B	I	St/B	CAN Node 4 Receive Data Input
9	P7.3	O0 / I	St/B	Bit 3 of Port 7, General Purpose Input/Output
	EMUX1	O1	St/B	External Analog MUX Control Output 1 (ADC1)
	U0C1_DOUT	O2	St/B	USIC0 Channel 1 Shift Data Output
	U0C0_DOUT	O3	St/B	USIC0 Channel 0 Shift Data Output
	CCU62_CCP OS1A	I	St/B	CCU62 Position Input 1
	TMS_C	IH	St/B	JTAG Test Mode Selection Input If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin low when nothing is driving it.
	U0C1_DX0F	I	St/B	USIC0 Channel 1 Shift Data Input
10	P8.2	O0 / I	St/B	Bit 2 of Port 8, General Purpose Input/Output
	CCU60_CC6 2	O1	St/B	CCU60 Channel 2 Output
	TxDC1	O2	St/B	CAN Node 1 Transmit Data Output
	U1C1_DOUT	O3	St/B	USIC1 Channel 1 Shift Data output
	CCU60_CC6 2INB	I	St/B	CCU60 Channel 2 Input
11	P7.1	O0 / I	St/B	Bit 1 of Port 7, General Purpose Input/Output
	EXTCLK	O1	St/B	Programmable Clock Signal Output
	TXDC4	O2	St/B	CAN Node 4 Transmit Data Output
	CCU62_CTR APA	I	St/B	CCU62 Emergency Trap Input
	BRKIN_C	I	St/B	OCDS Break Signal Input

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
69	P2.6	O0 / I	St/B	Bit 6 of Port 2, General Purpose Input/Output
	U0C0_SELO0	O1	St/B	USIC0 Channel 0 Select/Control 0 Output
	U0C1_SELO1	O2	St/B	USIC0 Channel 1 Select/Control 1 Output
	CC2_CC19	O3 / I	St/B	CAPCOM2 CC19IO Capture Inp./ Compare Out.
	A19	OH	St/B	External Bus Interface Address Line 19
	U0C0_DX2D	I	St/B	USIC0 Channel 0 Shift Control Input
	RxDC0D	I	St/B	CAN Node 0 Receive Data Input
	ESR2_6	I	St/B	ESR2 Trigger Input 6
70	P4.4	O0 / I	St/B	Bit 4 of Port 4, General Purpose Input/Output
	U3C0_SELO2	O1	St/B	USIC3 Channel 0 Select/Control 2 Output
	CC2_CC28	O3 / I	St/B	CAPCOM2 CC28IO Capture Inp./ Compare Out.
	CS4	OH	St/B	External Bus Interface Chip Select 4 Output
	CLKIN2	I	St/B	Clock Signal Input 2
	U3C0_DX2C	I	St/B	USIC3 Channel 0 Shift Control Input
71	P4.3	O0 / I	St/B	Bit 3 of Port 4, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	CC2_CC27	O3 / I	St/B	CAPCOM2 CC27IO Capture Inp./ Compare Out.
	CS3	OH	St/B	External Bus Interface Chip Select 3 Output
	RxDC2A	I	St/B	CAN Node 2 Receive Data Input
	T2EUDA	I	St/B	GPT12E Timer T2 External Up/Down Control Input
	CCU62_CCP OS2B	I	St/B	CCU62 Position Input 2

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
75	P0.0	O0 / I	St/B	Bit 0 of Port 0, General Purpose Input/Output
	U1C0_DOUT	O1	St/B	USIC1 Channel 0 Shift Data Output
	CCU61_CC60	O3	St/B	CCU61 Channel 0 IOutput
	A0	OH	St/B	External Bus Interface Address Line 0
	U1C0_DX0A	I	St/B	USIC1 Channel 0 Shift Data Input
	CCU61_CC60INA	I	St/B	CCU61 Channel 0 Input
	ESR1_11	I	St/B	ESR1 Trigger Input 11
76	P4.5	O0 / I	St/B	Bit 5 of Port 4, General Purpose Input/Output
	U3C0_DOUT	O1	St/B	USIC3 Channel 0 Shift Data Output
	CC2_CC29	O3 / I	St/B	CAPCOM2 CC29IO Capture Inp./Compare Out.
	CCU61_CCP0S0A	I	St/B	CCU61 Position Input 0
	U3C0_DX0B	I	St/B	USIC3 Channel 0 Shift Data Input
	ESR2_10	I	St/B	ESR2 Trigger Input 10
77	P4.6	O0 / I	St/B	Bit 6 of Port 4, General Purpose Input/Output
	U3C0_DOUT	O1	St/B	USIC3 Channel 0 Shift Data Output
	CC2_CC30	O3 / I	St/B	CAPCOM2 CC30IO Capture Inp./ Compare Out.
	T4INA	I	St/B	GPT12E Timer T4 Count/Gate Input
	CCU61_CCP0S1A	I	St/B	CCU61 Position Input 1
78	P2.7	O0 / I	St/B	Bit 7 of Port 2, General Purpose Input/Output
	U0C1_SELO0	O1	St/B	USIC0 Channel 1 Select/Control 0 Output
	U0C0_SELO1	O2	St/B	USIC0 Channel 0 Select/Control 1 Output
	CC2_CC20	O3 / I	St/B	CAPCOM2 CC20IO Capture Inp./ Compare Out.
	A20	OH	St/B	External Bus Interface Address Line 20
	U0C1_DX2C	I	St/B	USIC0 Channel 1 Shift Control Input
	RxDC1C	I	St/B	CAN Node 1 Receive Data Input
	ESR2_7	I	St/B	ESR2 Trigger Input 7

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
84	P10.0	O0 / I	St/B	Bit 0 of Port 10, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	CCU60_CC60	O2	St/B	CCU60 Channel 0 Output
	AD0	OH / IH	St/B	External Bus Interface Address/Data Line 0
	CCU60_CC60INA	I	St/B	CCU60 Channel 0 Input
	ESR1_2	I	St/B	ESR1 Trigger Input 2
	U0C0_DX0A	I	St/B	USIC0 Channel 0 Shift Data Input
	U0C1_DX0A	I	St/B	USIC0 Channel 1 Shift Data Input
85	P3.0	O0 / I	St/B	Bit 0 of Port 3, General Purpose Input/Output
	U2C0_DOUT	O1	St/B	USIC2 Channel 0 Shift Data Output
	BREQ	OH	St/B	External Bus Request Output
	ESR1_1	I	St/B	ESR1 Trigger Input 1
	U2C0_DX0A	I	St/B	USIC2 Channel 0 Shift Data Input
	RxDC3B	I	St/B	CAN Node 3 Receive Data Input
	U2C0_DX1A	I	St/B	USIC2 Channel 0 Shift Clock Input
86	P10.1	O0 / I	St/B	Bit 1 of Port 10, General Purpose Input/Output
	U0C0_DOUT	O1	St/B	USIC0 Channel 0 Shift Data Output
	CCU60_CC61	O2	St/B	CCU60 Channel 1 Output
	AD1	OH / IH	St/B	External Bus Interface Address/Data Line 1
	CCU60_CC61INA	I	St/B	CCU60 Channel 1 Input
	U0C0_DX1A	I	St/B	USIC0 Channel 0 Shift Clock Input
	U0C0_DX0B	I	St/B	USIC0 Channel 0 Shift Data Input

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
87	P0.3	O0 / I	St/B	Bit 3 of Port 0, General Purpose Input/Output
	U1C0_SELO0	O1	St/B	USIC1 Channel 0 Select/Control 0 Output
	U1C1_SELO1	O2	St/B	USIC1 Channel 1 Select/Control 1 Output
	CCU61_COUT60	O3	St/B	CCU61 Channel 0 Output
	A3	OH	St/B	External Bus Interface Address Line 3
	U1C0_DX2A	I	St/B	USIC1 Channel 0 Shift Control Input
	RxDC0B	I	St/B	CAN Node 0 Receive Data Input
88	P3.1	O0 / I	St/B	Bit 1 of Port 3, General Purpose Input/Output
	U2C0_DOUT	O1	St/B	USIC2 Channel 0 Shift Data Output
	TxDC3	O2	St/B	CAN Node 3 Transmit Data Output
	HLDA	OH / IH	St/B	External Bus Hold Acknowledge Output/Input Output in master mode, input in slave mode.
	U2C0_DX0B	I	St/B	USIC2 Channel 0 Shift Data Input
89	P10.2	O0 / I	St/B	Bit 2 of Port 10, General Purpose Input/Output
	U0C0_SCLKOUT	O1	St/B	USIC0 Channel 0 Shift Clock Output
	CCU60_CC62	O2	St/B	CCU60 Channel 2 Output
	U3C0_SELO1	O3	St/B	USIC3 Channel 0 Select/Control 1 Output
	AD2	OH / IH	St/B	External Bus Interface Address/Data Line 2
	CCU60_CC62INA	I	St/B	CCU60 Channel 2 Input
	U0C0_DX1B	I	St/B	USIC0 Channel 0 Shift Clock Input
	U3C0_DX2B	I	St/B	USIC3 Channel 0 Shift Control Input

3.3 Central Processing Unit (CPU)

The core of the CPU consists of a 5-stage execution pipeline with a 2-stage instruction-fetch pipeline, a 16-bit arithmetic and logic unit (ALU), a 32-bit/40-bit multiply and accumulate unit (MAC), a register-file providing three register banks, and dedicated SFRs. The ALU features a multiply-and-divide unit, a bit-mask generator, and a barrel shifter.

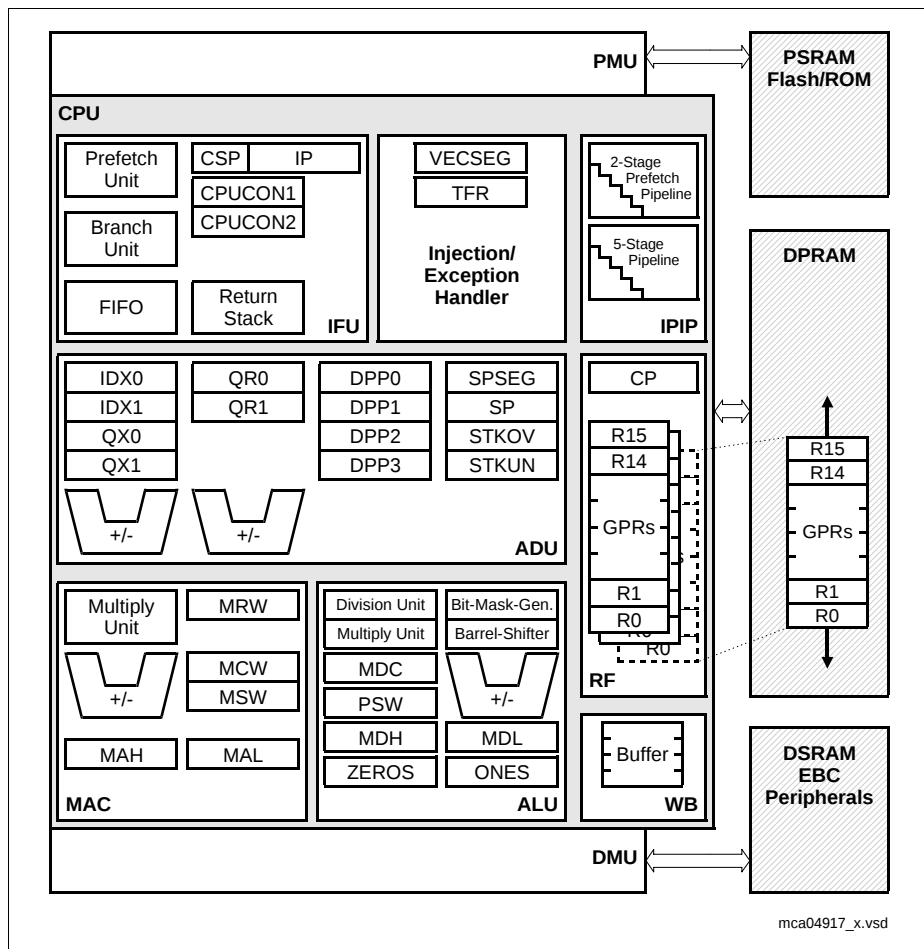


Figure 5 CPU Block Diagram

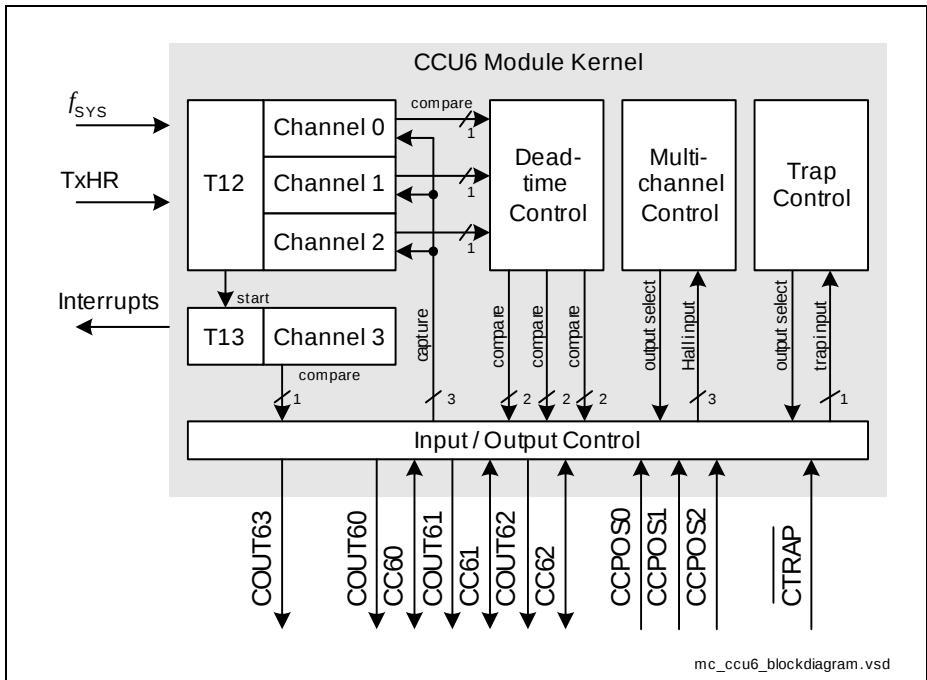


Figure 7 CCU6 Block Diagram

Timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined. Timer T13 can work in compare mode only. The multi-channel control unit generates output patterns that can be modulated by timer T12 and/or timer T13. The modulation sources can be selected and combined for signal modulation.

3.13 Universal Serial Interface Channel Modules (USIC)

The XE167xM features the USIC modules USIC0, USIC1, USIC2, USIC3. Each module provides two serial communication channels.

The Universal Serial Interface Channel (USIC) module is based on a generic data shift and data storage structure which is identical for all supported serial communication protocols. Each channel supports complete full-duplex operation with a basic data buffer structure (one transmit buffer and two receive buffer stages). In addition, the data handling software can use FIFOs.

The protocol part (generation of shift clock/data/control signals) is independent of the general part and is handled by protocol-specific preprocessors (PPPs).

The USIC's input/output lines are connected to pins by a pin routing unit. The inputs and outputs of each USIC channel can be assigned to different interface pins, providing great flexibility to the application software. All assignments can be made during runtime.

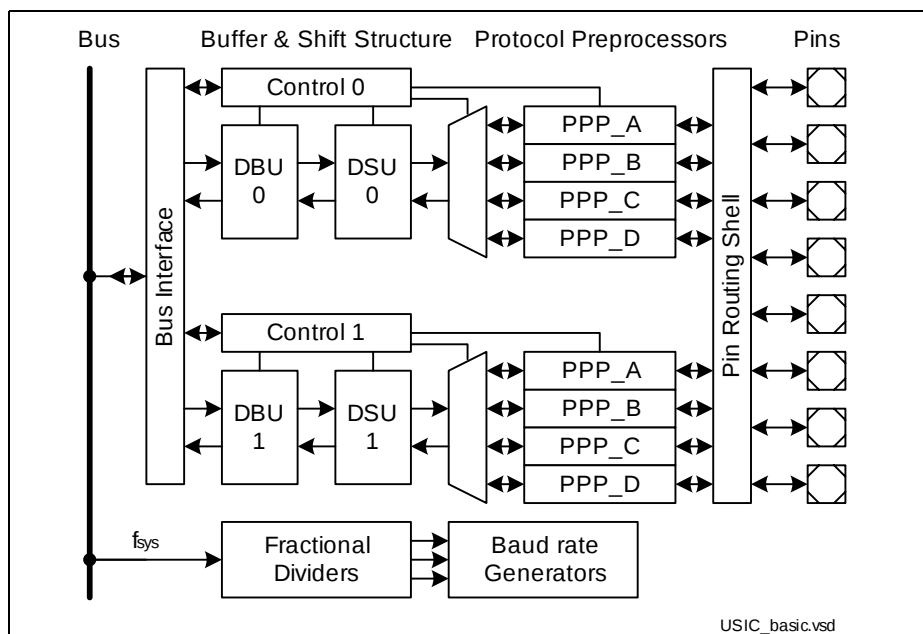


Figure 11 General Structure of a USIC Module

The regular structure of the USIC module brings the following advantages:

- Higher flexibility through configuration with same look-and-feel for data management
- Reduced complexity for low-level drivers serving different protocols
- Wide range of protocols with improved performances (baud rate, buffer handling)

Functional Description

Table 10 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
ROL/ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2
MOV(B)	Move word (byte) data	2 / 4
MOVBS/Z	Move byte operand to word op. with sign/zero extension	2 / 4
JMPA/I/R	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4
JB(C)	Jump relative if direct bit is set (and clear bit)	4
JNB(S)	Jump relative if direct bit is not set (and set bit)	4
CALLA/I/R	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH/POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack and update register with word operand	4
RET(P)	Return from intra-segment subroutine (and pop direct word register from system stack)	2
RETS	Return from inter-segment subroutine	2
RETI	Return from interrupt service subroutine	2
SBRK	Software Break	2
SRST	Software Reset	4
IDLE	Enter Idle Mode	4
PWRDN	Unused instruction ¹⁾	4
SRVWDT	Service Watchdog Timer	4
DISWDT/ENWDT	Disable/Enable Watchdog Timer	4
EINIT	End-of-Initialization Register Lock	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTENDED Register sequence	2
EXTP(R)	Begin EXTENDED Page (and Register) sequence	2 / 4
EXTS(R)	Begin EXTENDED Segment (and Register) sequence	2 / 4

4 Electrical Parameters

The operating range for the XE167xM is defined by its electrical parameters. For proper operation the specified limits must be respected when integrating the device in its target environment.

4.1 General Parameters

These parameters are valid for all subsequent descriptions, unless otherwise noted.

4.1.1 Absolut Maximum Rating Conditions

Stresses above the values listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for an extended time may affect device reliability.

During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < V_{SS}$) the voltage on V_{DDP} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Table 11 Absolute Maximum Rating Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output current on a pin when high value is driven	I_{OH} SR	-30	—	—	mA	
Output current on a pin when low value is driven	I_{OL} SR	—	—	30	mA	
Overload current	I_{OV} SR	-10	—	10	mA	¹⁾
Absolute sum of overload currents	$\Sigma I_{OV} $ SR	—	—	100	mA	¹⁾
Junction Temperature	T_J SR	-40	—	150	°C	
Storage Temperature	T_{ST} SR	-65	—	150	°C	
Digital supply voltage for IO pads and voltage regulators	V_{DDPA} , V_{DDPB} SR	-0.5	—	6.0	V	
Voltage on any pin with respect to ground (V_{SS})	V_{IN} SR	-0.5	—	$V_{DDP} + 0.5$	V	$V_{IN} \leq V_{DDP(max)}$

1) Overload condition occurs if the input voltage V_{IN} is out of the absolute maximum rating range. In this case the current must be limited to the listed values by design measures.

4.1.3 Pad Timing Definition

If not otherwise noted, all timing parameters are tested and are valid for the corresponding output pins operating in strong driver, fast edge mode.

See also [“Pad Properties” on Page 116](#).

4.1.4 Parameter Interpretation

The parameters listed in the following include both the characteristics of the XE167xM and its demands on the system. To aid in correctly interpreting the parameters when evaluating them for a design, they are marked accordingly in the column “Symbol”:

CC (Controller Characteristics):

The logic of the XE167xM provides signals with the specified characteristics.

SR (System Requirement):

The external system must provide signals with the specified characteristics to the XE167xM.

4.2 DC Parameters

These parameters are static or average values that may be exceeded during switching transitions (e.g. output current).

Leakage current is strongly dependent on the operating temperature and the voltage level at the respective pin. The maximum values in the following tables apply under worst case conditions, i.e. maximum temperature and an input level equal to the supply voltage.

The value for the leakage current in an application can be determined by using the respective leakage derating formula (see tables) with values from that application.

The pads of the XE167xM are designed to operate in various driver modes. The DC parameter specifications refer to the pad current limits specified in [Section 4.6.4](#).

Supply Voltage Restrictions

The XE167xM can operate within a wide supply voltage range from 3.0 V to 5.5 V. However, during operation this supply voltage must remain within 10 percent of the selected nominal supply voltage. It cannot vary across the full operating voltage range.

Because of the supply voltage restriction and because electrical behavior depends on the supply voltage, the parameters are specified separately for the upper and the lower voltage range.

During operation, the supply voltages may only change with a maximum speed of $dV/dt < 1 \text{ V/ms}$.

During power-on sequences, the supply voltages may only change with a maximum speed of $dV/dt < 5 \text{ V/}\mu\text{s}$, i.e. the target supply voltage may be reached earliest after approx. 1 μs .

Note: To limit the speed of supply voltage changes, the employment of external buffer capacitors at pins V_{DDPA}/V_{DDPB} is recommended.

Electrical Parameters

Table 14 DC Characteristics for Lower Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output Low Voltage ⁸⁾	$V_{OL\ CC}$	—	—	1.0	V	$I_{OL} \leq I_{OLmax}$
		—	—	0.4	V	$I_{OL} \leq I_{OLnom}$ ¹⁰⁾

- 1) Because each double bond pin is connected to two pads (standard pad and high-speed pad), it has twice the normal value. For a list of affected pins refer to the pin definitions table in chapter 2.
- 2) Not subject to production test - verified by design/characterization. Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot suppress switching due to external system noise under all conditions.
- 3) If the input voltage exceeds the respective supply voltage due to ground bouncing ($V_{IN} < V_{SS}$) or supply ripple ($V_{IN} > V_{DDP}$), a certain amount of current may flow through the protection diodes. This current adds to the leakage current. An additional error current (I_{IN3}) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor K_{OV} .
- 4) The given values are worst-case values. In production test, this leakage current is only tested at 125 °C; other values are ensured by correlation. For derating, please refer to the following descriptions: Leakage derating depending on temperature (T_J = junction temperature [°C]): $I_{OZ} = 0.05 \times e^{(1.5 + 0.028 \times T_J)}$ [μA]. For example, at a temperature of 95 °C the resulting leakage current is 3.2 μA. Leakage derating depending on voltage level ($DV = V_{DDP} - V_{PIN}$ [V]): $I_{OZ} = I_{OZtempmax} - (1.6 \times DV)$ (μA). This voltage derating formula is an approximation which applies for maximum temperature.
- 5) Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: $V_{PIN} \leq V_{IL}$ for a pullup; $V_{PIN} \geq V_{IH}$ for a pulldown.
- 6) These values apply to the fixed pull-devices in dedicated pins and to the user-selectable pull-devices in general purpose IO pins.
- 7) Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: $V_{PIN} \geq V_{IH}$ for a pullup; $V_{PIN} \leq V_{IL}$ for a pulldown.
- 8) The maximum deliverable output current of a port driver depends on the selected output driver mode. This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is determined by the external circuit.
- 9) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL} \rightarrow V_{SS}$, $V_{OH} \rightarrow V_{DDP}$). However, only the levels for nominal output currents are verified.
- 10) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL} \rightarrow V_{SS}$, $V_{OH} \rightarrow V_{DDP}$). However, only the levels for nominal output currents are verified.

4.6 AC Parameters

These parameters describe the dynamic behavior of the XE167xM.

4.6.1 Testing Waveforms

These values are used for characterization and production testing (except pin XTAL1).

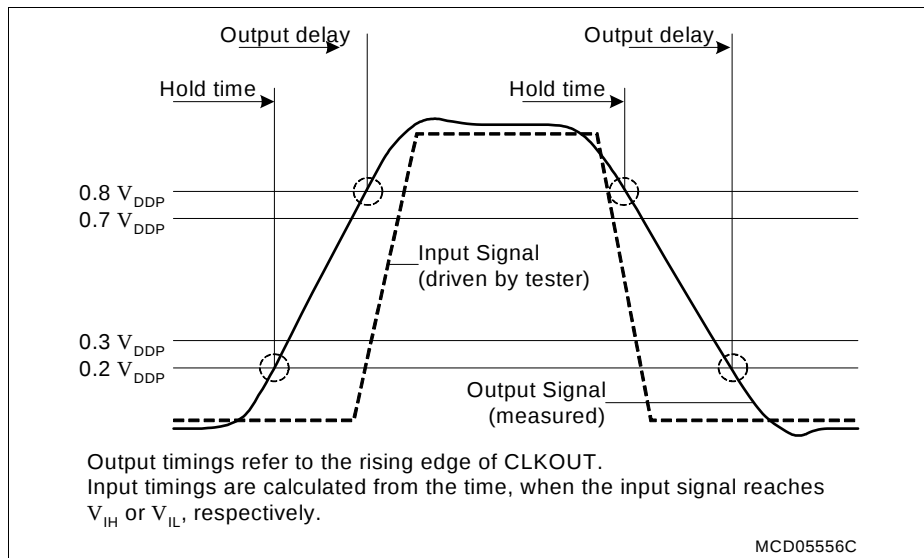


Figure 17 Input Output Waveforms

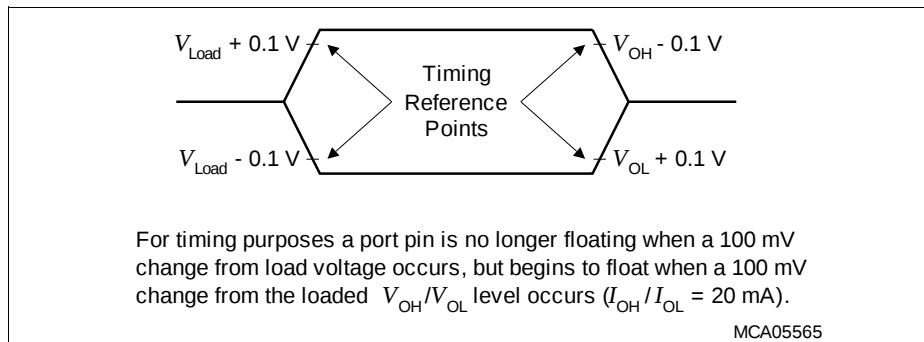


Figure 18 Floating Waveforms

Direct Drive

When direct drive operation is selected (SYSCON0.CLKSEL = 11_B), the system clock is derived directly from the input clock signal CLKIN1:

$$f_{SYS} = f_{IN}$$

The frequency of f_{SYS} is the same as the frequency of f_{IN} . In this case the high and low times of f_{SYS} are determined by the duty cycle of the input clock f_{IN} .

Selecting Bypass Operation from the XTAL1¹⁾ input and using a divider factor of 1 results in a similar configuration.

Prescaler Operation

When prescaler operation is selected (SYSCON0.CLKSEL = 10_B, PLLCON0.VCOBY = 1_B), the system clock is derived either from the crystal oscillator (input clock signal XTAL1) or from the internal clock source through the output prescaler K1 (= K1DIV+1):

$$f_{SYS} = f_{OSC} / K1.$$

If a divider factor of 1 is selected, the frequency of f_{SYS} equals the frequency of f_{OSC} . In this case the high and low times of f_{SYS} are determined by the duty cycle of the input clock f_{OSC} (external or internal).

The lowest system clock frequency results from selecting the maximum value for the divider factor K1:

$$f_{SYS} = f_{OSC} / 1024.$$

4.6.2.1 Phase Locked Loop (PLL)

When PLL operation is selected (SYSCON0.CLKSEL = 10_B, PLLCON0.VCOBY = 0_B), the on-chip phase locked loop is enabled and provides the system clock. The PLL multiplies the input frequency by the factor **F** ($f_{SYS} = f_{IN} \times F$).

F is calculated from the input divider **P** (= PDIV+1), the multiplication factor **N** (= NDIV+1), and the output divider **K2** (= K2DIV+1):

$$(F = N / (P \times K2)).$$

The input clock can be derived either from an external source at XTAL1 or from the on-chip clock source.

The PLL circuit synchronizes the system clock to the input clock. This synchronization is performed smoothly so that the system clock frequency does not change abruptly.

Adjustment to the input clock continuously changes the frequency of f_{SYS} so that it is locked to f_{IN} . The slight variation causes a jitter of f_{SYS} which in turn affects the duration of individual TCSs.

1) Voltages on XTAL1 must comply to the core supply voltage V_{DDIM} .

Table 25 is valid under the following conditions:

$V_{DDP} \geq 4.5 \text{ V}$; $V_{DDPtyp} = 5 \text{ V}$; $V_{DDP} \leq 5.5 \text{ V}$; $C_L \geq 20 \text{ pF}$; $C_L \leq 100 \text{ pF}$;

Table 25 Standard Pad Parameters for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum output driver current (absolute value) ¹⁾	I_{Omax} CC	—	—	10	mA	Strong driver
		—	—	4.0	mA	Medium driver
		—	—	0.5	mA	Weak driver
Nominal output driver current (absolute value)	I_{Onom} CC	—	—	2.5	mA	Strong driver
		—	—	1.0	mA	Medium driver
		—	—	0.1	mA	Weak driver
Rise and Fall times (10% - 90%)	t_{RF} CC	—	—	$4.2 + 0.14 \times C_L$	ns	Strong driver; Sharp edge
		—	—	$11.6 + 0.22 \times C_L$	ns	Strong driver; Medium edge
		—	—	$20.6 + 0.22 \times C_L$	ns	Strong driver; Slow edge
		—	—	$23 + 0.6 \times C_L$	ns	Medium driver
		—	—	$212 + 1.9 \times C_L$	ns	Weak driver

1) The total output current that may be drawn at a given time must be limited to protect the supply rails from damage. For any group of 16 neighboring output pins, the total output current in each direction (ΣI_{OL} and ΣI_{OH}) must remain below 50 mA.

Electrical Parameters

Table 26 is valid under the following conditions:

$V_{DDP} \geq 3.0 \text{ V}$; $V_{DDPtyp} = 3.3 \text{ V}$; $V_{DDP} \leq 4.5 \text{ V}$; $C_L \geq 20 \text{ pF}$; $C_L \leq 100 \text{ pF}$;

Table 26 Standard Pad Parameters for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum output driver current (absolute value) ¹⁾	I_{Omax} CC	—	—	10	mA	Strong driver
		—	—	2.5	mA	Medium driver
		—	—	0.5	mA	Weak driver
Nominal output driver current (absolute value)	I_{Onom} CC	—	—	2.5	mA	Strong driver
		—	—	1.0	mA	Medium driver
		—	—	0.1	mA	Weak driver
Rise and Fall times (10% - 90%)	t_{RF} CC	—	—	$6.2 + 0.24 \times C_L$	ns	Strong driver; Sharp edge
		—	—	$24 + 0.3 \times C_L$	ns	Strong driver; Medium edge
		—	—	$34 + 0.3 \times C_L$	ns	Strong driver; Slow edge
		—	—	$37 + 0.65 \times C_L$	ns	Medium driver
		—	—	$500 + 2.5 \times C_L$	ns	Weak driver

1) The total output current that may be drawn at a given time must be limited to protect the supply rails from damage. For any group of 16 neighboring output pins, the total output current in each direction (ΣI_{OL} and ΣI_{OH}) must remain below 50 mA.

Table 30 EBC External Bus Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output valid delay for $\overline{RD}$, $\overline{WR}(L/H)$	t_{10} CC	–	11	20	ns	
Output valid delay for BHE, ALE	t_{11} CC	–	10	21	ns	
Address output valid delay for A23 ... A0	t_{12} CC	–	11	22	ns	
Address output valid delay for AD15 ... AD0 (MUX mode)	t_{13} CC	–	10	22	ns	
Output valid delay for $\overline{CS}$	t_{14} CC	–	10	13	ns	
Data output valid delay for AD15 ... AD0 (write data, MUX mode)	t_{15} CC	–	10	22	ns	
Data output valid delay for D15 ... D0 (write data, DEMUX mode)	t_{16} CC	–	10	22	ns	
Output hold time for $\overline{RD}$, $\overline{WR}(L/H)$	t_{20} CC	-2	8	10	ns	
Output hold time for BHE, ALE	t_{21} CC	-2	8	10	ns	
Address output hold time for AD15 ... AD0	t_{23} CC	-3	8	10	ns	
Output hold time for $\overline{CS}$	t_{24} CC	-3	8	11	ns	
Data output hold time for D15 ... D0 and AD15 ... AD0	t_{25} CC	-3	8	10	ns	
Input setup time for READY, D15 ... D0, AD15 ... AD0	t_{30} SR	29	17	–	ns	
Input hold time READY, D15 ... D0, AD15 ... AD0 ¹⁾	t_{31} SR	0	-9	–	ns	

1) Read data are latched with the same internal clock edge that triggers the address change and the rising edge of $\overline{RD}$. Address changes before the end of $\overline{RD}$ have no impact on (demultiplexed) read cycles. Read data can change after the rising edge of $\overline{RD}$.

5.3 Quality Declarations

The operation lifetime of the XE167xM depends on the operating temperature. The life time decreases with increasing temperature as shown in [Table 43](#).

Table 42 Quality Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Operation lifetime	t_{OP} CC	–	–	20	a	See Table 43
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	–	–	2 000	V	EIA/JESD22-A114-B
Moisture sensitivity level	MSL CC	–	–	3	–	JEDEC J-STD-020C

Table 43 Lifetime dependency from Temperature

Operating Time	Operating Temperature
20 a	$T_J \leq 110^{\circ}\text{C}$
95 500 h	$T_J = 120^{\circ}\text{C}$
68 500 h	$T_J = 125^{\circ}\text{C}$
49 500 h	$T_J = 130^{\circ}\text{C}$
26 400 h	$T_J = 140^{\circ}\text{C}$
14 500 h	$T_J = 150^{\circ}\text{C}$