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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16-Bit
Speed	80MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	119
Program Memory Size	576KB (576K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	50K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-144-4
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xe167hm72f80laafxuma1

16-Bit Single-Chip Real Time Signal Controller
XE167xM (XE166 Family)

1 Summary of Features

For a quick overview and easy reference, the features of the XE167xM are summarized here.

- High-performance CPU with five-stage pipeline and MPU
  - 12.5 ns instruction cycle at 80 MHz CPU clock (single-cycle execution)
  - One-cycle 32-bit addition and subtraction with 40-bit result
  - One-cycle multiplication (16 × 16 bit)
  - Background division (32 / 16 bit) in 21 cycles
  - One-cycle multiply-and-accumulate (MAC) instructions
  - Enhanced Boolean bit manipulation facilities
  - Zero-cycle jump execution
  - Additional instructions to support HLL and operating systems
  - Register-based design with multiple variable register banks
  - Fast context switching support with two additional local register banks
  - 16 Mbytes total linear address space for code and data
  - 1024 Bytes on-chip special function register area (C166 Family compatible)
  - Integrated Memory Protection Unit (MPU)
- Interrupt system with 16 priority levels for up to 96 sources
  - Selectable external inputs for interrupt generation and wake-up
  - Fastest sample-rate 12.5 ns
- Eight-channel interrupt-driven single-cycle data transfer with Peripheral Event Controller (PEC), 24-bit pointers cover total address space
- Clock generation from internal or external clock sources, using on-chip PLL or prescaler
- Hardware CRC-Checker with Programmable Polynomial to Supervise On-Chip Memory Areas
- On-chip memory modules
  - 8 Kbytes on-chip stand-by RAM (SBRAM)
  - 2 Kbytes on-chip dual-port RAM (DPRAM)
  - Up to 16 Kbytes on-chip data SRAM (DSRAM)
  - Up to 32 Kbytes on-chip program/data SRAM (PSRAM)
  - Up to 576 Kbytes on-chip program memory (Flash memory)
  - Memory content protection through Error Correction Code (ECC)
- On-Chip Peripheral Modules
  - Multi-functional general purpose timer unit with 5 timers
  - 16-channel general purpose capture/compare unit (CAPCOM2)
  - Up to 4 capture/compare units for flexible PWM signal generation (CCU6x)

1.1 Basic Device Types

Basic device types are available and can be ordered through Infineon's direct and/or distribution channels.

Table 1 Synopsis of XE167xM Basic Device Types

Derivative[1)]	Flash Memory[2)]	PSRAM DSRAM[3)]	Capt./Comp. Modules	ADC[4)] Chan.	Interfaces[4)]
XE167FM-72FxxL	576 Kbytes	32 Kbytes 16 Kbytes	CC2 CCU60/1/2/3	16 + 8	6 CAN Nodes, 8 Serial Chan.
XE167FM-48FxxL	384 Kbytes	16 Kbytes 16 Kbytes	CC2 CCU60/1/2/3	16 + 8	6 CAN Nodes, 8 Serial Chan.
XE167GM-72FxxL	576 Kbytes	32 Kbytes 16 Kbytes	CC2 CCU60/1	8 + 8	2 CAN Nodes, 4 Serial Chan.
XE167GM-48FxxL	384 Kbytes	16 Kbytes 16 Kbytes	CC2 CCU60/1	8 + 8	2 CAN Nodes, 4 Serial Chan.
XE167HM-72FxxL	576 Kbytes	32 Kbytes 16 Kbytes	CC2 CCU60/1/2/3	16 + 8	No CAN Nodes, 8 Serial Chan.
XE167HM-48FxxL	384 Kbytes	16 Kbytes 16 Kbytes	CC2 CCU60/1/2/3	16 + 8	No CAN Nodes, 8 Serial Chan.
XE167KM-72FxxL	576 Kbytes	32 Kbytes 16 Kbytes	CC2 CCU60/1	8 + 8	No CAN Nodes, 4 Serial Chan.
XE167KM-48FxxL	384 Kbytes	16 Kbytes 16 Kbytes	CC2 CCU60/1	8 + 8	No CAN Nodes, 4 Serial Chan.

1) xx is a placeholder for the available speed grade (in MHz).
2) Specific information about the on-chip Flash memory in **Table 2**.
3) All derivatives additionally provide 8 Kbytes SBRAM and 2 Kbytes DPRAM.
4) Specific information about the available channels in **Table 4**.
Analog input channels are listed for each Analog/Digital Converter module separately (ADC0 + ADC1).

The XE167xM types are offered with several SRAM memory sizes. **Figure 1** shows the allocation rules for PSRAM and DSRAM. Note that the rules differ:

- PSRAM allocation starts from the **lower** address
- DSRAM allocation starts from the **higher** address

For example 8 Kbytes of PSRAM will be allocated at E0’0000h-E0’1FFFh and 8 Kbytes of DSRAM will be at 00’C000h-00’DFFFh.

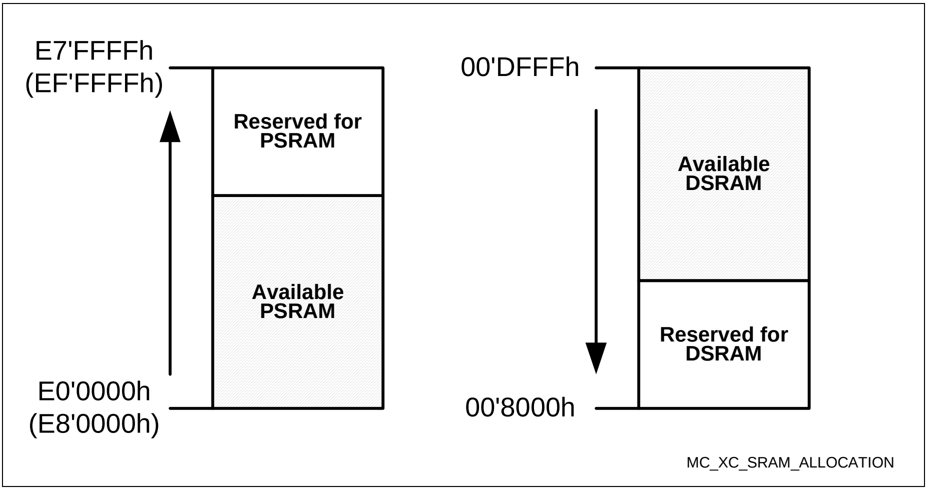

Figure 1 SRAM Allocation

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
5	P8.4	O0 / I	St/B	**Bit 4 of Port 8, General Purpose Input/Output**
	CCU60_COUT61	O1	St/B	**CCU60 Channel 1 Output**
	CCU62_CC61	O2	St/B	**CCU62 Channel 1 Output**
	TMS_D	IH	St/B	**JTAG Test Mode Selection Input** If JTAG pos. D is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it.
	CCU62_CC61INB	I	St/B	**CCU62 Channel 1 Input**
6	$\overline{\text{TRST}}$	I	In/B	**Test-System Reset Input** For normal system operation, pin $\overline{\text{TRST}}$ should be held low. A high level at this pin at the rising edge of $\overline{\text{PORST}}$ activates the XE167xM's debug system. In this case, pin $\overline{\text{TRST}}$ must be driven low once to reset the debug system. An internal pull-down device will hold this pin low when nothing is driving it.
7	P8.3	O0 / I	St/B	**Bit 3 of Port 8, General Purpose Input/Output**
	CCU60_COUT60	O1	St/B	**CCU60 Channel 0 Output**
	CCU62_CC60	O2	St/B	**CCU62 Channel 0 Output**
	TDI_D	IH	St/B	**JTAG Test Data Input** If JTAG pos. D is selected during start-up, an internal pull-up device will hold this pin low when nothing is driving it.
	CCU62_CC60INB	I	St/B	**CCU62 Channel 0 Input**

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
66	P11.0	O0 / I	St/B	**Bit 0 of Port 11, General Purpose Input/Output**
	CCU61_COUT60	O1	St/B	**CCU61 Channel 0 Output**
	U3C1_SCLKOUT	O2	St/B	**USIC3 Channel 1 Shift Clock Output**
	CCU63_CCPOS0A	I	St/B	**CCU63 Position Input 0**
	RxDC0F	I	St/B	**CAN Node 0 Receive Data Input**
	U3C1_DX1A	I	St/B	**USIC3 Channel 1 Shift Clock Input**
	ESR1_7	I	St/B	**ESR1 Trigger Input 7**
67	P2.5	O0 / I	St/B	**Bit 5 of Port 2, General Purpose Input/Output**
	U0C0_SCLKOUT	O1	St/B	**USIC0 Channel 0 Shift Clock Output**
	TxDC0	O2	St/B	**CAN Node 0 Transmit Data Output**
	CC2_CC18	O3 / I	St/B	**CAPCOM2 CC18IO Capture Inp./ Compare Out.**
	A18	OH	St/B	**External Bus Interface Address Line 18**
	U0C0_DX1D	I	St/B	**USIC0 Channel 0 Shift Clock Input**
	ESR1_10	I	St/B	**ESR1 Trigger Input 10**
68	P4.2	O0 / I	St/B	**Bit 2 of Port 4, General Purpose Input/Output**
	U3C0_SCLKOUT	O1	St/B	**USIC3 Channel 0 Shift Clock Output**
	TxDC2	O2	St/B	**CAN Node 2 Transmit Data Output**
	CC2_CC26	O3 / I	St/B	**CAPCOM2 CC26IO Capture Inp./ Compare Out.**
	$\overline{\text{CS2}}$	OH	St/B	**External Bus Interface Chip Select 2 Output**
	T2INA	I	St/B	**GPT12E Timer T2 Count/Gate Input**
	CCU62_CCPOS1B	I	St/B	**CCU62 Position Input 1**
	U3C0_DX1B	I	St/B	**USIC3 Channel 0 Shift Clock Input**

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
95	P10.3	O0 / I	St/B	**Bit 3 of Port 10, General Purpose Input/Output**
	CCU60_COUT60	O2	St/B	**CCU60 Channel 0 Output**
	AD3	OH / IH	St/B	**External Bus Interface Address/Data Line 3**
	U0C0_DX2A	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX2A	I	St/B	**USIC0 Channel 1 Shift Control Input**
	U3C0_DX0A	I	St/B	**USIC3 Channel 0 Shift Data Input**
96	P0.5	O0 / I	St/B	**Bit 5 of Port 0, General Purpose Input/Output**
	U1C1_SCLKOUT	O1	St/B	**USIC1 Channel 1 Shift Clock Output**
	U1C0_SELO2	O2	St/B	**USIC1 Channel 0 Select/Control 2 Output**
	CCU61_COUT62	O3	St/B	**CCU61 Channel 2 Output**
	A5	OH	St/B	**External Bus Interface Address Line 5**
	U1C1_DX1A	I	St/B	**USIC1 Channel 1 Shift Clock Input**
	U1C0_DX1C	I	St/B	**USIC1 Channel 0 Shift Clock Input**
	RXDC3E	I	St/B	**CAN Node 3 Receive Data Input**
97	P3.3	O0 / I	St/B	**Bit 3 of Port 3, General Purpose Input/Output**
	U2C0_SELO0	O1	St/B	**USIC2 Channel 0 Select/Control 0 Output**
	U2C1_SELO1	O2	St/B	**USIC2 Channel 1 Select/Control 1 Output**
	U2C0_DX2A	I	St/B	**USIC2 Channel 0 Shift Control Input**
	RxDC3A	I	St/B	**CAN Node 3 Receive Data Input**

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
113	P10.8	O0 / I	St/B	**Bit 8 of Port 10, General Purpose Input/Output**
	U0C0_MCLKOUT	O1	St/B	**USIC0 Channel 0 Master Clock Output**
	U0C1_SELO0	O2	St/B	**USIC0 Channel 1 Select/Control 0 Output**
	U2C1_DOUT	O3	St/B	**USIC2 Channel 1 Shift Data Output**
	AD8	OH / IH	St/B	**External Bus Interface Address/Data Line 8**
	CCU60_CCPOS1A	I	St/B	**CCU60 Position Input 1**
	U0C0_DX1C	I	St/B	**USIC0 Channel 0 Shift Clock Input**
	$\overline{\text{BRKIN\_B}}$	I	St/B	**OCDS Break Signal Input**
	T3EUDB	I	St/B	**GPT12E Timer T3 External Up/Down Control Input**
114	P9.1	O0 / I	St/B	**Bit 1 of Port 9, General Purpose Input/Output**
	CCU63_CC61	O1	St/B	**CCU63 Channel 1 Output**
	CCU63_CC61INA	I	St/B	**CCU63 Channel 1 Input**

Table 5 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
137	XTAL1	I	Sp/M	**Crystal Oscillator Amplifier Input** To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Voltages on XTAL1 must comply to the core supply voltage V_{DDIM}.
	ESR2_9	I	St/B	**ESR2 Trigger Input 9**
138	$\overline{\text{PORST}}$	I	In/B	**Power On Reset Input** A low level at this pin resets the XE167xM completely. A spike filter suppresses input pulses <10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 120 ns. An internal pull-up device will hold this pin high when nothing is driving it.
139	$\overline{\text{ESR1}}$	O0 / I	St/B	**External Service Request 1** After power-up, an internal weak pull-up device holds this pin high when nothing is driving it.
	RxDC0E	I	St/B	**CAN Node 0 Receive Data Input**
	U1C0_DX0F	I	St/B	**USIC1 Channel 0 Shift Data Input**
	U1C0_DX2C	I	St/B	**USIC1 Channel 0 Shift Control Input**
	U1C1_DX0C	I	St/B	**USIC1 Channel 1 Shift Data Input**
	U1C1_DX2B	I	St/B	**USIC1 Channel 1 Shift Control Input**
	U2C1_DX2C	I	St/B	**USIC2 Channel 1 Shift Control Input**

Table 10 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
NOP	Null operation	2
CoMUL/CoMAC	Multiply (and accumulate)	4
CoADD/CoSUB	Add/Subtract	4
Co(A)SHR	(Arithmetic) Shift right	4
CoSHL	Shift left	4
CoLOAD/STORE	Load accumulator/Store MAC register	4
CoCMP	Compare	4
CoMAX/MIN	Maximum/Minimum	4
CoABS/CoRND	Absolute value/Round accumulator	4
CoMOV	Data move	4
CoNEG/NOP	Negate accumulator/Null operation	4

1) The Enter Power Down Mode instruction is not used in the XE167xM, due to the enhanced power control scheme. PWRDN will be correctly decoded, but will trigger no action.

4.1.2 Operating Conditions

The following operating conditions must not be exceeded to ensure correct operation of the XE167xM. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Note: Typical parameter values refer to room temperature and nominal supply voltage, minimum/maximum parameter values also include conditions of minimum/maximum temperature and minimum/maximum supply voltage. Additional details are described where applicable.

Table 12 Operating Conditions

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Voltage Regulator Buffer Capacitance for DMP_M	C_{EVRM} SR	1.0	–	4.7	µF	[1]
Voltage Regulator Buffer Capacitance for DMP_1	C_{EVR1} SR	0.47	–	2.2	µF	[1][2]
External Load Capacitance	C_L SR	–	20[3]	–	pF	pin out driver= default [4]
System frequency	f_{SYS} SR	–	–	100	MHz	[5]
Overload current for analog inputs[6]	I_{OVA} SR	-2	–	5	mA	not subject to production test
Overload current for digital inputs[6]	I_{OVD} SR	-5	–	5	mA	not subject to production test
Overload current coupling factor for analog inputs[7]	K_{OVA} CC	–	2.5 x 10^{-4}	1.5 x 10^{-3}	-	I_{OV} < 0 mA; not subject to production test
		–	1.0 x 10^{-6}	1.0 x 10^{-4}	-	I_{OV} > 0 mA; not subject to production test
Overload current coupling factor for digital I/O pins	K_{OVD} CC	–	1.0 x 10^{-2}	3.0 x 10^{-2}		I_{OV} < 0 mA; not subject to production test
		–	1.0 x 10^{-4}	5.0 x 10^{-3}		I_{OV} > 0 mA; not subject to production test

Pullup/Pulldown Device Behavior

Most pins of the XE167xM feature pullup or pulldown devices. For some special pins these are fixed; for the port pins they can be selected by the application.

The specified current values indicate how to load the respective pin depending on the intended signal level. **Figure 13** shows the current paths.

The shaded resistors shown in the figure may be required to compensate system pull currents that do not match the given limit values.

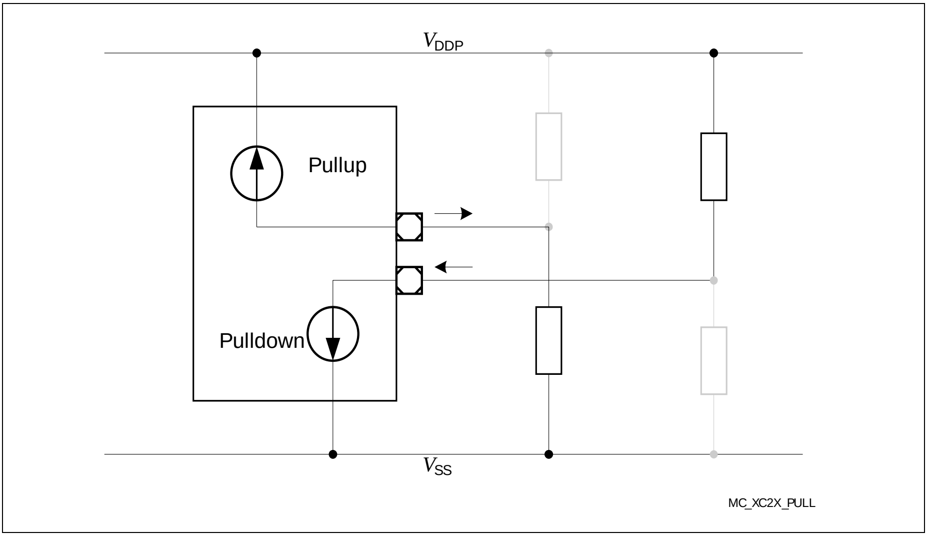

Figure 13 Pullup/Pulldown Current Definition

Table 13 DC Characteristics for Upper Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output Low Voltage[8)]	V_{OL} CC	–	–	1.0	V	$I_{OL} \leq I_{OLmax}$
		–	–	0.4	V	$I_{OL} \leq I_{OLnom}$[9)]

1) Because each double bond pin is connected to two pads (standard pad and high-speed pad), it has twice the normal value. For a list of affected pins refer to the pin definitions table in chapter 2.

2) Not subject to production test - verified by design/characterization. Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot suppress switching due to external system noise under all conditions.

3) If the input voltage exceeds the respective supply voltage due to ground bouncing ($V_{IN} < V_{SS}$) or supply ripple ($V_{IN} > V_{DDP}$), a certain amount of current may flow through the protection diodes. This current adds to the leakage current. An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor K_{OV}.

4) The given values are worst-case values. In production test, this leakage current is only tested at 125 °C; other values are ensured by correlation. For derating, please refer to the following descriptions: Leakage derating depending on temperature (T_J = junction temperature [°C]): I_{OZ} = 0.05 x $e^{(1.5 + 0.028 \times TJ>)}$ [µA]. For example, at a temperature of 95 °C the resulting leakage current is 3.2 µA. Leakage derating depending on voltage level (DV = V_{DDP} - V_{PIN} [V]): $I_{OZ} = I_{OZtempmax}$ - (1.6 x DV) (µA]. This voltage derating formula is an approximation which applies for maximum temperature.

5) Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: $V_{PIN} \leq V_{ILmax}$ for a pullup; $V_{PIN} \geq V_{IHmin}$ for a pulldown.

6) These values apply to the fixed pull-devices in dedicated pins and to the user-selectable pull-devices in general purpose IO pins.

7) Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: $V_{PIN} \geq V_{IHmin}$ for a pullup; $V_{PIN} \leq V_{ILmax}$ for a pulldown.

8) The maximum deliverable output current of a port driver depends on the selected output driver mode. This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is determined by the external circuit.

9) As a rule, with decreasing output current the output levels approach the respective supply level (V_{OL}->V_{SS}, V_{OH}->V_{DDP}). However, only the levels for nominal output currents are verified.

4.4 System Parameters

The following parameters specify several aspects which are important when integrating the XE167xM into an application system.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 19 Various System Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Short-term deviation of internal clock source frequency[1]	Δf_{INT} CC	-1	–	1	%	$\Delta T_J \leq 10$ °C
Internal clock source frequency	f_{INT} CC	4.8	5.0	5.2	MHz	
Wakeup clock source frequency[2]	f_{WU} CC	400	–	700	kHz	FREQSEL= 00
		210	–	390	kHz	FREQSEL= 01
		140	–	260	kHz	FREQSEL= 10
		110	–	200	kHz	FREQSEL= 11
Startup time from power-on with code execution from Flash	t_{SPO} CC	1.8	2.2	2.7	ms	f_{WU} = 500 kHz
Startup time from stopover mode with code execution from PSRAM	t_{SSO} CC	11 / f_{WU}[3]	–	12 / f_{WU}[3]	µs	
Core voltage (PVC) supervision level	V_{PVC} CC	V_{LV} - 0.03	V_{LV}	V_{LV} + 0.07[4]	V	[5]
Supply watchdog (SWD) supervision level	V_{SWD} CC	V_{LV} - 0.10[6]	V_{LV}	V_{LV} + 0.15	V	Lower voltage range[5]
		V_{LV} - 0.15	V_{LV}	V_{LV} + 0.15	V	Upper voltage range[5]

1) The short-term frequency deviation refers to a timeframe of a few hours and is measured relative to the current frequency at the beginning of the respective timeframe. This parameter is useful to determine a time span for re-triggering a LIN synchronization.

2) This parameter is tested for the fastest and the slowest selection. The medium selections are not subject to production test - verified by design/characterization

Table 22 Flash Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Number of erase cycles	N_{Er} SR	–	–	15 000	cycles	$t_{RET} \geq 5$ years; Valid for up to 64 user-selected sectors (data storage)
		–	–	1 000	cycles	$t_{RET} \geq 20$ years

1) All Flash module(s) can be erased/programmed while code is executed and/or data is read from only one Flash module or from PSRAM. The Flash module that delivers code/data can, of course, not be erased/programmed.

2) Flash module 3 can be erased/programmed while code is executed and/or data is read from any other Flash module.

3) Value of IMB_IMBCTRL.WSFLASH.

4) Programming and erase times depend on the internal Flash clock source. The control state machine needs a few system clock cycles. This increases the stated durations noticably only at extremely low system clock frequencies.

Access to the XE167xM Flash modules is controlled by the IMB. Built-in prefetch mechanisms optimize the performance for sequential access.

Flash access waitstates only affect non-sequential access. Due to prefetch mechanisms, the performance for sequential access (depending on the software structure) is only partially influenced by waitstates.

Table 26 is valid under the following conditions:
$V_{DDP} \geq 3.0$ V; $V_{DDPtyp} = 3.3$ V; $V_{DDP} \leq 4.5$ V; $C_L \geq 20$ pF; $C_L \leq 100$ pF;

Table 26 Standard Pad Parameters for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum output driver current (absolute value)[1]	I_{Omax} CC	–	–	10	mA	Strong driver
		–	–	2.5	mA	Medium driver
		–	–	0.5	mA	Weak driver
Nominal output driver current (absolute value)	I_{Onom} CC	–	–	2.5	mA	Strong driver
		–	–	1.0	mA	Medium driver
		–	–	0.1	mA	Weak driver
Rise and Fall times (10% - 90%)	t_{RF} CC	–	–	6.2 + 0.24 x C_L	ns	Strong driver; Sharp edge
		–	–	24 + 0.3 x C_L	ns	Strong driver; Medium edge
		–	–	34 + 0.3 x C_L	ns	Strong driver; Slow edge
		–	–	37 + 0.65 x C_L	ns	Medium driver
		–	–	500 + 2.5 x C_L	ns	Weak driver

1) The total output current that may be drawn at a given time must be limited to protect the supply rails from damage. For any group of 16 neighboring output pins, the total output current in each direction (ΣI_{OL} and $\Sigma\text{-}I_{OH}$) must remain below 50 mA.

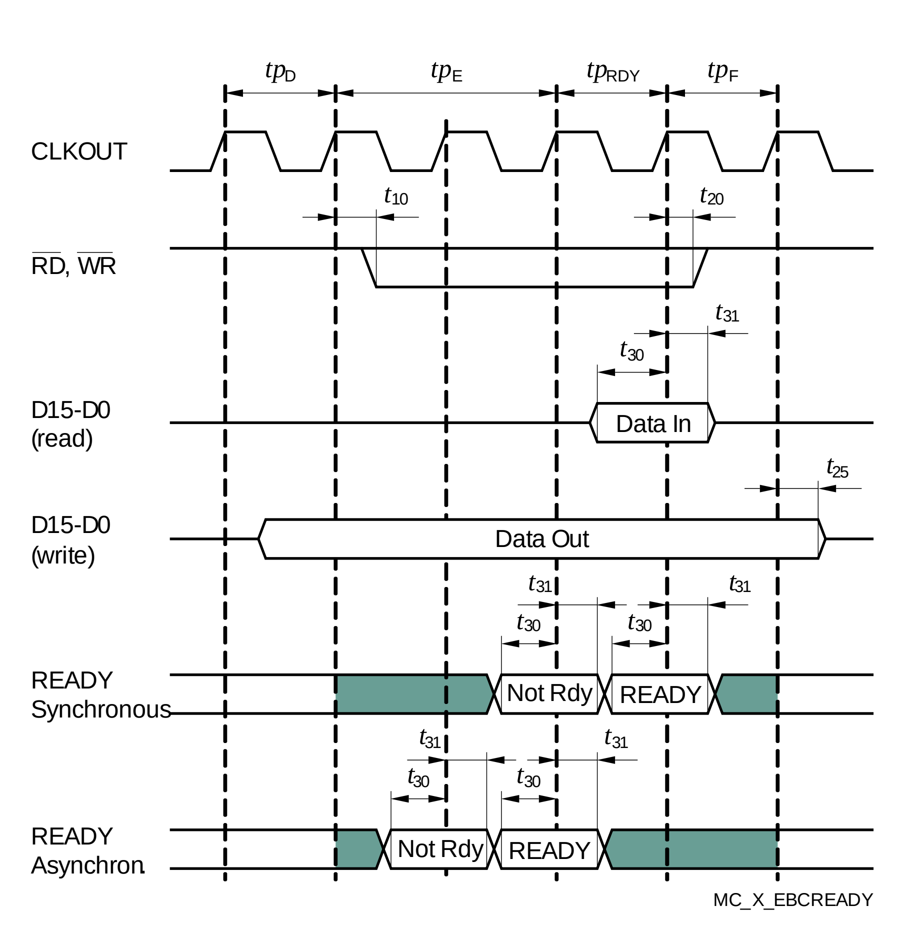

Figure 25 READY Timing

Note: If the READY input is sampled inactive at the indicated sampling point ("Not Rdy") a READY-controlled waitstate is inserted (tpRDY),
sampling the READY input active at the indicated sampling point ("Ready") terminates the currently running bus cycle.
Note the different sampling points for synchronous and asynchronous READY.
This example uses one mandatory waitstate (see tpE) before the READY input value is used.

4.6.6 Synchronous Serial Interface Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply; C_L = 20 pF.

Table 33 USIC SSC Master Mode Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Slave select output SELO active to first SCLKOUT transmit edge	t_1 CC	t_{SYS} - 8 [1)]	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2 CC	t_{SYS} - 6 [1)]	–	–	ns	
Data output DOUT valid time	t_3 CC	-6	–	9	ns	
Receive data input setup time to SCLKOUT receive edge	t_4 SR	31	–	–	ns	
Data input DX0 hold time from SCLKOUT receive edge	t_5 SR	-4	–	–	ns	

1) $t_{SYS} = 1 / f_{SYS}$

Table 34 USIC SSC Master Mode Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Slave select output SELO active to first SCLKOUT transmit edge	t_1 CC	t_{SYS} - 10 [1)]	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2 CC	t_{SYS} - 9 [1)]	–	–	ns	
Data output DOUT valid time	t_3 CC	-7	–	11	ns	

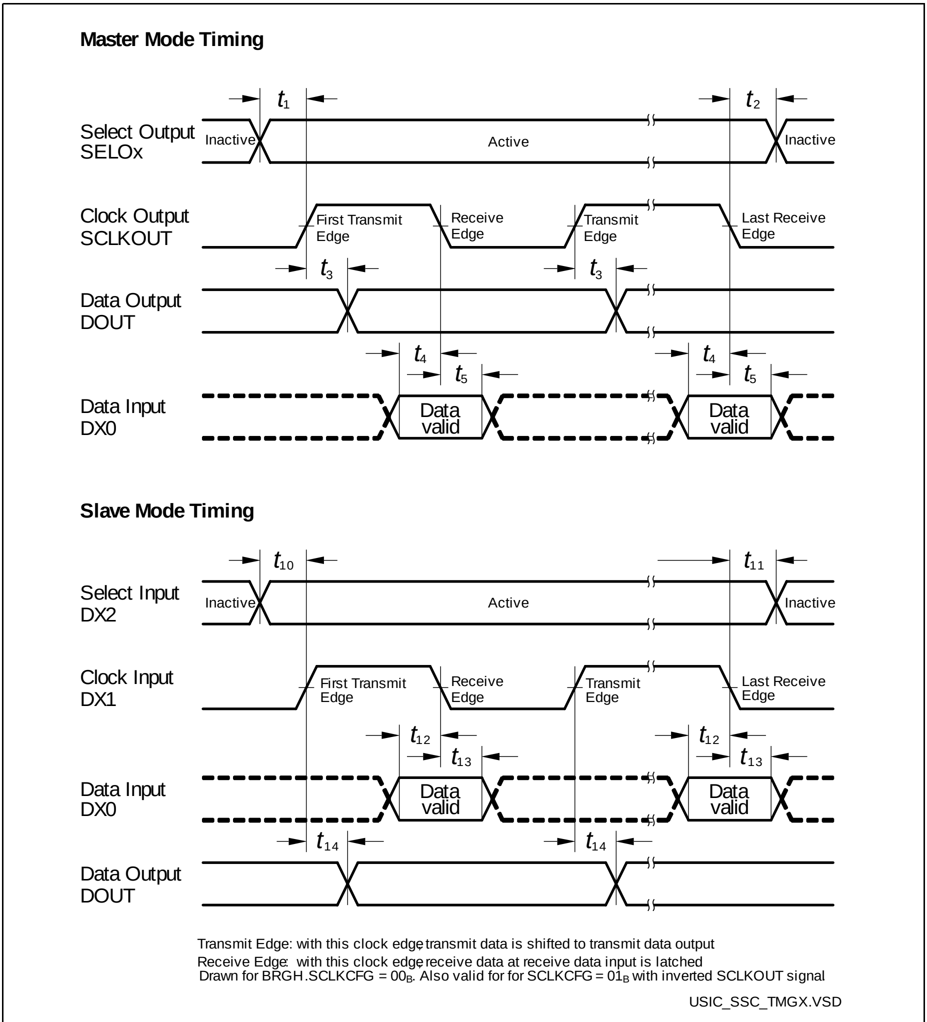

Figure 28 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration where the slave select signal is low-active and the serial clock signal is not shifted and not inverted.

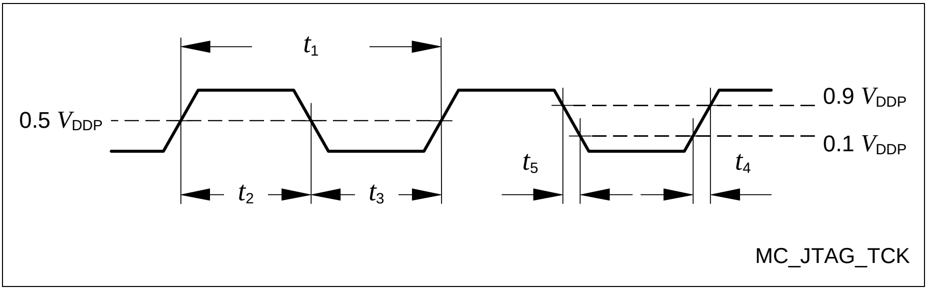

Figure 32 Test Clock Timing (TCK)

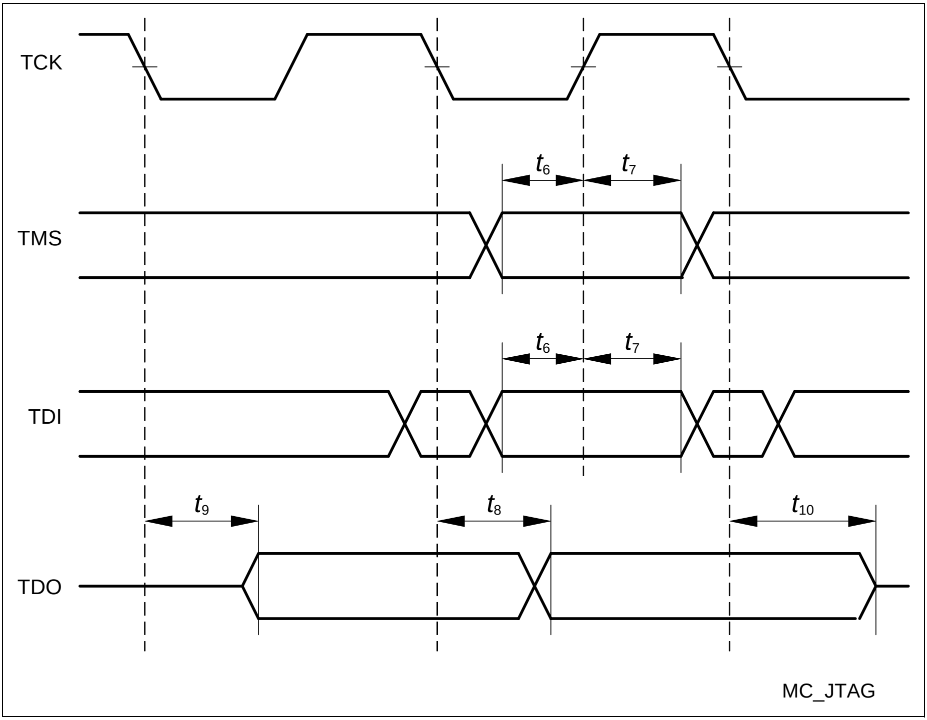

Figure 33 JTAG Timing